Testing Embedded Toggle Generation Through On-Chip IR Drop Measurements

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I. INTRODUCTION

In integrated circuit (IC)-test, the test equipment applies test stimuli on the inputs of the IC and the IC's responses are compared to the expected responses. Test patterns are generated by an automatic test pattern generator (ATPG). The traditional test generation approach treated the full IC as one unit for ATPG. The staggering gate count of today's digital designs, especially for system-on-a-chip (SoC) and three-dimensional stacked ICs (3D-SIC), makes the traditional test generation approach become intractable. Today, most SoCs and 3DICs are tested with modular test approaches [1].

Test application time is one of its key performance indicators. ATPG traditionally tries to cramp as much switching as possible into each test pattern, to maximize the fault coverage per a test pattern, and hence minimize the required number of test patterns and corresponding test application time. Consequently, the switching activity during test is significantly higher than during functional operation[2]. To avoid excess PS current, ATPG tools provide support to generate 'low-power' test patterns. Without considerations, low-power ATPG is only effective for the module under tests (MUTs) [2]. Test patterns generated for a particular module will appear as (near-)random test stimuli to all other ('neighbor') modules. One of the ways to avoid such (near-)random test stimuli in neighbor modules is shielding those modules by gating scan chains, gating clock signal, but it might provide too optimistic test condition and cause test escapes ('false negatives')[3]. In [2], embedded programmable toggle generator (ePTG) is used to create a realistic test condition. However it is difficult to correctly evaluate internal operations of an ePTG without observing any digital output.

Recent SoC very large scale integration (VLSI) chips contain embedded toggle generators for various objectives, such as (1) stabilizing the voltage variations on a power supply (PS) network in high-bandwidth wireline circuits [4], (2) emulating background switching activity during test to create a realistic test environment [2], and (3) equalizing PS noise to improve resiliency against power side-channel attacks [5]. These circuits provide the effect of intentionally designed power consumption without direct outputs. Some functional blocks need to be fully turned off to meet the power budget of the whole SoC VLSI chip in a many-core heterogeneous architecture. Those non-powered areas, called dark silicon [6], move around over time within a big chip, according to the contexts of processing.

A mechanism is needed that confirms the proper amount of toggles in those circuits without digital outputs which can be complementary to traditional function-based testing. There are some previous works combining testing, on-chip monitoring and PS noise [7][8], however, which are mainly for validating PS noise analysis techniques over the time duration of highly activated operation, and do not meet the toggle verification at the resolution of a single clock cycle.

In this paper, an IR-drop-based power-domain scenario-based testing and in-field diagnosis technique using on-chip monitor (OCM) circuits is presented. The number of toggled gates can be precisely estimated from dynamic IR-drop waveforms on PS nodes in each power domain locally supplied with a micro voltage regulator module (μVRM). The proposed technique realizes in-place quantitative evaluation of toggles among power domains granularly defined in SoC chips. The toggle patterns can be designed through test pattern generation algorithms.

On-chip PS and substrate noise measurement techniques have been reported for various objectives in the literature. A built-in current sensing technique measured substrate current to find faulty transistors in analog circuits [9]. Another built-in technique visualized dynamic IR drops distributed in a microprocessor and related with fault mechanisms [10]. On-chip measurements in those papers have contributed to the accurate understandings of PS noise and interference mechanisms. In contrast, the usage of OCM in this paper is intended for the scenario-based testing and in-field diagnosis of power domains among circuit blocks without visible outputs, which is suitable for SoC VLSI chips with granular power managements.

II. POWER-DOMAIN TESTING AND DIAGNOSIS OF TOGGLE PATTERN GENERATION

A. General architecture with ePTGs and OCMs

An SoC VLSI chip has multiple power domains for functional cores, as depicted in Figure 1a. Each domain is regulated by μVRM at the DC voltage of V_{DD} for meeting required operation performance and isolated from the others. A power domain can include an ePTG [2], which has the function of creating an on-chip generated switching activity of a user-defined programmable level. The program to toggle generation is digitally coded and preloaded in status registers of an ePTG. While digital output is not given, PS current, I_{DD}, is consumed and leads to dynamic IR drop. The chip also includes OCM waveform capturing and processing functions.

The OCM has input-channel interconnects to the power (V_{DD}) and ground (V_{SS}) rail to capture the dynamic IR-drop waveforms. The waveforms are then processed and evaluated in the following dynamic IR-drop-based toggle diagnosis. There are multiple input channels to probe and diagnose the power domains of interest.

The ePTG is intended to maintain PS current at the programmed level of power consumption, and also to smooth

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PS current and prevent from over- and under-shooting in PS voltage. The intentional toggle generation is used for various objectives in recent SoC VLSI chips as we described in Sec. I [4][5][7]. For the sake of generality in the following part of this paper, the ePTG is chosen as a MUT with designed and controlled switching among logic gate cells.

B. On-chip monitor

The OCM captures the PS voltage waveforms in the power domain of interest. The OCM circuits, Figure 1b, include a source follower (SF) to sense the voltage of interest at its input and a subsequent single-bit comparator for digitizing the output of SF. The iterative comparisons are made for time and voltage discretization as in [10] and others.

The strobe timing, T_S, is in phase and shifted in a stepwise way relative to the system clock of the SoC. The reference voltage, V_R, is also changed in a staircase way. The comparator indicates at its output whether the input voltage, V_{SF}, is larger than V_R at the timing of T_S. The most approximate voltage of V_{SF} is searched in the staircase of V_R through iterative comparisons by the comparator, and then the process is repeated at the next timestep of length T_S. Finally, the time evolvement of approximated V_{SF} provides a voltage waveform. The relation of the input to output voltages are calibrated with known slopes or sinusoids before diagnosis.

C. Dynamic IR-drop PS waveform

The time-domain PS voltage, $V_{DD}(t)$, is related with PS current, $I_{DD}(t)$, according to (1) where Z_{DD} represents PS impedance associated with a power domain. Since the domain is compactly confined to the silicon area of digital standard cells, Z_{DD} is mainly dominated by metal wirings forming power rails. The off-chip impedance brings substantial impacts on the characteristics of system wide power delivery networks. However, on-chip power domains can be effectively decoupled by µVRMs.

$$V_{DD}(t) = Z_{DD} * I_{DD}(t) \quad (1)$$

While the V_{DD} side of power rails is regulated by µVRM, the V_{SS} side is typically tied to a p-type Si substrate through p^+ contacts and necessarily shared among power domains. This makes the ground side of Z_{DD} is almost negligible. On the other hand, Z_{DD} is dominated by the resistance (R) lumped and in series to the V_{DD} side of power rails, which is typically less than 1 Ω which is targeted in design. The capacitance (C) in parallel to power rails works as the shunt impedance for PS current, and it is estimated to be larger than 1 kΩ for the AC components lower than 1 GHz once we assume 1 pF of parasitic capacitance. From these considerations, the dynamic IR-drop voltage waveform (1) purely represents $I_{DD}(t)$ with a frequency independent coefficient, R_{DD}, governed by parasitic resistance in series. Here R_{DD} of 0.25 Ω is assumed in the following part of this paper.

D. Dynamic PS monitoring and analysis principles

The time integral of dynamic IR-drop waveforms provides the amount of consumed charges in a power domain, as Q_{DD} given in (2) and sketched in Figure 2a. The time evolution of $Q_{DD}(t_i)$ in the successive time sections for t_i ($i=0,1,2,..$) reflects the chronological sequences of toggle types among logic cell operations. The length of time section, $t_{i+1} - t_i$, can be chosen as an order larger than the time resolution of OCM waveform capturing.

$$Q_{DD}(t_i) = \frac{1}{R_{DD}} \int_{t_i}^{t_{i+1}} |V_{DD}(t) - V_{CORE}| \, dt \quad (2)$$

Figure 2b shows, based on gate-level simulations of a synchronous digital circuit, where and when net toggles occur. As indicated with three different colors, we distinguish the types of toggles. Immediately after a rising or falling clock edge, we observe toggling in the clock drivers and the clock distribution network. Then, the binary digital data is latched and captured in flip-flops or latches in registers. The third type of toggles originates from the combinational logic cells.

Traditional synchronous digital IC design assumes that the transitions on the clock network all happen instantaneously. Consequently, the spread in time of the toggles in the clock network and the registers is very narrow. We can expect that

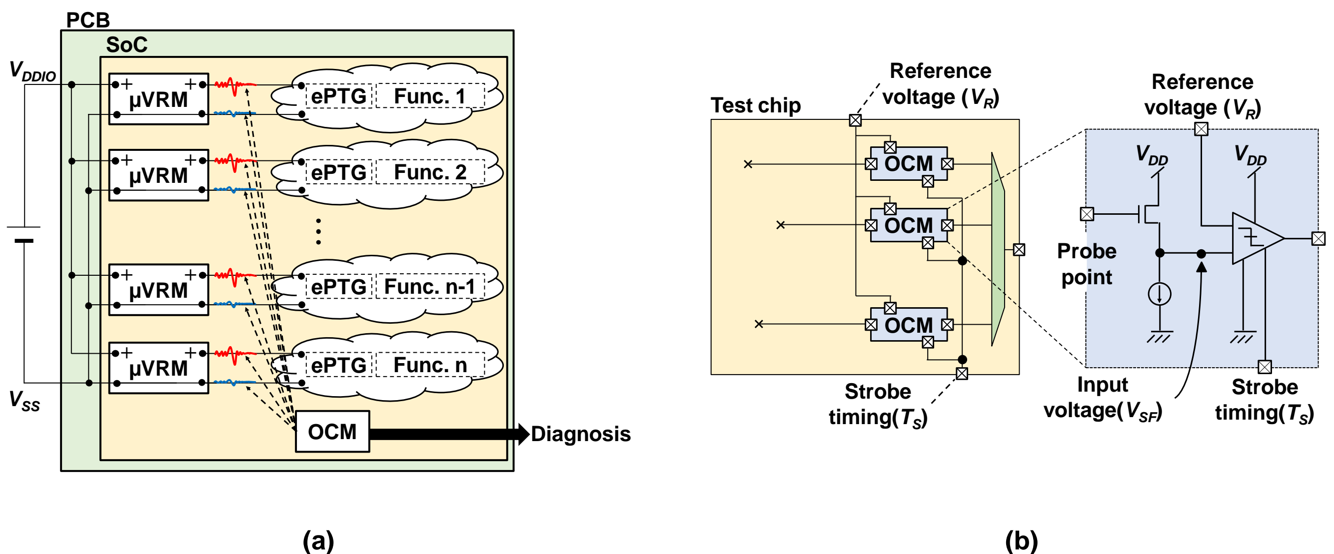


Figure 1 : (a) SoC VLSI chip with multiple power domains includes ePTG and OCM for PS diagnosis[12]., (b) On chip monitor circuits[12].

these two toggle types are almost identical for different test scenarios. A much wider distribution of toggles is observed in combinational logic cells, due to the fact that different logical functions include different numbers of cascaded logic cells on their logic paths. The amount of this (the third) toggle type is strongly dependent on test data embedded in the test patterns.

The charge consumption, $Q_{EST}(t_i)$, is estimated on the basis of the occurrence counts for the three toggle types that we observe in a gate-level logic simulation. We assume that any change in a logic signal is caused by an associated single toggle in the preceding logic library cell, which is approximately represented by a two-input NAND (NAND2) gate. Therefore the number of toggles, #toggles, is counted at the inputs of logic library cells per a power domain. The unit charge Q_{NAND2} consumed in a logic switching operation of a NAND2 cell is determined beforehand through transistor-level simulation. The charge consumption among logic cells is gauaged in the unit of Q_{NAND2} as will be analyzed in Sect.IV.B. Then, #toggles in time interval t_i is multiplied with Q_{NAND2} to derive $Q_{EST}(t_i)$ for time interval t_i, as expressed in Eq. (3):

$$Q_{EST}(t_i) = Q_{NAND2} * \#\text{toggles}(t_i) \tag{3}$$

In the IR-drop-based toggle diagnosis (Figure 2c), the evolution over time of the consumed charge is compared against Q_{DD} by OCM measurements and Q_{EST} by cell-level simulation. The trends of the amount of charge in response to time and test scenarios confirm the certainty of operation in a digital circuit that will not produce any digital output. The significant difference between Q_{DD} and Q_{EST} should be considered as a warning for either (1) faulty behavior in the IC hardware, or (2) bugs in the test program. This warning should then be followed up by additional in-depth diagnosis to identify the root cause of the problem.

A particular example is assumed as in Figure 2c for the test scenario of #3, where Q_{DD} deviates from Q_{EST}. We might find some mistakes in the test scenario, or in the implementation of digital circuits. We will see the practicality of the proposed technique through silicon measurements in the next section.

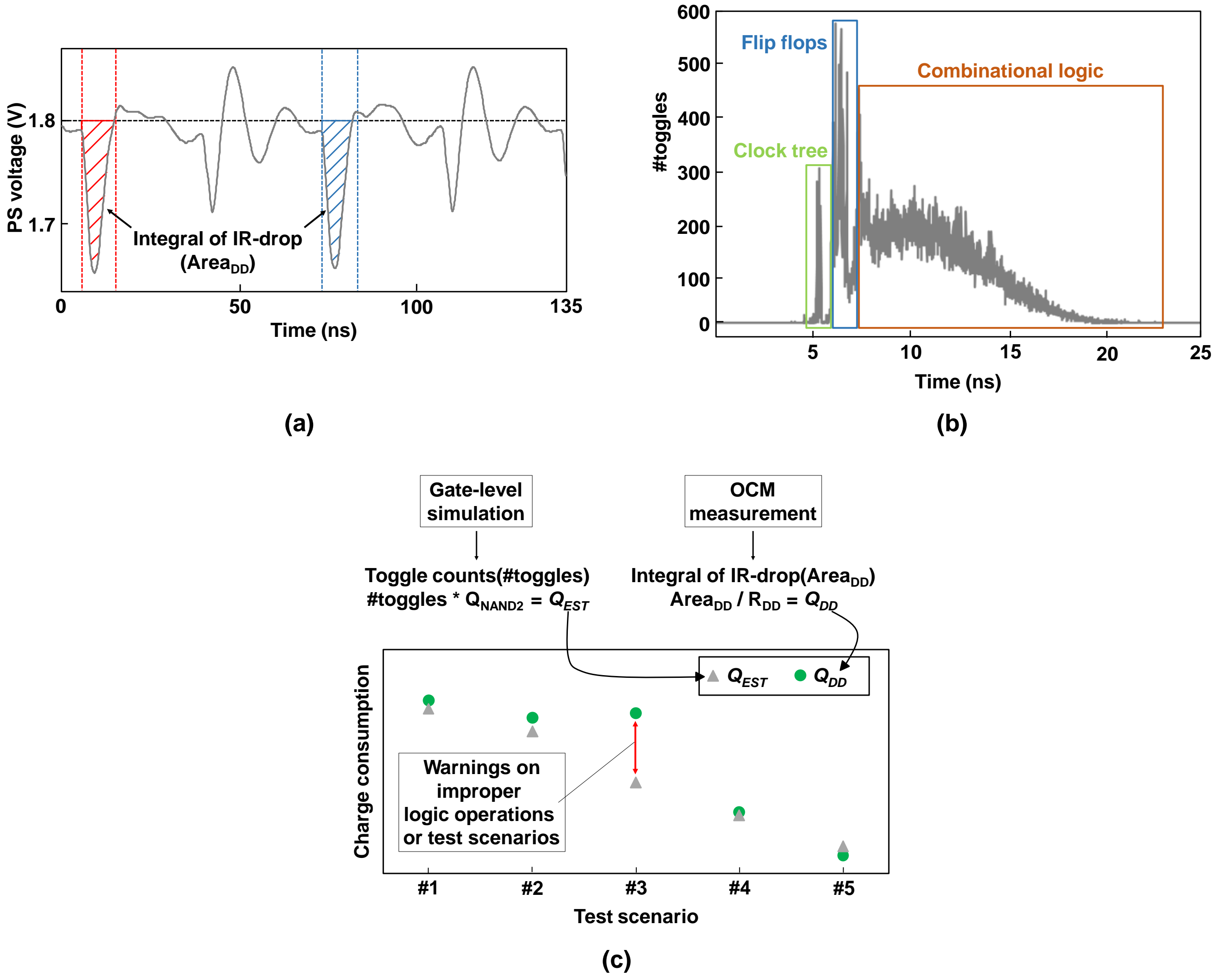


Figure 2 : (a) Time integral of dynamic IR-drop waveforms by on-chip measurements[12].,
(b) Three toggle types in one clock period[12].,
(c) Dynamic IR-drop-based PS diagnosis flow comparing gate-level simulation and on-chip measurements.

III. Silicon Prototype

A. Test chip design

A test chip was designed and fabricated in a commercially available 0.18 µm CMOS technology. The chip embeds three digital blocks (referred to as A, B, and C) and an OCM system, as shown in Figure 3a and 3b. Each digital block functions for cryptographic operations based on the advanced encryption standard, AES. The size of A, B and C, individually including an ePTG, is 73.1 KGE, 75.6 KGE and 75.7 KGE, respectively. The entire test chip runs on a single power domain, directly supplied by an external power source. The three digital blocks are full-scan designs equipped with IEEE Std 1500^{TM}-2005 [11] core test wrappers, allowing them to be tested as independent modules with common clock distribution and power delivery networks.

The OCM system is isolated from the digital blocks for clocking and power delivery. The OCM channels connect to the pairs of V_{DD} and V_{SS} nodes at proximate points within the digital blocks. One of the OCM channels in the core is digitally selected for capturing waveforms. In this paper, dynamic PS waveforms are captured by the OCM with the resolution of 100 ps and 100 µV.

B. Demonstrator system setup

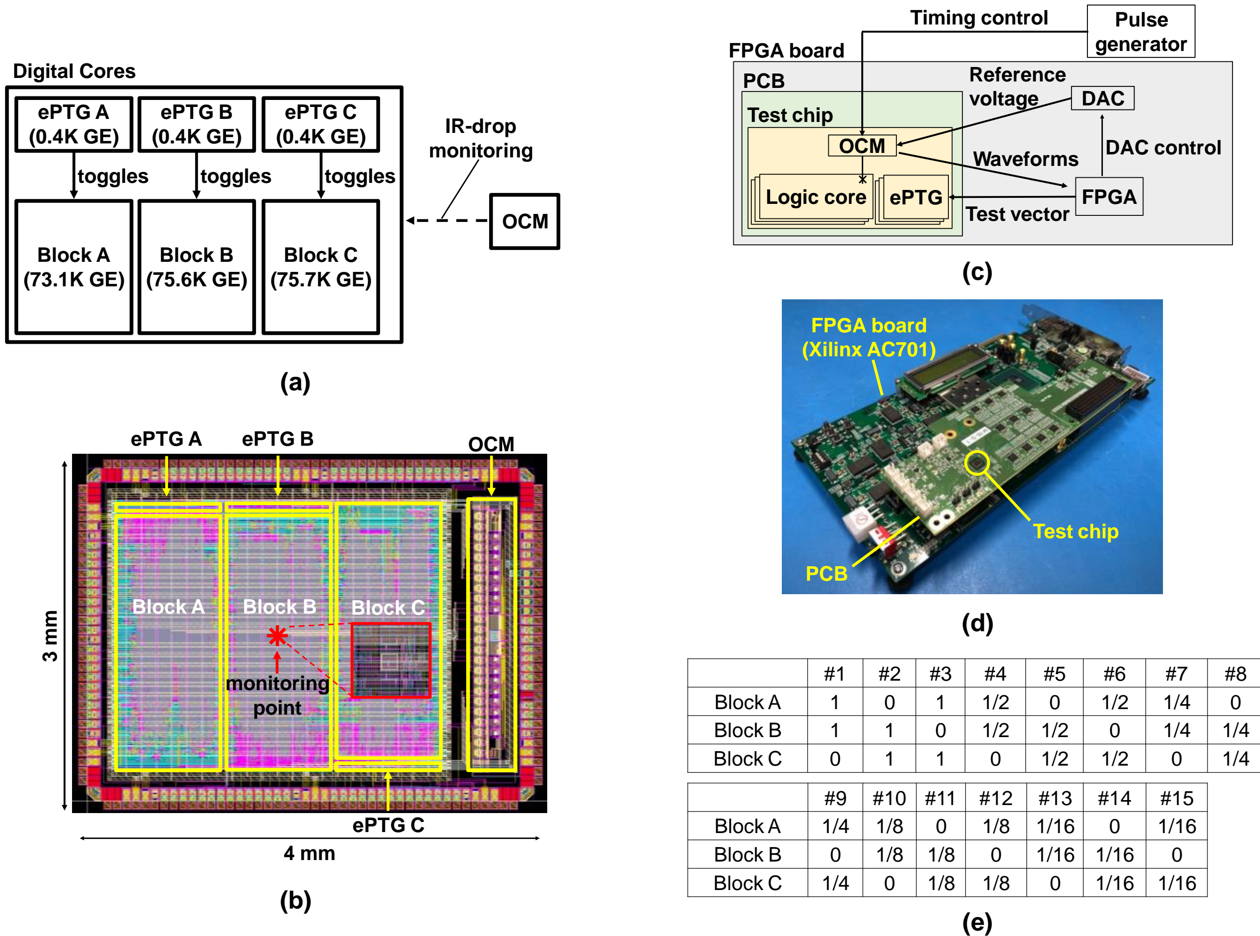
The test chip is packaged in a ball grid array, assembled on a custom printed circuit board (PCB), and integrated with a field programmable gate array (FPGA) commercial board (Xilinx AC701). A demonstrator system of Figure 3c and 3d is then built with a controller PC. The various test scenarios are programmed on the PC, partially stored in the FPGA board and loaded to the chip through an I/F block. An external pulse generator produces the system clock to the FPGA as well as to the test chip. The whole system is autonomously controlled by the PC to operate digital circuits and to capture dynamic IR-drop waveforms.

The test scenarios for three digital blocks are designed with intentionally different levels of internal logic activities as listed in Figure 3e. There are 15 test scenarios in which the three digital cores load toggle data from their private ePTG in one of two modes of 0 and 1/X (seeTab.1.) Here, the digital block in Mode 0 means to become MUT where ePTG does not demand toggling; while those in Mode 1/X (X=1, 2, 4, 8, 16) are 'neighbor' module where ePTGs create stimuli to force the block to toggle at every X clock cycles.

IV. Results

A. Measurement results

A set of on-chip V_{DD} waveforms are captured by OCM at the position of a monitoring point in Figure 3b with all the test scenarios. Power currents are shared and summed among the cores, flow through the power trunk wiring and create the IR



	#1	#2	#3	#4	#5	#6	#7	#8
Block A	1	0	1	1/2	0	1/2	1/4	0
Block B	1	1	0	1/2	1/2	0	1/4	1/4
Block C	0	1	1	0	1/2	1/2	0	1/4

	#9	#10	#11	#12	#13	#14	#15
Block A	1/4	1/8	0	1/8	1/16	0	1/16
Block B	0	1/8	1/8	0	1/16	1/16	0
Block C	1/4	0	1/8	1/8	0	1/16	1/16

(e)

Figure 3 : (a) Modules in the test chip., (b) Layout of the test chip.
(c) Block diagram showing the design hierarchy [12]., (d) Photo of the test system. [12], (e) Test scenarios.

drop, which is represented by the V_{DD} voltage on this position. The waveform is observed typically as in Figure 2a.

The amount of charges, Q_{DD} and Q_{EST}, derived from on-chip measurements and estimated by gate-level simulation, respectively, are compared to the designed test scenarios (Figure 3e), as shown in Figure 4a. We sampled two chips (chip α and chip β) in each test scenario to confirm the consistency of results among devices. The trends generally agree with each other in the wide range of digital activities.

The toggle types defined in the clock network and registers are estimated for their switching activity by simulation, as plotted in the respective curves in Figure 4a. Clearly, they contribute only to a small fraction of the total toggling in the core, and as predicted in Section II.D, keep almost constant among the different test scenarios.

The Q_{DD} and Q_{EST} are resolved and compared for the nominal and varied supply voltage in Figure 4b, showing that the features among chips are nicely consistent. The slopes of Q_{DD} and Q_{EST} are almost fixed for the wide range of digital activities. The slopes in chip α and chip β are resolved to be approximately 17.1 fC/gate and 19.0 fC/gate respectively. The sensitivity of the slopes against the variation of V_{CORE} (+10% and -10% from 1.8 V) is also evaluated, properly reflecting the proportional increase or decrease of power consumption current against the power supply voltage.

B. Evaluation

The amount of charge consumption in a 2-input NAND, Q_{NAND2}, is estimated to be 33 fC by transistor-level simulation with the transistor parameters of a typical process, power voltage and temperature (PVT) condition, as in Figure 4c and 4d. In comparison, the slope of Q_{DD} and Q_{EST} against the number of toggles in Figure 4b, which were repeatedly measured for the chip α and chip β, is almost 1/2 of the Q_{NAND2}. This leads to the assumption that the proposed charge-based diagnosis achieves the resolution of a single two-input NAND gate.

The influence of transistor property variations on the diagnosis is evaluated with transistor-level simulation with standard PVT model parameters. The waveforms of a $I_{DD}(t)$ by ePTG-A (in Figure 3a) are simulated with three process corner models (SS, TT and FF) and exhibit the dependency, as shown in Figure 5a, where the voltage and temperature conditions remain typical. The Q_{DD} are resolved and plotted in Figure 5b (upper) among three time periods of different clock cycles (T1, T2 and T3 in Figure 5a). Further comparisons are made in Figure 5b (middle) and Figure 5b (bottom) additionally with the voltage and temperature variations. Based on these results, voltage and temperature variation have a bigger impact on the size of charge consumption than process corner variation. However, since those fluctuations are not sudden, we can limit their impact on the accuracy of dynamic IR-drop-based PS diagnosis by periodic calibration.

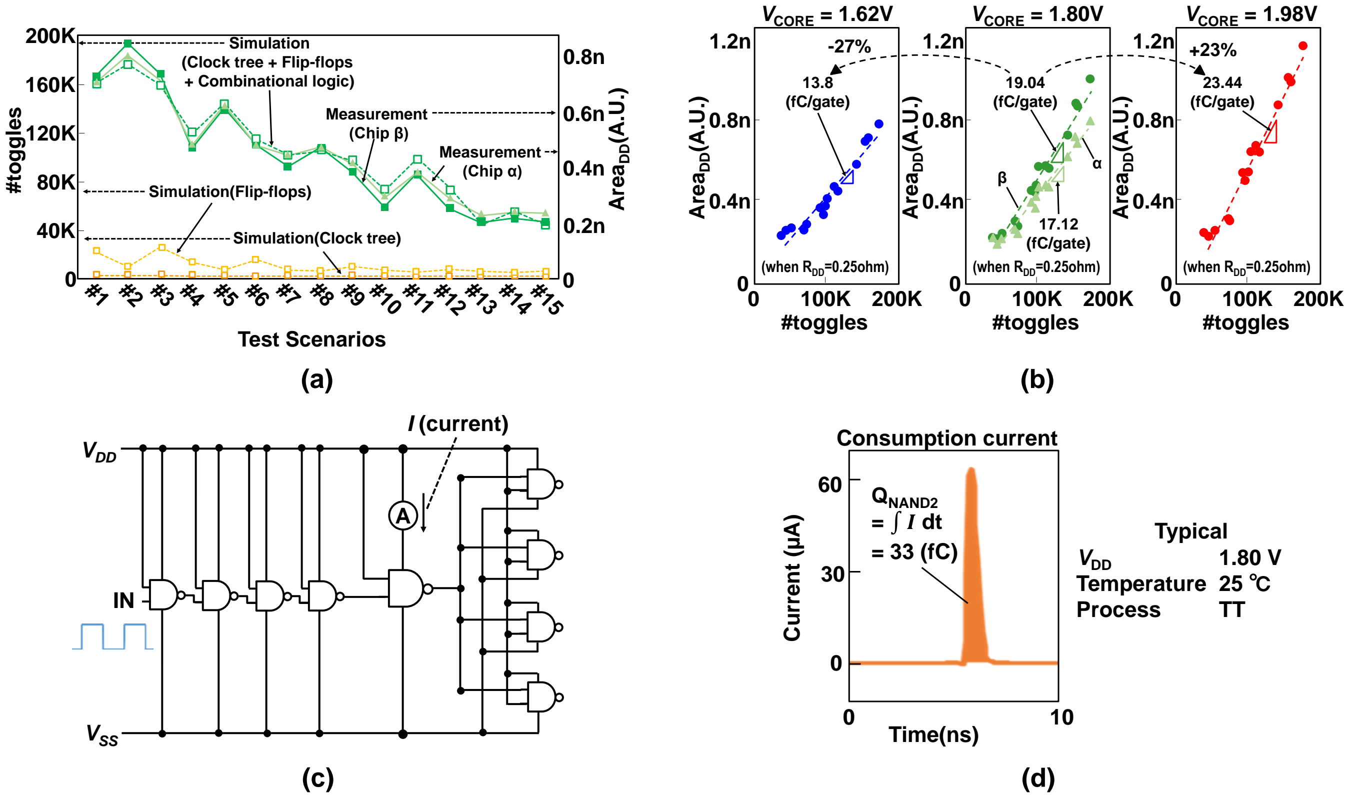


Figure 4 : (a) Comparison of $Area_{DD}$(A.U.) ($\propto Q_{DD}$ measurement) and #toggles ($\propto Q_{EST}$ simulation) among test scenarios.,

(b) Comparison of $\#Area_{DD}$(A.U.) ($\propto Q_{DD}$ measurement) and #toggles ($\propto Q_{EST}$ simulation) with variation of V_{CORE} voltage.,

(c) Evaluated circuit to derive Q_{NAND2}.,

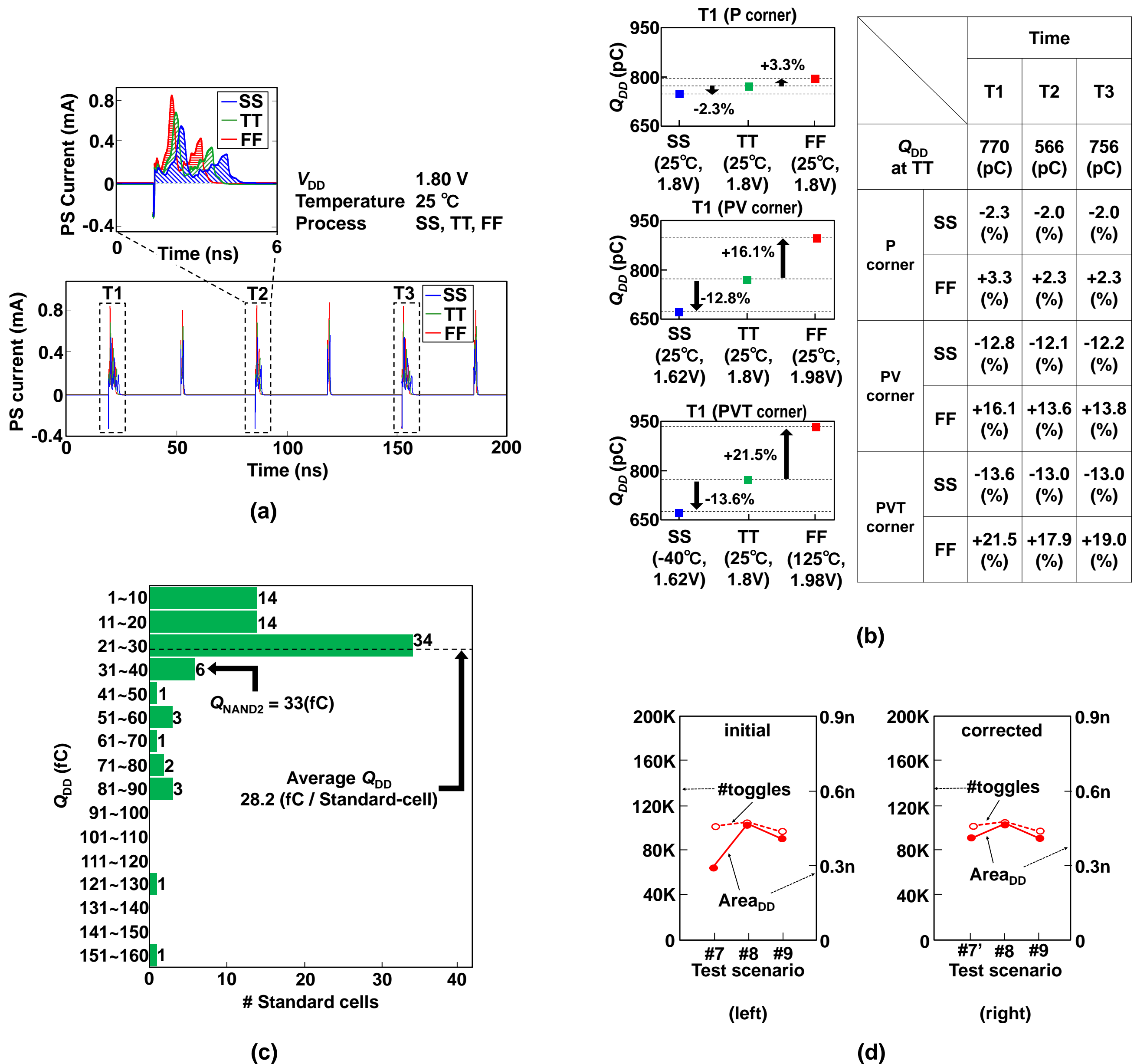
(d) Consumption current waveform of Q_{NAND2} with typical PVT condition.

The Q_{DD} of standard cells in ePTG-A are evaluated one by one and compared in Figure 5c. The size of charge consumption per one cell is different for different cells. The differences are mainly brought by the number of transistor fingers in a cell and associated load-capacitance. This result shows that the size of some cells' Q_{DD} is 4 times or 5 times as large as the Q_{NAND2}. On the other hand, the number of standard-cells which have such large charge consumption is very small and Q_{DD} of most of the cells are almost same as Q_{NAND2}. From these results and consideration, we conclude that the Q_{NAND2} can be a standard size of charge consumption.

C. *Example of diagnosis*

A large discrepancy was initially found for the test scenario of "#7" through the on-chip IR-drop-based PS diagnosis, as in Figure 5d (left). This in fact came from the wrong setup of ATPG for ePTG for "#7." The test scenario of "#7'" was updated and then diagnosed again as in Figure 5d (right). We now confirm the proper correction of ATPG setup by comparing Q_{EST} and Q_{DD}.

Without the diagnosis, the ePTG might create the smaller IR drop and optimistically lead to wrong responses by other circuits. It is noted here that the difference in trends among test scenarios is more sensitive and apparent to the wrong or unintentional conditions given to the digital circuits without digital outputs.



		Time		
		T1	T2	T3
Q_{DD} at TT		770 (pC)	566 (pC)	756 (pC)
P corner	SS	-2.3 (%)	-2.0 (%)	-2.0 (%)
	FF	+3.3 (%)	+2.3 (%)	+2.3 (%)
PV corner	SS	-12.8 (%)	-12.1 (%)	-12.2 (%)
	FF	+16.1 (%)	+13.6 (%)	+13.8 (%)
PVT corner	SS	-13.6 (%)	-13.0 (%)	-13.0 (%)
	FF	+21.5 (%)	+17.9 (%)	+19.0 (%)

Figure 5 : (a) PS current waveforms by simulation with process corner model.,
(b) Sensitivity to PVT corners calculated from simulation waveforms.,
(c) Histogram of Q_{DD} among standard cells in ePTG-A.,
(d) On-chip IR-drop-based PS diagnosis, (left) with initial set of ePTG test vectors,
(right) with corrected set of ePTG test vectors.

V. CONCLUSION

We have experimentally demonstrated a dynamic IR-drop-based PS scenario-based testing and in-field diagnosis technique with 0.18 μm CMOS test chips that embed digital functions of cryptography and ePTG cores. The on-chip monitored PS voltage waveforms finely capture the time evolution of gate toggles in chronologic sequences of a synchronous digital system. The amount of charges consumed in a power domain is estimated from the time integral of on-chip and in-field captured waveforms, which algorithm can be realized by an analyzer following to OCM. The toggle type is almost equivalently resolved in the unit of a single two-input NAND gate. The deviation in the amount of charges from the reference either by a golden sample or even by simulation warns for potential errors under a test scenario given to MUT. This helps to diagnose those circuits which intentionally create toggles or consume power, while not producing any signal output, in the background of primary circuits to equalize, flatten or stabilize power delivery. It also finds inconsistent toggles that can be related with design faults and unintentional insertion of logic circuits like hardware Trojans.

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REFERENCES

[1] Yervant Zorian et al., 'Testing Embedded-Core Based System Chips', IEEE International Test Conference (ITC1998), Washington, D.C, October 1998, pp. 130-143, DOI 10.1109/TEST.1998.743146

[2] L.Katselas et al., 'On-Chip Toggle Generators to Provide Realistic Conditions during Test of Digital 2D-SoCs and 3D-SICs', IEEE International Test Conference (ITC'18), Oct. 2018, doi: 10.1109/TEST.2018.8624803

[3] E.J. Marinissen and S. Deutsch, "Controlled toggle rate of non-test signals during modular scan testing of an integrated circuit," Dec. 16 2014, US Patent 8,914,689. [Online]. Available: https://www.google.com/patents/US8914689

[4] Y.Komatsu et al., "A 0.25–27-Gb/s PAM4/NRZ Transceiver With Adaptive Power CDR and Jitter Analysis," in IEEE Journal of Solid-State Circuits, vol. 54, no. 10, pp. 2802-2811, Oct. 2019, doi: 10.1109/JSSC.2019.2920082.

[5] C.Wang et al., "Power Profile Equalizer: A Lightweight Countermeasure against Side-Channel Attack," 2017 IEEE International Conference on Computer Design (ICCD), Boston, MA, 2017, pp. 305-312, doi: 10.1109/ICCD.2017.54

[6] H.Esmaeilzadeh et al.,"Dark silicon and the end of multicore scaling," 2011 38th Annual International Symposium on Computer Architecture (ISCA), San Jose, CA, 2011, pp. 365-376.

[7] J. Saxena et al., "A case study of ir-drop in structured at-speed testing," International Test Conference, 2003. Proceedings. ITC 2003., 2003, pp. 1098-1104, doi: 10.1109/TEST.2003.1271098.

[8] Z. Abuhamdeh et al.,"Characterize Predicted vs Actual IR Drop in a Chip Using Scan Clocks," 2006 IEEE International Test Conference, 2006, pp. 1-8, doi: 10.1109/TEST.2006.297656.

[9] Y.Lechuga et al.,"Built-in dynamic current sensor for hard-to-detect faults in mixed-signal ICs," Proceedings 2002 Design, Automation and Test in Europe Conference and Exhibition, Paris, France, 2002, pp. 205-211, doi: 10.1109/DATE.2002.998271.

[10] M.Nagata et al., "A built-in technique for probing power supply and ground noise distribution within large-scale digital integrated circuits," in IEEE Journal of Solid-State Circuits, vol. 40, no. 4, pp. 813-819, April 2005, doi: 10.1109/JSSC.2005.845559.

[11] IEEE Std 1500 Working Group, 'IEEE Standard Testability Method for Embedded Core-based Integrated Circuits', IEEE Std 1500-2005, published August 29, 2005, DOI 10.1109/IEEESTD.2005.96465

[12] K.Monta et al., "Testing Embedded Toggle Pattern Generation Through On-Chip IR Drop Monitoring," 2021 IEEE European Test Symposium (ETS), 2021, pp. 1-4, doi: 10.1109/ETS50041.2021.9465391.

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