Logic via printability enhancement using restricted via placement and exhaustive SRAF placement on a staggered grid

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ABSTRACT

In order to improve logic via printing we propose staggered vias to effectively regularize randomly placed vias in a typical logic design. We accomplish this (i) by forcing via placement on a staggered sub-grid of the standard manhattan grid and (ii) by placing smaller fixed-size via Sub-Resolution Assist Features (SRAFs) on all remaining empty positions of the staggered grid. We devised a methodology to create such staggered via placement in a standard Place&Route (PNR) design flow and evaluated the concept on a 64-bit (64b) ARM core implementation through a Power-Performance-Area (PPA) analysis. From a PNR run-time perspective and PPA analysis this looked a very viable implementation with little to no disadvantages compared to standard via placement. Finally, to experimentally test and compare staggered vias and against standard manhattan vias, we designed a via mask with both staggered and standard manhattan vias patterns and exposed them on an 0.33NA NXE3400 EUV lithography system. Analysis of experimental results on a 38nm via pitch show 40% smaller best-focus shift across the slit, and 20% smaller via-via CD variation for staggered vias compared to Manhattan vias with regular SMO.

Keywords: OPC, SRAF, homogenized, regularized, logic vias

1. INTRODUCTION, EXPECTATIONS, SIMULATIONS

Logic vias are inherently irregular and therefore print less well than regular holes, especially near the resolution limit of the lithographic system[1]. The central idea of this study is to increase printability of logic vias by regularizing them, as shown in Figure 1 by (i) forcing via placement on a staggered grid and (ii) placing fixed-size via SRAFs on all remaining empty positions of the staggered grid.

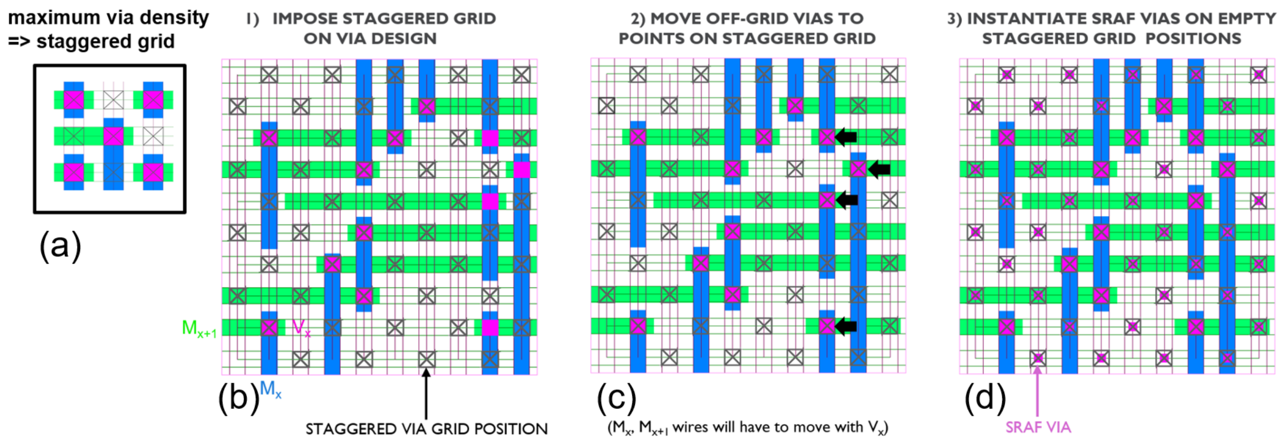
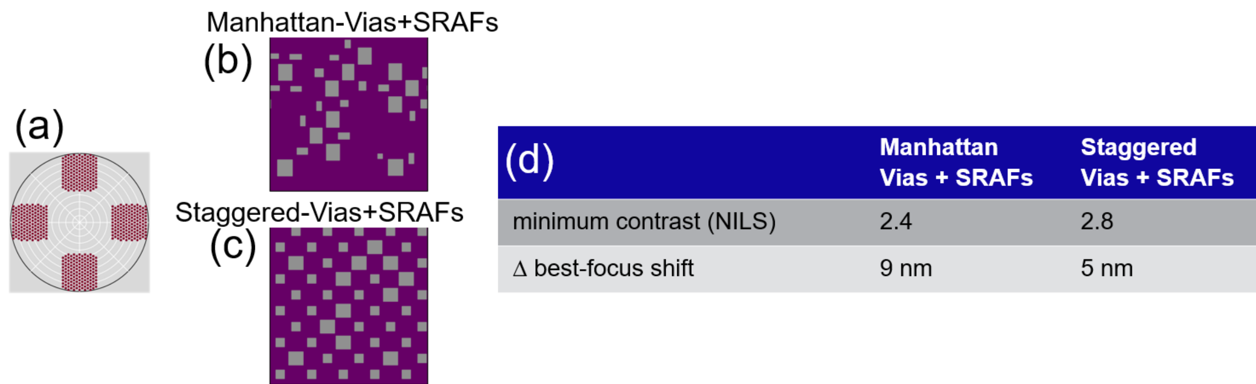


Figure 1 (a) based on standard design rules, assumed densest possible via construct (b) sample of standard manhattan via placement, (b) imposing staggered grid on the manhattan-routed sample, necessitating changes in vias and routes (c)

addition of via SRAF on all empty positions on the staggered grid

The fact that gridded logic via design is immersed in a grid of via SRAFs, simplifies the optical spectra, which is important to EUV lithography, as Mask-3D (M3D) effects introduce large pitch-dependent best-focus (BF) shifts, which can be particularly important in randomly placed vias in logic. Based on some small design samples, we did simulation with a single pupil, showing 16% larger contrast and 49% smaller BF shift (Fig. 2)



(d)	Manhattan Vias + SRAFs	Staggered Vias + SRAFs
minimum contrast (NILS)	2.4	2.8
Δ best-focus shift	9 nm	5 nm

Figure 2. Early simulation results obtained with (a) single pupil, (b) for manhattan vias and SRAFs, (c) staggered vias and SRAFs, as well as (d) simulation results listed in a table.

2. DESIGN IMPLEMENTATION & PPA ANALYSIS

The next question is how to implement such staggered via placement in a real design flow: in a standard PNR methodology all via grid positions on the standard manhattan grid are enabled for via placement, and minimum via-to-via distance is enforced through routing rules. In order to impose via placement on the staggered (sub-)grid of the manhattan grid, we chose a blockage-based solution as shown in Figure 3, superimposing via blockage shapes on all standard manhattan grid positions that are off the intended staggered grid, while relaxing the via-via minimum distance, allowing via placement only on the remaining open positions on the staggered sub-grid.

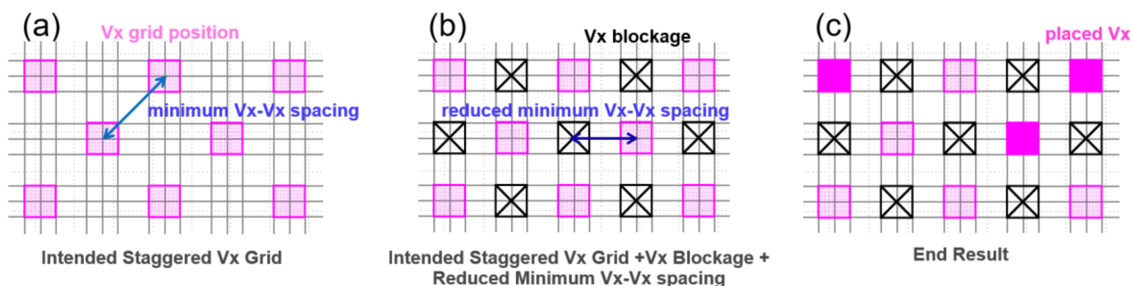


Figure 3. Implementation of staggered via placement in PNR (a) simple manhattan grid spanned by routing levels, intended staggered Vx via positions indicated in pink (b) instantiation of blockage (black) via shapes on the unintended grid positions, and reducing the minimum via-via distance for via placement (c) the end result with placed vias indicated in solid pink.

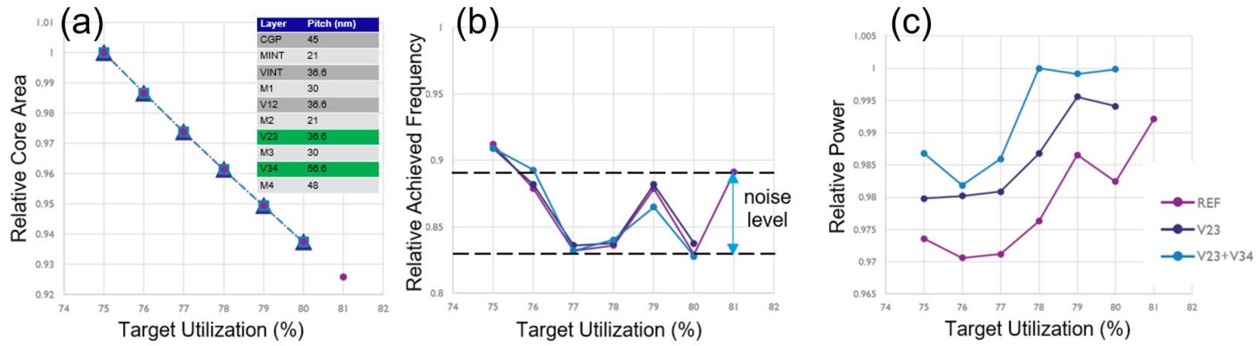


Figure 4. Results of the PPA analysis of the 64b ARM core (a) relative core area does not dramatically change between the via placement options, inset showing the metal and via pitches in the IMEC iN5 technology (b) achieved frequency does not significantly change between the via placement options (c) a roughly 1% power increase is observed as one restricts via placement by staggered vias

Based on the pitches in the IMEC iN5 technology (inset in Fig 4a), we selected 2 via levels, the V23 via level (between the M2 and M3 wire levels), and the V34 via level (between the M3 and M4 wire levels) as candidates for this restricted staggered grid. A PNR implementation 64-bit ARM core was generated in the IMEC iN5 technology for both the standard manhattan via design and the staggered via design, to test the workability of our solution and assess the impact on the overall design through a Power-Performance-Area (PPA) analysis. The design was run in 3 modes: (i) without via grid restrictions (manhattan vias) for all via levels, (ii) imposing a staggered via grid for V23 vias, and (iii) imposing a staggered grid for both V23 and V34 vias. While a modest increase in run-time was observed (which probably could be improved upon), from the PPA analysis we see that the design is not structurally altered imposing staggered vias (Fig. 4a), and observe negligeable impact on performance (Fig. 4b) and a very small (~1%) impact on power (Fig. 4c).
The surprisingly small impact of staggered vias can be understood by realizing that, although 50% of the potential via placement sites are eliminated by imposing a staggered grid, the maximum via density is not reduced as the staggered grid is compatible with the densest via configuration possible commonly allowed by the design rules (Fig. 1a).

3. LITHOGRAPHIC EXPERIMENT AND ANALYSIS

In order to experimentally check the lithographic performance, we used a TaBN absorber-based EUV mask with V23 patterns from the PNR implementation of the 64b ARM core, for the 2 via placement types: (i) for standard (unrestricted) manhattan vias, and (ii) for (restricted) staggered vias. From both via design implementations we selected small areas of around 2umx2um for printing with similar densities. Although the 2 versions of the complete ARM core correspond in term of functionality, due to the randomness of PNR, these selected areas are likely to correspond to different underlying circuits. The patterns were subsequently modified to cover a range of via pitches from 44nm down to 36nm.
Computational lithography was done in 2 ways:
(i) for the standard manhattan-grid design, we used a standard computational lithography flow from ASML Brion (SMO and uncalibrated OPC model) creating un-gridded SRAFs, and generating its own optimal pupil.
(ii) for the restricted, staggered via design we used a single target via size and a single SRAF size (chosen to avoid SRAF printing), for source optimization an internal ASML tool was used to generate an optimal pupil for dense via arrangement. No OPC was done on the staggered via design.

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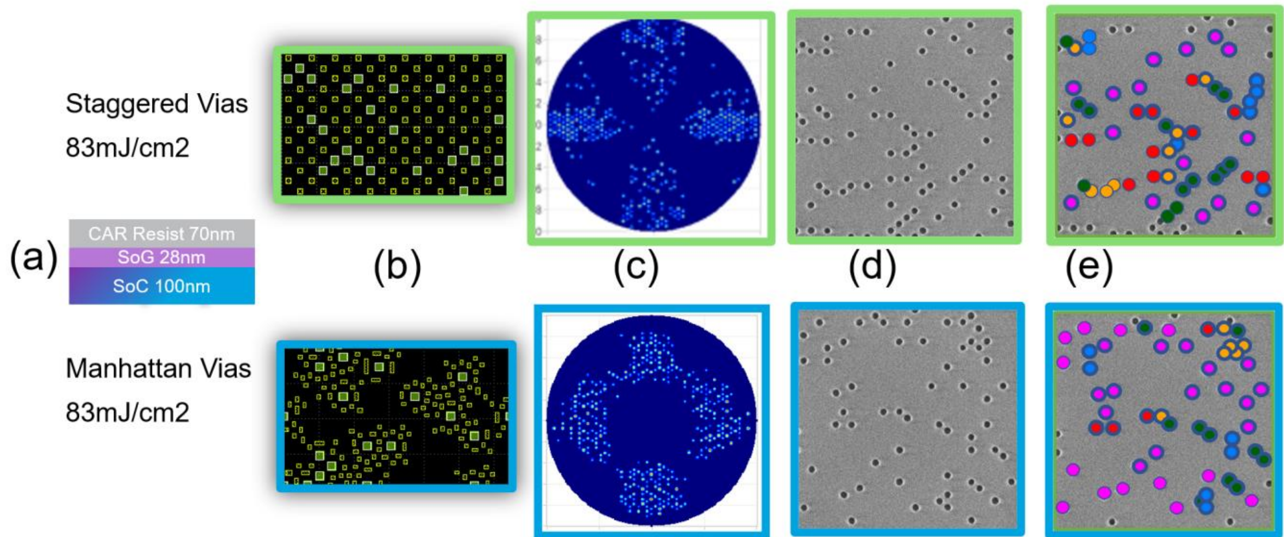

Figure 5. (a) the resist layer stack that was used; comparison between several aspects for the staggered vs manhattan experiment: (b) the physical layout design of the vias, (c) the custom optimized source, (d) CD-SEM image of the exposed vias, (e) color coded categorization of the vias depending on their relative nearest neighbor environment.

Using their respective optimal pupil derived from the source optimization, the manhattan and staggered via mask designs were exposed on an ASML NXE3400 EUV scanner with CAR resist (Fig. 5); based on a printability check with a generic pupil a via pitch of 38nm was selected for further exposures. For each via solution a random Focus Exposure Matrix (rFEM) wafer and CD Uniformity (CDU) wafer were exposed. The selection of best focus for the CDU wafer was based on a CD peak through focus criterion. The CD-SEM measurements were done with a Hitachi CD-SEM 6300, with off-line custom image processing. Based on a spatial frequency analysis[1], the vias were classified in 5 clusters, and within the patterns areas with similar distributions were selected for further analysis (Fig. 5e). On the CD-SEM we primarily used a scan in the x-direction for the first set of measurements, making the measurements in the y direction less accurate; for a second set of CD-SEM measurements, we used a special x/y to get equal accuracy in both the x and the y directions.

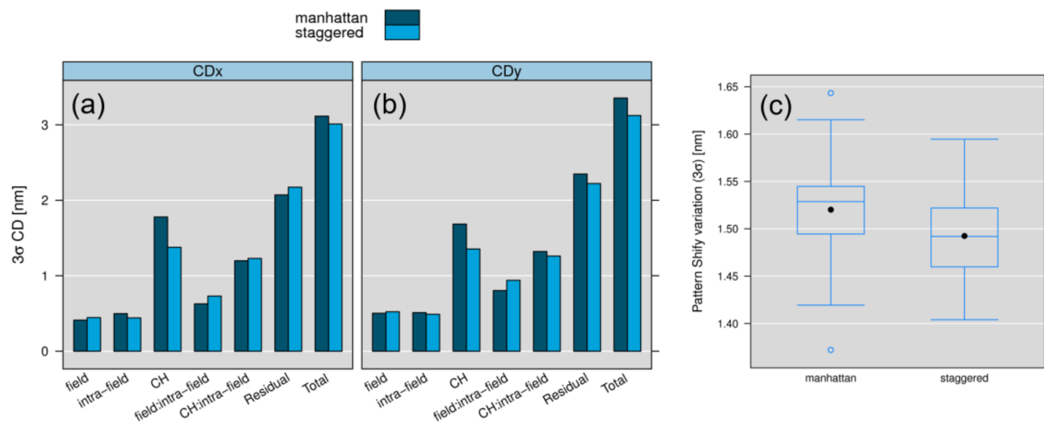

Figure 6. results of an ANOVA analysis of the CDU wafer data, (a) showing CDx, (b) CDy, (c) shows the pattern shift from the CDU wafer data.

On the CDU wafer data we performed an Analysis of Variance (ANOVA)[1] of CDx and CDy for manhattan and staggered vias. This was done using field, intra-field (slit) and CH (via) as independent statistical variables, as well as first-order interactions between them, so that model residuals represent stochastic and measurement effects (Fig. 6a and

6b). From this ANOVA analysis, the 3σ standard deviation of CDx and CDy for CH (showing the similarity in CD between vias) is more than 20% smaller for staggered vias than for manhattan vias. In the residuals of 3σ CD we observe that staggered and manhattan vias behave differently, for CDx and CDy. An investigation of the positional variation of vias, shown in Figure 6c, shows that there is no significant difference between positioning accuracy of manhattan and staggered vias.

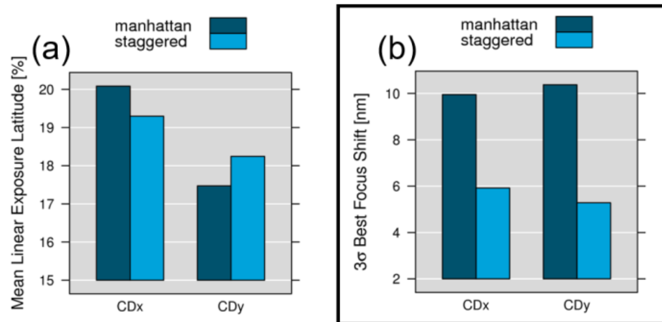

Figure 7. From the rFEM wafer data: (a) mean of the exposure latitude for CDx and CDy between manhattan and staggered vias, and (b) 3σ of the exposure latitude for CDx and CDy for manhattan and staggered vias.

Finally, we looked at the rFEM data to investigate the exposure latitude (EL) and the BF shift (Fig. 7). For EL, we see opposite trends for CDx and CDy, with staggered have slightly worse EL for CDx and slightly better EL for CDy; this explains the same observed behavior in the residuals of the decomposed 3σ CD. The big difference, both for CDx and CDy, is a drop of 40% in BF shift for staggered vias compared to manhattan vias, as expected from our simulations. Finally, as a sanity check, we did some more CD-SEM measurements using the special x/y scan, which were subsequently processed with Brion MXP software; these measurements show 3σ CD variation between manhattan and staggered vias in the CDx and CDy, consistent with the measurements obtained with the CD-SEM, which were done scanning in the x-direction (Fig.8).

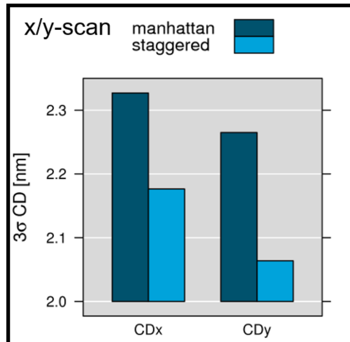

Figure 8. From the CDU wafer data: comparison between staggered and manhattan vias for 3σ of CDx and CDy; x and y data measured on CDU wafer measured with the CD-SEM using a special x/y-recipe. (3σ CD values are smaller than in Figure 6, because the number of measurements is larger and averaging was performed).

4. CONCLUSIONS

We demonstrated a way to regularize random vias in logic, by (i) restricting their placement on a staggered grid and (ii) exhaustive placement of via SRAFs on the empty positions of this staggered grid. We showed a simple way to implement staggered vias in a slightly modified standard PNR flow on a 64-bit ARM core in IMEC iN5 technology, with negligible or small impact on power, performance and area of the core and run-time of PNR. From the lithographic experiment we conclude that expected lithographic benefits materialize in the experiment:

20% smaller via-via CD variation and 40% smaller BF shift for staggered vias compared to manhattan vias. Additionally, we see the potential for a simpler, faster OPC, a likely reduction in the risk of occurrence of lithographic hot spots. Finally we expect a positive impact on mask making, due to smaller variety in via and SRAF sizes on the mask, leading to tighter distribution of mask errors. OPC and effects on mask making are areas for future exploration.

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