Monte Carlo analysis of p-type $Si_{0.75}Ge_{0.25}$-channel nanosheet performance

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***Abstract*— The performance of $Si_{0.75}Ge_{0.25}$-channel p-type nanosheet devices with a gate length of 14 nm and a sheet width of 12 nm is investigated by Monte Carlo device simulation. It is found that the stress in the Si–Ge channel can eliminate the performance imbalance with n-type nanosheets arising from the (001) surface in the absence of stress. The performance is the same as the theoretical performance of Si-channel p-type nanosheets with $Si_{0.5}Ge_{0.5}$ source/drain pockets under the ideal assumption that no stress relaxation e.g. due to grain boundaries from merging epitaxial growth occurs for the Si-channel devices. It is shown that the performance levels can be related to stress–induced quasi–ballistic velocity overshoot and the impact of alloy scattering. This is not captured by standard drift–diffusion simulation where a smaller saturation velocity predicts a performance degradation for Si–Ge channel devices.**

***Index Terms*— Monte Carlo, Si–Ge, nanosheet, alloy scattering**

I. Introduction

In order to further increase the drive current per footprint, FinFETs are being replaced by devices with stacked sheets of tunable width such as nanosheet (NS) devices [1], [2] and forksheets [3].

One challenge associated with these new device types is the effectiveness of source/drain (S/D) stressors for p-type devices. The traditional approach for stress engineering consists of embedding silicon–germanium (Si–Ge) pockets in the S/D regions where the lattice–mismatch to the Si substrate leads to uniaxial compressive stress in the channel. This strongly increases the hole mobility in the $\langle 110 \rangle$ channel direction.

However, crystal defects at the sidewalls of the Si–Ge pockets can increase the access resistance and impair the device performance in spite of a high stress–induced channel mobility. This was already observed for planar bulk pMOSFETs [4] and might become a more serious problem for NS devices with high S/D Ge–contents in view of the scaled device dimensions. On the other hand, the creation and maintenance of a high compressive channel stress by embedded Si–Ge S/D pockets could also be problematic in NS devices, since merging of epitaxial growth from the substrate and the different NS channels can lead to a complete stress loss [5]. The importance of stress is even larger for nanosheets since the dominant surface is in contrast to the (110) sidewall of FinFETs in the (001) wafer direction which is unfavorable for holes and can lead to a performance imbalance with nFETs.

This raises the question if other stressors can be effective for NS performance improvements. One possibility is to use Si–Ge as channel material where compressive stress originates from lattice–mismatch to a Si substrate. Compressively strained Si–Ge as channel material has been used for FDSOI devices [6]. Challenges for nanosheets concern the selectivity for etching the sacrificial SiGe layers with a different Ge–content than the target SiGe channel in the multi–layer stack as well as the surface quality of the interface between the SiGe channel and the interfacial oxide in the gate stack. As far as self–heating affects performance this effect will become stronger for a SiGe channel due to its lower thermal conductivity. However, these potential problems for SiGe as a channel material can be overcome since, recently, it has also been demonstrated for stacked nanosheets and performance improvement with respect to Si-channel control devices was measured [7].

It is the purpose of this work to explore by device simulation the performance of p-type Si–Ge channel (cSiGe) nanosheets at a future technology node featuring a gate length of L_G=14 nm. Note that cSiGe performance depends both on the predictable stress–induced mobility increase and the surface quality with unknown dependence on the Ge–content. Therefore the focus of this work is the comparison of a cSiGe–NS with a fixed realistic Ge–content of 0.25 to a standard Si-channel (cSi) NS.

This task requires a microscopic transport model since the on–current (ION) at these short L_G is determined by quasi–ballistic velocity overshoot. Corresponding Monte Carlo (MC) [8]–[10] and nonequilibrium Green's function (NEGF) [11]–[13] simulations were restricted to n-type nanosheets. P-type nanosheets were only investigated in [14] and, for the same access resistance and doping profiles, found to involve about 35 % lower performance than pFinFETs. Here, we extend this work and find that $Si_{0.75}Ge_{0.25}$-channel nanosheets can achieve the same performance as their n-type cSi counterparts. Together with their potentially more stable stress configuration this makes them an attractive contender for future technology nodes.

II. Simulation approach

Fig. 1 shows the NS device which is investigated by MC

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Manuscript received month xx, 2022.

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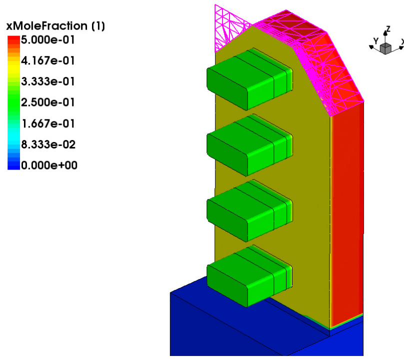

Fig. 1. Geometry and Ge-content of a p-type nanosheet with four sheets. The distance between sheets is 10 nm and the S/D regions are contacted from above. The contacted poly pitch (CPP) is 42 nm and the spacer width is 5 nm. The channel orientation is in $\langle 110 \rangle$ direction.

simulation [15] in this work. It corresponds to the NS of [14] with dimensions scaled to the next technology node. This involves smaller values for L_G (14 nm vs. 15 nm), sheet width (12 nm vs. 16 nm), CPP (42 nm vs. 45 nm), spacer width (5 nm vs. 8 nm) and distance between sheets (10 nm vs. 14 nm).

In [14] contact resistivities and the parameters of analytic doping profiles were adjusted to reproduce measured transfer characteristics of FinFETs with L_G=20 nm [16] and then used for device simulation of the target devices with L_G=15 nm. Here, we use the same values as obtained in [14] for the simulation of the NS devices with L_G=14 nm except that there is now no channel doping in the nanosheets.

The employed MC approach is discussed in detail in Sect. II of [8]. The specifics for p-type cSiGe devices are on one hand the hole band structure which is described by the 6–band $\mathbf{k} \cdot \mathbf{p}$ model. On the other hand, both Si–type and Ge–type optical and elastic acoustic phonon scattering rates weighted by the corresponding molefraction are taken into account. All intraband and interband transitions are allowed for phonon and for alloy scattering. The alloy scattering potential is adjusted to drift mobility measurements in unstrained, lightly doped bulk Si–Ge [17]. Mechanical stress simulation [18] takes into account lattice mismatch to the substrate, source/drain etch (where the stress in the case of a Si–Ge channel is maintained by the multi-layer stack and the dummy gate oxide) and regrowth as well as dummy gate removal. In order to validate the MC model for cSiGe devices we compare in Fig. 2 the simulated long–channel effective hole mobilities with corresponding measurements [19] in planar bulk pMOSFETs for a Si-channel and a $Si_{0.75}Ge_{0.25}$-channel. With a ratio for diffusive surface scattering (accounting for surface roughness) of r_{diff}=0.07 (r_{spec}=0.93 for specular surface scattering, accounting via energy and parallel–momentum conservation for the orientation–dependence of the effective mobility, see the detailed discussion in [20]) a good agreement is obtained with the measured Si-channel mobility and also with the $Si_{0.75}Ge_{0.25}$-channel mobility. Some overestimation of the Si–Ge mobility can be eliminated by increasing the surface roughness slightly via r_{diff}=0.09, but essentially the mobility increase originating from the biaxial compressive stress due to lattice–mismatch of Si–Ge with the Si substrate is captured

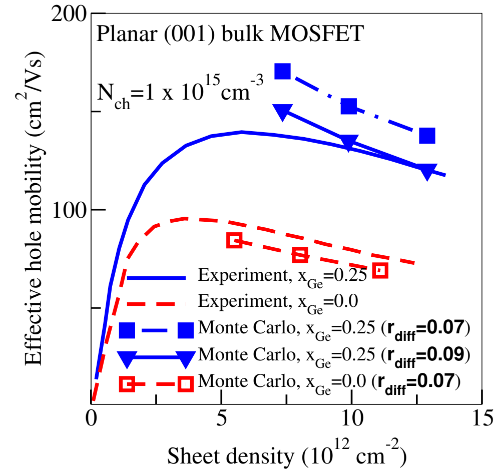

Fig. 2. Long–channel hole mobilities in planar bulk MOSFETs according to measurements [19] and 2D MC simulation. The biaxial compressive stress in the $Si_{0.75}Ge_{0.25}$-channel is about -1.5 GPa. The diffusive ratio of surface scattering, $\mathbf{r_{diff}}$, is a measure of the surface roughness. The higher value of 0.09 needed in case of the Si–Ge channel for a better agreement with the measured mobility suggests a somewhat stronger roughness than in case of the Si channel.

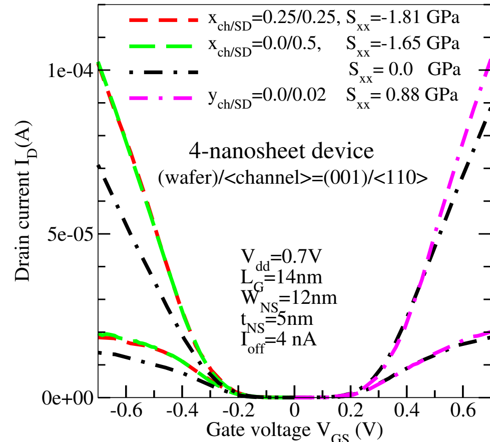

Fig. 3. MC transfer characteristics at V_{DS}=0.7 V and V_{DS}=0.05 V of $Si_{0.75}Ge_{0.25}$-channel and Si-channel nanosheet devices.

without any parameter adjustment. However, we use r_{diff}=0.15 for the simulation of Si and Si–Ge NS devices. The reason is that a higher surface roughness than for planar MOSFETs appears to be more realistic as reproducing the measured FinFET mobilities [20] involved such a higher surface roughness. This is plausible as the fins have to be etched, similar to the selective etch process for the sheet release in NS devices.

III. Short–channel result

Fig. 3 shows the short–channel transfer characteristics for the cSiGe NS device in comparison to p-type and n-type cSi nanosheets with S/D stressors (due to 50 % Ge and 2 % equivalent C concentration, respectively) and in the absence of stress. Stress relaxation reduces the performance for the p-cSi NS much more than for the n-cSi NS because of the stronger stress impact and the unfavorable (001) surface in the pMOS case. It is our main result that the p-cSiGe NS with x_{Ge}=0.25 can re–establish the same performance level of the n-cSi NS

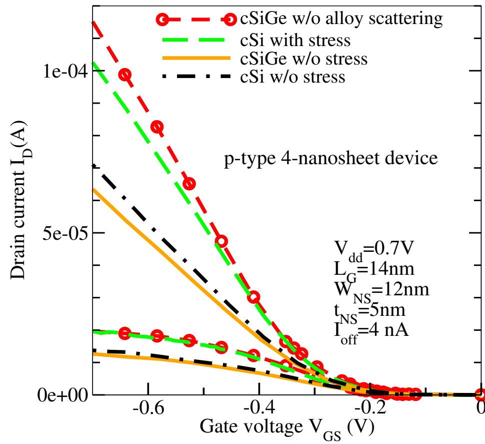

Fig. 4. MC transfer characteristics at V_{DS}=0.7 V and V_{DS}=0.05 V of the $Si_{0.75}Ge_{0.25}$-channel and Si-channel NS devices with respective S/D Ge–contents of x_{Ge}=0.25 and x_{Ge}=0.5. In addition, the result without alloy scattering as well as the results without stress are shown.

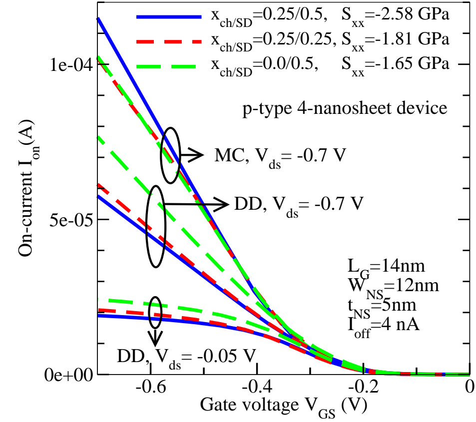

Fig. 5. Transfer characteristics of the $Si_{0.75}Ge_{0.25}$-channel and Si-channel NS devices according to MC and DD device simulations.

and even outperform the unstrained n-cSi device (though the p-cSiGe NS–ION is not higher than that of the stressed p-cSi NS despite a higher channel stress). In the latter case a better balance would be present upon changing in the context of sequential CFET [21] the channel orientation of the n-cSi NS to $\langle 100 \rangle$ or in case of a stronger surface roughness in the p-cSiGe NS as suggested by Fig. 2.

IV. Discussion

In this section we analyze a few particular conditions to provide a physical interpretation of the results in Fig. 3.

First, we investigate in Fig. 4 the influence of stress and alloy scattering. To this end we simulate two cases — cSiGe NS with x_{Ge}=0.25 in channel and S/D and cSi NS with x_{Ge}=0.5 in S/D — also in the absence of stress and without alloy scattering. Switching off alloy scattering leads now to a higher ION in the cSiGe device due to the higher channel stress, whereas the linear current remains unaffected. This can be related to the different transport regimes [22]: in the stationary case stress–induced drift–velocity enhancement is strongest for small driving fields whereas the saturation velocity is almost not improved; hence at a low V_{DS} of 50 mV, which at small L_G corresponds to a rather high driving field, the drain current is not much enhanced. In contrast, at a high V_{DS} of 0.7 V quasi–ballistic transport is present and a stress–induced reduction of the transport mass increases the velocity overshoot. And alloy scattering reduces the ballisticity leading to a degradation of the velocity overshoot and hence ION. This interpretation is supported by the IdVg curves without stress: as there is no stress benefit, a SiGe channel does not improve ION and alloy scattering then leads to an ION reduction.

The different transport regimes are further investigated by comparing in Fig. 5 ION according to drift–diffusion (DD) simulation — which corresponds also at high drain bias to near–equilibrium nonlinear transport — with MC simulation which at high drain bias is in the quasi–ballistic regime at short L_G. Here, we also consider cSiGe with a higher S/D Ge–content to study the effect of an increased channel stress

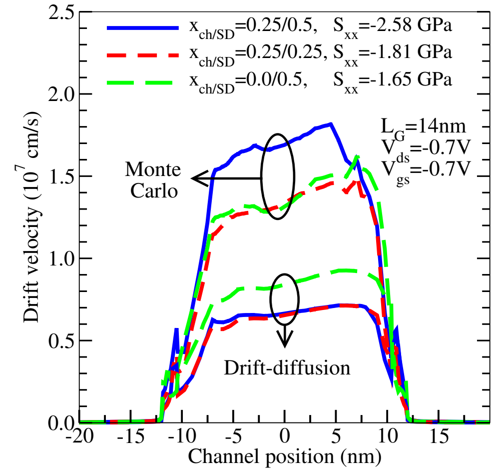

Fig. 6. Hole drift velocity profiles (averaged with the hole density over the sheet cross–section) for the NS device in Fig. 1 at L_G =14 nm.

assuming that no stress relaxation occurs. In contrast to the case of MC, it can be seen that ION according to DD is much lower for the Si–Ge channel than for the Si channel, whereas the degradation by the Si–Ge channel is weaker for the linear current. The reason is that in DD simulation the channel velocity cannot be higher than the saturation velocity which is in terms of the velocity–field characteristics an input (note that the stress–induced velocity enhancement is strongest for low driving fields and that the saturation velocity essentially does not change under stress, see Fig. 3 of [22]). And the saturation velocity in Si–Ge is smaller than in Si (because of the smaller optical phonon energy in Ge). This is reflected in the velocity profiles in the channel shown in Fig. 6 for high drain bias. For low drain bias the channel velocity is still below the saturation velocity and consequently the negative impact of its smaller value in Si–Ge is less pronounced such

that the DD drain current in the linear mode is less reduced for a Si–Ge channel.

V. Conclusion

We have demonstrated that p-type cSiGe nanosheets can achieve the performance level of n-type cSi nanosheets. This performance balance makes cSiGe nanosheets together with a potential for good stress maintenance a viable option for future technology nodes.

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