IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 28 August 2022, accepted 13 September 2022, date of publication 16 September 2022,
date of current version 26 September 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3207298

RESEARCH ARTICLE

A 2.03-mW CMOS Image Sensor With an Integrated Four-Stacked Charge-Recycling Driver for Image Signal Transmission

SANG-HOON KIM[1], (Member, IEEE), YONGSUNG CHO[1], (Member, IEEE), JIWON LEE[2,3], (Member, IEEE), JUNG-HOON CHUN[1,4], (Member, IEEE), AND JAEHYUK CHOI[1,4], (Member, IEEE)

[1]College of Information & Communication Engineering, Sungkyunkwan University, Suwon 16419, Republic of Korea
[2]IMEC, 3001 Leuven, Belgium
[3]Department of Photonics and Nanoelectronics, Hanyang University, Ansan 15888, Republic of Korea
[4]SolidVue Inc., Suwon 16419, Republic of Korea

Corresponding author: Jaehyuk Choi (choix215@skku.edu)

This work was supported in part by the Basic Science Research Program through the National Research Foundation of Korea (NRF) under Grant 2020R1C1C1011813; and in part by the Ministry of Trade, Industry, and Energy (MOTIE) under the Fostering Global Talents for Innovative Growth Program Supervised by the Korea Institute for Advanced Technology (KIAT), South Korea, under Grant P0008745. The EDA tool was supported by the IC Design Education Center (IDEC), Korea.

ABSTRACT We propose a CMOS image sensor with a dedicated low-power imaging mode and low-power integrated transmitter. The proposed CMOS image sensor selectively operates in dual mode: a high-quality mode with a 1.5 V supply voltage of readout circuits to achieve a high signal-to-noise ratio (SNR), and a low-power mode with a 0.9 V supply voltage to support always-on imaging. To further reduce the power consumption in the low-power mode, a single-slope analog to digital converter (ADC) embeds a power cutoff scheme in the comparator and a two-step conversion with dual reference voltages. To alleviate the SNR degradation in the low-power mode, which inherently occurs from voltage scaling, a correlated multiple sampling technique that consumes negligible power overhead is implemented using the proposed window-counting scheme. To reduce the significant power consumption that occurs during image signal transmission, an integrated transmitter with four-stacked charge-recycling drivers is used so that four symbols are simultaneously transmitted with a shared supply voltage. A prototype CMOS image sensor with 680 $\times$ 520 pixels is fabricated using 110-nm CMOS image sensor technology. The fabricated CMOS image sensor consumes only 301 μW (at 15 fps) in the sensor core and 2.03 mW including the transmitter and phase locked loop (PLL) while generating low temporal random noise under 0.27 LSB with correlated multiple sampling.

INDEX TERMS CMOS image sensor, correlated-multiple-sampling (CMS), dual-mode, low-power, power reduction techniques.

I. INTRODUCTION

There has been a rapid increase in the demand for CMOS image sensors (CISs), which enable the acquisition of visual information in addition to capturing pictures. This increase in demand is owing to the emergence of new applications such as augmented reality (AR), virtual reality (VR), authentication, and surveillance. The characteristics of CIS are different from those of sensors used for conventional photography. First, continuous image acquisition, that is, always-on imaging, is necessary to track objects and extract real-time information. Second, a relatively lower signal-to-noise ratio (SNR), which is sufficient for image recognition, is allowed. Third, a relatively smaller number of pixels under 640 $\times$ 480 (VGA) is acceptable, which is sufficient for image recognition.

The associate editor coordinating the review of this manuscript and approving it for publication was Chao Wang.

Because mobile and wearable devices or detachable surveillance cameras operate with limited energy sources such as batteries, the power consumption of the CIS becomes critical for long-term image acquisition [1], [2]. Although most of the research on CIS has focused on high-resolution and low-noise CIS, several studies have focused on optimizing the power consumption of CIS while avoiding significant degradation of the SNR from power reduction. The first always-on CIS with a 640 × 480 (VGA) resolution was reported in [1]. This CIS provides a separate low-power always-on mode and consumes a power of 45.5 μW in the sensor core by scaling the supply voltage (including the pixel power supply) to 0.9 V. Although the most efficient method for low power (LP) consumption is voltage scaling, if the power supply voltage is reduced to 1 V or less, the available signal range of the pixel and the analog circuit would be reduced, which significantly suppresses the SNR. To alleviate the SNR degradation, certain LP CISs use an in-pixel comparison method that compares the pixel output voltage with an external reference voltage to generate a 1-b flag instead of reading an analog voltage output through a source follower (buffer) circuit in a pixel [2], [3]. Consequently, the swing loss caused by the source follower is alleviated. However, the use of additional pixel circuits for an in-pixel comparison increases the pixel area. Therefore, the in-pixel comparison method limits the spatial resolution to below 320 × 240 (QVGA) and suppresses the SNR and dynamic range (DR) owing to the reduced fill factor.

More critically, the previous LP CISs did not consider the power consumption from the interface. Although the power consumed by the CIS core was reduced by voltage scaling or in-pixel comparison schemes, most of the power consumption in the CIS chip came from the interface. Further, the large power consumption from the interface circuit, which is inevitably located around a sensor core, causes local heating, resulting in image degradation owing to the increased dark current in the pixels.

For a system that transmits data in an existing multi-lane, such as D-PHY [10] or C-PHY [11], multiple identical lanes are used. Therefore, the power consumption increases in proportion to the number of lanes used.

In this study, we present an LP CIS that has a dedicated LP imaging mode for always-on imaging and a high-quality (HQ) imaging mode. The LP mode offers significant power reduction via voltage scaling to a supply voltage of 0.9 V. In addition, the single-slope (SS) ADC, which is the dominant power-consuming block in the CIS core, employs a power cutoff (POFF) scheme in the comparator and two-step conversion to realize further power savings. To compensate for the SNR degradation in the LP mode, we employed a correlated multiple sampling (CMS) with negligible power consumption overhead using the proposed window-counting scheme in the SS ADC. More critically, an integrated transmitter that embeds a four-stacked charge-recycling driver enhanced the energy efficiency.

The remainder of this paper is organized as follows: Section II presents the proposed CIS core with various power reduction schemes. In Section III, an integrated transmitter with four-stacked charge-recycling drivers is described. The experimental results are presented in Section IV, followed by the conclusions in Section V.

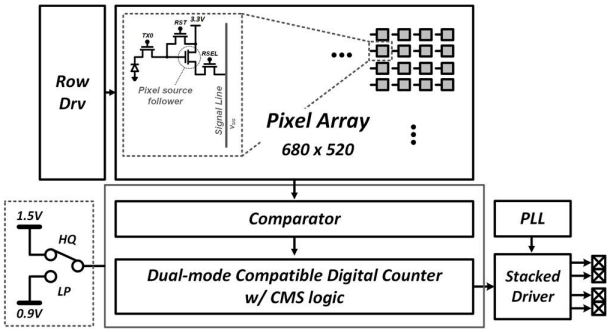


FIGURE 1. Overall architecture of the proposed CIS with dual mode.

II. SENSOR ARCHITECTURE AND POWER REDUCTION SCHEMES

Fig. 1 depicts the overall architecture of the proposed CIS. The CIS core includes a 680 × 520 pixel array with 4-transistor pixels, column-parallel 8-b/12-b SS ADCs with comparators and counters, and a row driver. The proposed CIS supports dual-mode imaging. In the HQ mode, the sensor has the same architecture as that of the conventional CIS, which has 12-b column-parallel ADCs that operate with a supply voltage of 1.5 V. An analog output from the pixel source follower that operates with a 3.3 V pixel supply voltage provides a signal swing of 1 V, and the 12-b SS ADC with a supply voltage of 1.5 V performs the conversion without any loss of signal range.

In the LP mode, the SS ADC operates at 0.9 V for power reduction, whereas the pixel is still driven at 3.3 V to guarantee the operation of the pinned photodiode (PPD). Although voltage scaling of the pixel circuits decreases the power consumption, a low pixel supply voltage prevents the use of PPDs that transfer an integrated charge into the high-potential node for the readout [1]. Accordingly, only the power supply voltage of the ADC and the digital circuit was scaled to 0.9 V, whereas the pixel power supply voltage was maintained at 3.3 V.

In the SS ADC, several power reduction schemes were implemented to attain low power consumption in the LP mode. This section provides details of the power reduction schemes.

A. TWO-STEP SINGLE-SLOPE ADF WITH POWER CUTOFF SCHEME AND DUAL REFERENCES

Fig. 2(a) depicts a schematic of the SS ADC, highlighting the locations at which power reduction techniques have been applied. Typically, a static comparator is used for the SS ADC

rather than a dynamic comparator to prevent any significant IR drop in the power supply line, power consumption in the clock distribution, and kickback effects. The POFF technique was applied to the static bias current of the comparator, and the dual-reference voltage (DREF) technique was applied to reduce the static current of the comparator and dynamic current of the digital counter.

In an SS ADC, when the digital counter stops counting after completing the operation according to the comparator output, the dynamic power is no longer consumed. However, in the comparator, even after completing the counting, there is a constant static current. The POFF technique was utilized to eliminate this wasted current. Fig. 2(b) depicts the detailed schematic of the comparator. The comparator has a general 5-transistor amplifier structure. In addition, several switches were added to apply the POFF scheme, as depicted in Fig. 3.

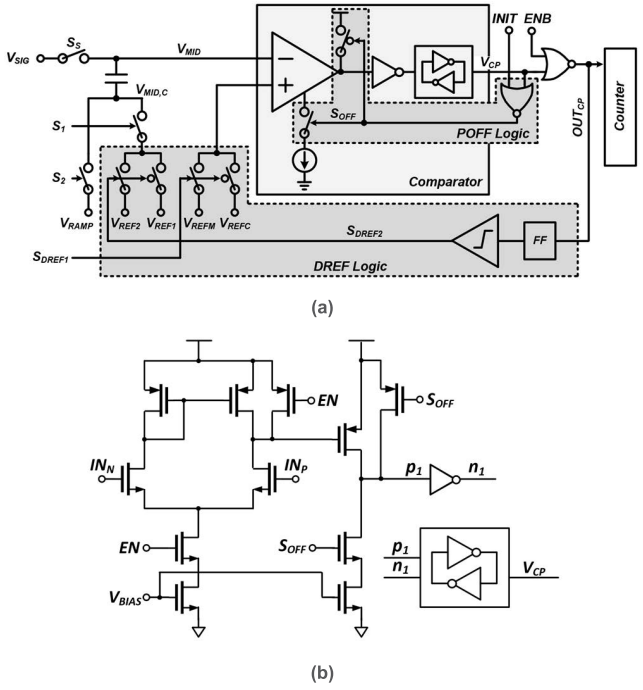


FIGURE 2. SS ADC circuits: (a) ADC circuit diagram highlighting the power reduction techniques; (b) Comparator circuit.

Fig. 3(a) depicts the SS ADC circuit using the POFF technique. The blue line represents the circuit added as a part of the POFF technique. A switch, S_{OFF}, which was controlled according to the comparator output, was added to block the static current. The comparator begins operation when the signal voltage, V_{MID}, ramps up from a voltage lower than the reference voltage, V_{REFC}. After beginning the operation, the output of the comparator goes 'high.' When V_{MID} exceeds V_{REFC}, the output of the comparator changes to 'low.' At the same time, V_{CP} and S_{OFF} are changed to 'high' and 'low,' respectively. Thereafter, the switch signal S_{OFF}, which is the output of the NOR gate, is changed to 'low.' Consequently, the static current of the comparator no longer flows. Fig. 3(b) depicts the current consumption. Without

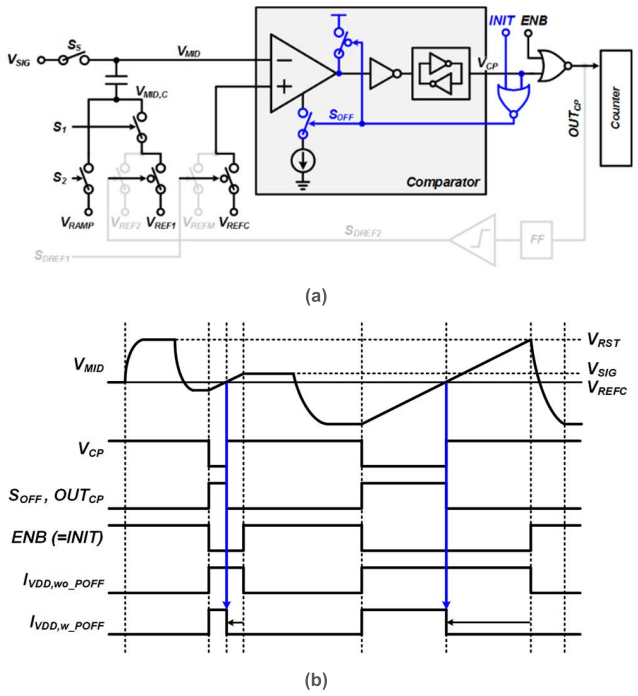


FIGURE 3. Operation of the POFF scheme: (a) Block diagram of comparator with POFF logic; (b) Timing diagram.

the POFF, a constant current (I_{VDD,wo_POFF}) flows when the comparator operates. However, with the POFF, the output of the comparator through the NOR gate, OUT_{CP}, becomes 'low,' and the current (I_{VDD,w_POFF}) is cut off. Because the comparator does not use the static current after the output of the comparator changes, the POFF scheme provides considerable power savings in dark environments. With respect to the area overhead, the POFF technique only requires six transistors.

To achieve further power saving even under bright conditions, the DREF technique, which enables two-step conversion with a short A/D conversion time, was used. Fig. 4(a) depicts a circuit using the DREF technique. One D flip-flop (DFF), one level-up shifter, and three switches (for V_{REF2}, V_{REFM}, and V_{REFC}) were also used.

The detailed operations are as follows: The A/D conversion of the reset voltage proceeds using the reference voltage of the comparator, V_{REFC}, in a regular manner. (1) Thereafter, the S_{DREF1} signal was enabled to change the reference voltage of the comparator to another reference voltage V_{REFM} that was set to V_{RST} - $\Delta V_{SIGmax}/2$ for the level decision, where V_{RST} is the reset voltage from the pixel and ΔV_{SIGmax} is the maximum input swing. If the signal voltage V_{SIG} from the pixel is lower than V_{REFM}, V_{SIG} will be in the lower half of the full signal range, ΔV_{SIGmax}. This low V_{SIG} (in bright conditions) requires a longer ramp scanning to scan the entire range of ΔV_{SIGmax}. Therefore, we adjusted the amount of level-down shifting using the second reference V_{REF2} when $\Delta V_{SIG} > \Delta V_{SIGmax}/2$. (2) If ΔV_{SIG} is greater than $\Delta V_{SIGmax}/2$, then the output of the comparator, OUT_{CP},

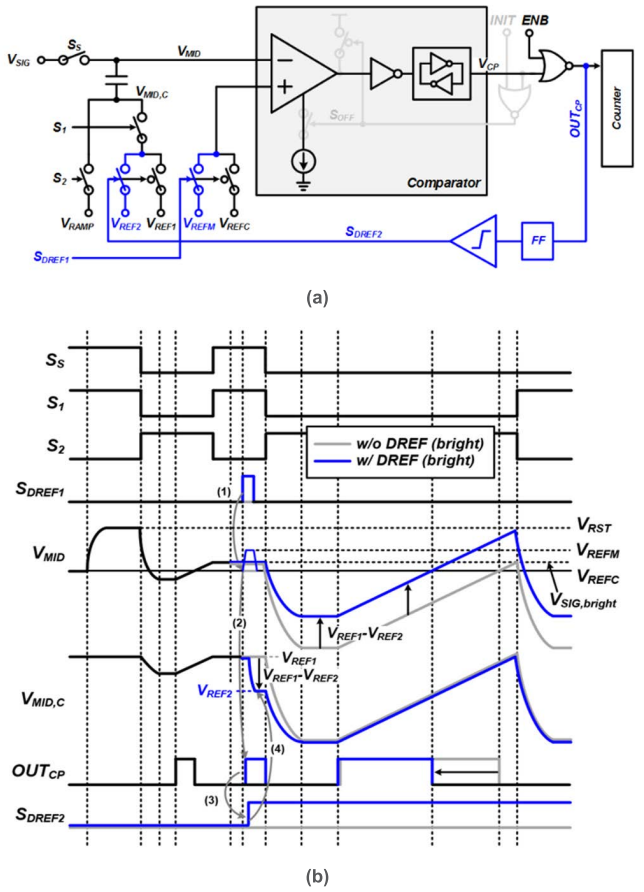


FIGURE 4. Operation of the DREF scheme: (a) Block diagram of comparator with DREF logic; (b) Timing diagram of ADC without and with DREF operation in bright illuminance.

is set to 'high.' The DFF stores this result of the level decision, which is read out after the A/D conversion to calibrate the digital output. (3) Thereafter, the decision result selects V_{REF2} and flips the switch S_{DREF2} to 'high.' (4) High S_{DREF2} varies the voltage of $V_{MID,C}$ to V_{REF2} from V_{REF1}. This change of the reference effectively increases the initial voltage of V_{MID} by 'V_{REF1}-V_{REF2}' such that the power-consuming time (when OUT_{CP} is high) is effectively reduced. Consequently, the power-consuming time of the comparator and digital counter was reduced, resulting in the further reduction of static and dynamic currents.

Note that the output of the DFF was level-shifted to control the thick-oxide transistors. Moreover, the existing comparator for the SS ADC was used for the level decision of V_{SIG} that had a high voltage from the pixel source follower (with 3.3 V supply voltage). This is possible because the comparator has low-V_{TH} thick-oxide transistors as the input transistors. Although the input transistors in the first stage operate in the triode region during the level decision owing to the high input voltages and provide lower gain, the second-stage amplifier in the comparator provides sufficient gain for the level decision. Because the DREF scheme uses only a single-ramp signal rather than dual-ramp signals from two separate ramp generators, nonlinearity from the mismatch of multiple ramp signals was not induced. There is the possibility for an offset because of the mismatch of the dual reference voltages. However, this offset can be easily post-calibrated by sampling the reset voltage successively and acquiring the digital code of 'V_{REF1}-V_{REF2}.'

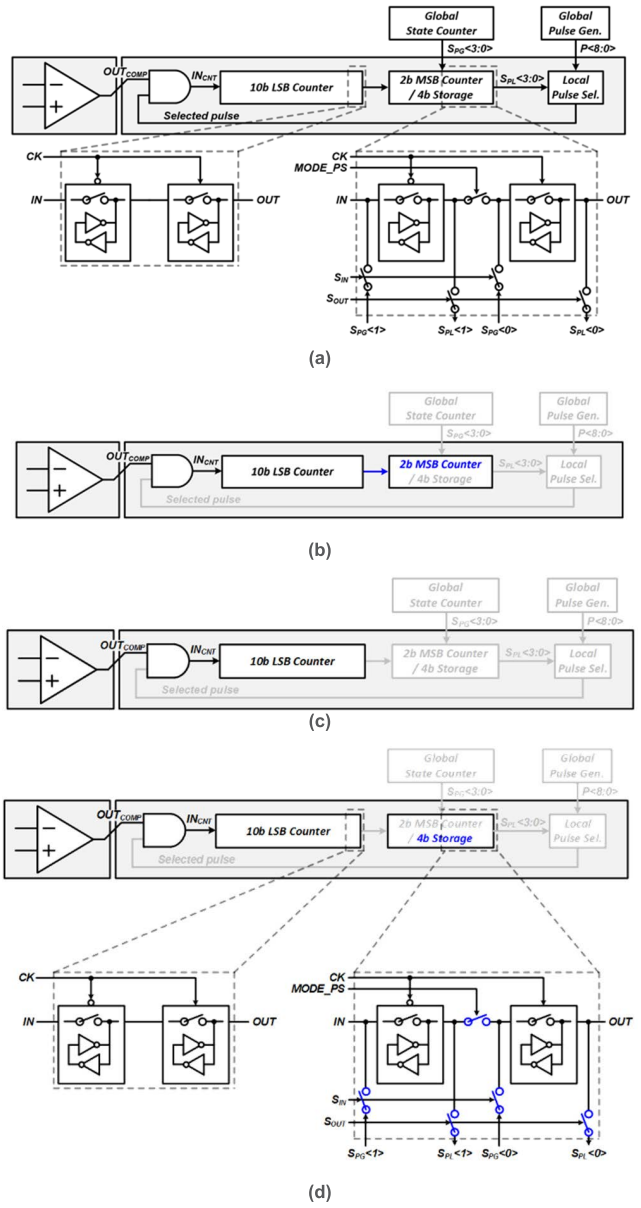


FIGURE 5. SS ADC architecture for dual mode: (a) Block diagram of the dual-mode compatible ADC; Block diagram of ADC (b) in HQ mode; (c) in LP mode; (d) in LP mode with CMS (LPCMS) operation.

B. DUAL-MODE COMPATIBLE UP-DOWN COUNTER

Fig. 5(a) depicts the block diagram of the SS ADC to illustrate the dual-mode operation. The digital counter supports 12-bit and 8-bit operations in HQ and LP modes, respectively. The digital counter consists of a 10-bit LSB counter and a 2-bit MSB counter. The LSB and MSB counters have similar structures except that the 2-bit MSB counter has additional

switches for operating as a 4-bit storage memory. This storage is required for the CMS with window counting that will be illustrated in Section II-C.

In the HQ mode, 12-bit digital counting was performed using a 10-bit LSB counter and an additional 2-bit MSB counter, as depicted in Fig. 5(b). In the LP mode, only the 10-bit LSB counter was used for an 8-bit operation without the CMS operation, as depicted in Fig. 5(c). In the LP mode with CMS (LP CMS), a 10-bit LSB counter was used to support up to four CMS operations with 8-bit digital codes. The remaining 2-bit MSB counters were used as 4-bit storage to store the CMS state required for the CMS operation, as depicted in Fig. 5(d). Only ten switches were added to the counter for the dual-mode operation in a one-column circuit.

C. CORRELATED MULTIPLE SAMPLING WITH WINDOWED COUNTING

Because an SS ADC involves 2^n iterations of high-frequency counting, the requirement for significant power consumption is inevitable. Moreover, in the conventional CMS with k-times sampling, the power consumption is increased k times [12], [13]. To achieve power savings, we implemented windowed counting that accumulates only the fine codes in the target coarse window while deactivating the power outside of the window. The first sampling out of the k-times CMS detects an appropriate coarse level of analog input. In the remaining k-1 times of CMS, we must only obtain the fine codes. Therefore, we recorded the coarse level as a 4-bit state in the first CMS. In the remaining CMS samples, a window that enables fine counting only when the time coincides with the stored state was generated. Consequently, for the k-1 samples, we performed only n-1 bit (including redundancy) fine counting, which suppressed the power consumption twice. When fast moving objects are captured, accumulating only the fine codes may induce an error because coarse levels can be changed. However, the sensor can support frame rates of up to 30 fps such that errors from the dynamic scene are eliminated.

For this LP CMS operation, the 2-bit MSB counter stores the 4-bit state locally using a 4-bit global counter. The state that is stored in each column was used to select the appropriate window generated in the global window generator. The selected window was used to perform an LP CMS operation.

To reuse the 2-bit MSB counter circuit as a 4-bit storage, only five switches were placed in each DFF, as illustrated in Fig. 5(d).

Fig. 6 depicts the CMS with conventional digital counting and the proposed windowed counting method. As illustrated, the proposed windowed counting method offers fewer counts. Note that the counting for the reset sample and for the first signal sample is the same as that of the conventional CMS operation. While converting the first sample, an appropriate state (S3) was stored (S_{PL}) from the output of the global counter (S_{PG}). While converting the second sample, an active window (P3) was generated by the global window generator (P1–P4) according to the stored state S3. The input of the

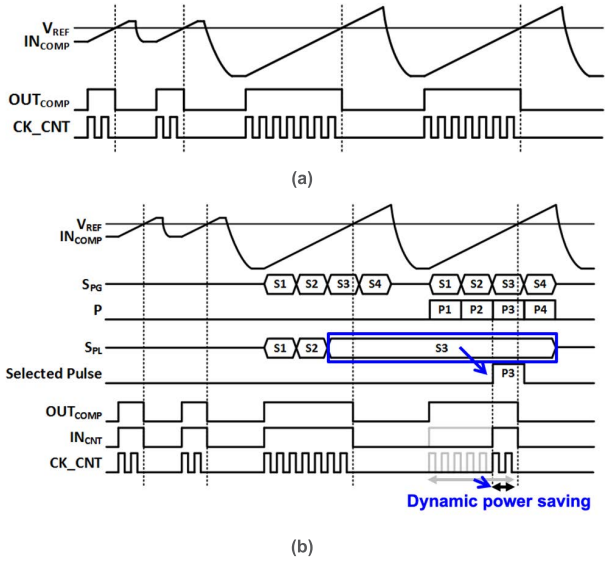


FIGURE 6. Operations of the SS ADC with two-times CMS with (a) conventional counting; (b) proposed windowed counting.

counter (IN_{CNT}) was activated by the active window and deactivated by the comparator output, OUT_{COMP}. Thus, the dynamic power used in the digital counter was reduced. It should be noted that the states for the CMS operation (S_{PG}) are represented as four states for a brief explanation in Fig. 6(b). Eight states were used for the actual implementation.

III. INTEGRATED TRANSMITTER WITH FOUR-STACKED CHARGE-RECYCLIING DRIVERS

A CIS must transmit a large number of image signals via a transmitter. In the CIS, neighboring pixels usually have similar values. For neighboring pixels, there is a higher probability that the MSB sides have the same value as that of the LSB side. For clock and data recovery on the receiver side, the received data require a specific minimum transition density. In our previous study [8], we separated the output channel into two channels for energy efficiency. One channel is responsible for transmitting MSBs with higher transition densities (HTDs) and the other for LSBs with lower transition densities (LTDs). On the transmitter side, no equalization is required to reduce power consumption and design complexity. On the receiver side, the clock and data recovery could be performed only in the HTD channel without any line coding. However, there is still a large power consumption in the driver of the integrated transmitter.

The power used in the transmitter comprises the static power used in the driver and the dynamic power used in the pre-driver and data path. The dynamic power is proportional to the operating frequency as CV^2f. Static power consumes constant power regardless of the operating frequency. Therefore, it constitutes a significant portion of the total power consumption at low speeds [9]. To reduce this dominant static power, we applied the following two techniques:

1) charge-recycling stacked driver, and 2) driver idle mode. In the case of a system that transmits data in a multi-lane, such as D-PHY/C-PHY [10], [11], as mentioned above, N drivers that consume static current in proportion to the number of drivers are required to transmit N separate sets of data. For LP imaging, we previously used a two-stacked driver recycling the static current consumed by the driver, thereby improving the static current efficiency [8]. In this study, we further improved the efficiency by implementing the four-stacked driver circuit. Fig. 7 depicts the architecture of the proposed transmitter. The outputs of the two pixels were reordered, serialized, and transmitted through the drivers. The transmitter had a four-stacked driver that could transmit the outputs for two pixels simultaneously. By stacking four driver circuits (Drv) and sharing a static current, the dominant power consumption on the transmitter side could be reduced significantly. Compared with the previous study that employed a two-stacked driver, the increase in the number of stacked drivers offered twice the current efficiency at the driver stage.

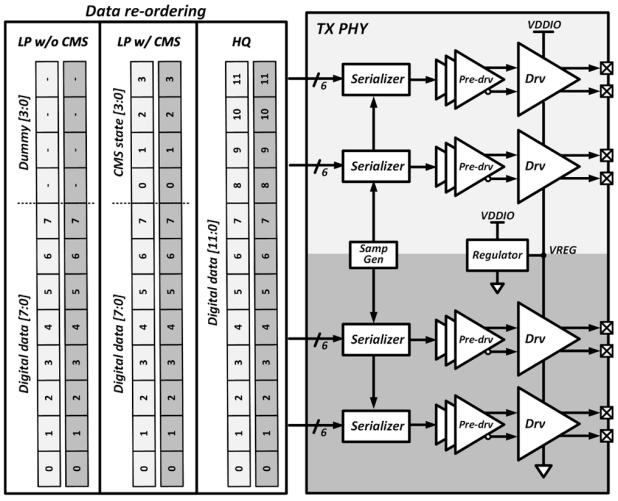


FIGURE 7. Architecture of the proposed transmitter with four-stacked charge-recycling drivers.

The transmitter receives the output of the digital counter and uses it as an input. Because the operation of the digital counter is not continuous, there is a time period within which invalid data are output. The standard C-PHY interface has an alternate LP (ALP) mode [11] to prevent additional power consumption. In the ALP mode, there is no transmission of data, and all signals in each lane are set to low in order to minimize power consumption. Similarly, in this study, simple logic gates in the pre-driver stage were used to prevent unnecessary static current on the driver in an operation where invalid data are transmitted. Each driver of the four-stacked driver had a segmented structure, and impedance matching was performed according to the number of turned-on drivers. Because the output voltage level of the driver varies depending on the stacking position of the driver, the type of driver varies for optimization, such as n-over-n and p-over-p. To turn off the driver in the idle mode, the output of the pre-driver is set to high or low according to the driver type, thereby blocking the static current path. When the driver switched from idle to active mode, the startup time was set to 1 μs to ensure stable operation. This is sufficiently larger than the minimum time from the ALP-pause-stop state of the C-PHY, which is approximately 100 ns. Owing to the simple logic gates that operate the static driver only when valid data are transmitted, the active operation time of the static driver is reduced to 20%.

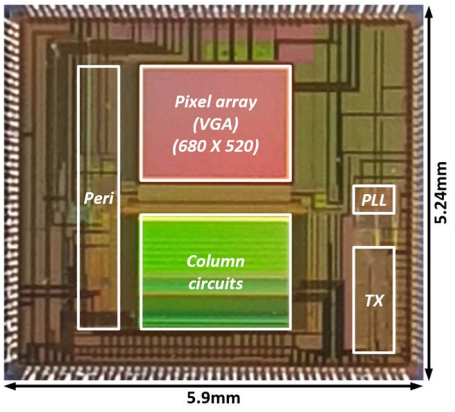


FIGURE 8. Chip microphotograph.

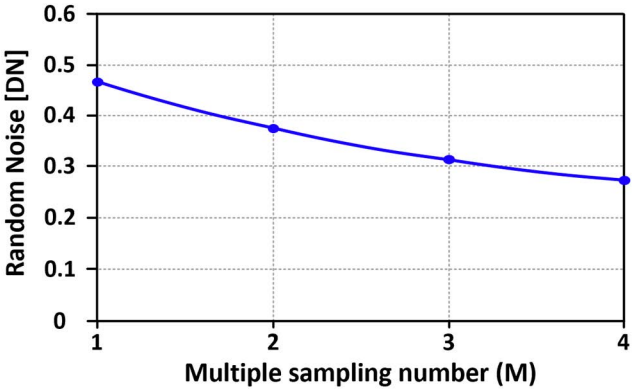


FIGURE 9. Measured dark random noise with various multiple sampling numbers from 1 – 4.

Therefore, the transmitter only consumes approximately 20% of the power, reduced from 1.91 mW–0.423 mW, compared with the power consumption when the driver is always on. In the transmitter, PRBS7/PRBS13 generators were also integrated to verify the data path and transmitter.

In the case of conventional interfaces in the image sensors [14], [15], [16], the multi-lane architecture is usually adopted because the amount of data to be transmitted is large owing to the large pixel array. The current used in the output driver increases N times according to the number of multi-lanes when using a conventional driver, as mentioned in Section III. For example, a 4-lane SLVS of 300 $mV_{pp,diff}$ uses 6 mA (= 1.5 mA*4) from four drivers. On the other hand, if the four-stacked driver which has the same swing as the SLVS

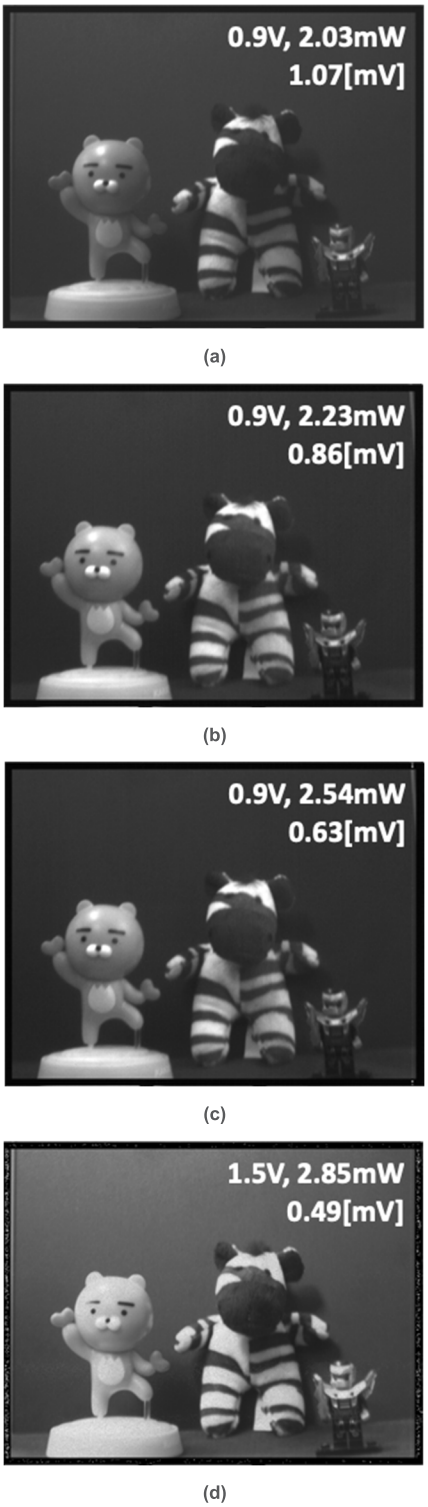


FIGURE 10. Sample images obtained from the fabricated sensor: (a) LP mode without CMS; (b) LP mode with 2-times CMS; (c) LP mode with 4-times CMS; (d) HQ mode. Power supply voltage, power consumption, and dark random noise in each mode were indicated.

is utilized, the required current consumption is only 1.5 mA. Therefore, large current consumption in the output driver due to the use of multi-lane architecture can be reduced.

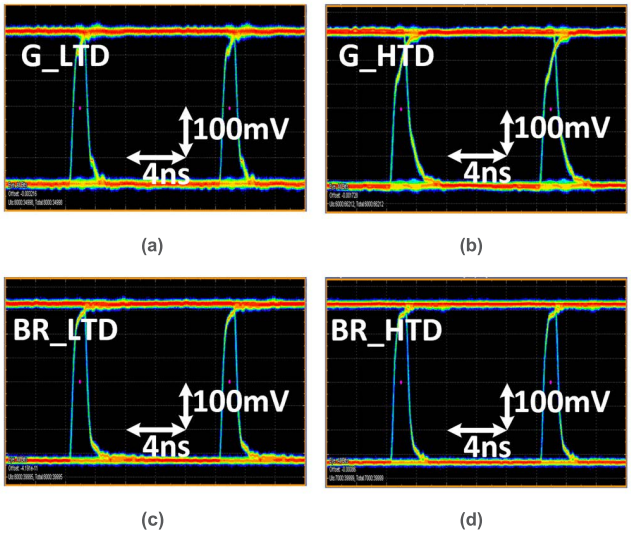


FIGURE 11. Measured eye diagrams for differential outputs: (a) G_LTD; (b) G_HTD; (c) BR_LTD; (d) BR_HTD.

IV. EXPERIMENTAL RESULTS

The proposed CIS was fabricated using a 110-nm front-side illumination CIS process. Fig. 8 depicts a die microphotograph of the fabricated sensor chip. The total chip size of the CIS was 5.9 mm $\times$ 5.24 mm. The areas of the transmitter and PLL were 1.2 mm $\times$ 0.5 mm and 5 mm $\times$ 2.5 mm, respectively. The sensor had 680 $\times$ 520 pixels, including the dummy pixels. The pixel pitch was 3.2 μm, and the length of the column circuits was 2 mm.

The CIS core uses a power supply of 3.3 V for pixels, 0.9/1.5 V for the SS ADCs, and 0.9 V for the digital readout circuits. Because of the low supply voltage and LP ADCs, the sensor core, which includes pixels, ADCs, row and column scanners, and digital readout circuits consumes only 301 μW in the LP mode and 932 μW in the HQ mode, excluding the PLL and integrated transmitter.

Fig. 9 depicts the measured dark random noise according to the number of samplings (1–4) of the CMS. The measured random noises without CMS and with 4-times CMS operations were 0.47 LSB (1.07 mV) and 0.27 LSB (0.63 mV), respectively.

Fig. 10 depicts the sample images of the different modes obtained with the implemented image sensor. In the LP modes, power consumption can be optimized to 2.03 mW without CMS, while random noise can be optimized to 0.63 mV with 4-times CMS. Even though the HQ mode provides a lower temporal noise, the LP mode offers a 29% power savings, which is suitable for always-on imaging with moderate random noise that is sufficient for object recognition [1]. Fig. 10(a) depicts an image of the 8-bit LP mode without CMS operation, and Figs. 10(b) and 10(c) depict the images of the 8-bit LP CMS mode with two and four sampling numbers, respectively. Fig. 10(d) depicts the ima1ge of the 12-bit HQ mode. All images were captured in an indoor environment.

TABLE 1. Chip characteristics and performance comparison.

Reference	[1]	[4]	[3]	[5]	[6]	[7]	This work
Process	110nm CIS	45nm CIS / 65nm CMOS	180nm CIS	180nm CMOS	65nm CMOS	350nm Std. CMOS	110nm CIS
Pixel array	340 × 260	3296 × 2512	336 × 256	300 × 200	128 × 128	800 × 600	680 × 520 (VGA)
Pixel size [μm^2]	5.0 × 5.0	1.1 × 1.1	5.6 × 5.6	7.6 × 7.6	4.0 × 4.0	16 × 16	3.2 × 3.2
Frame rate [fps]	15	7.2	15	40	32	50	15
Photodiode	p-n	-	p-n	p-n	p-n	NPD	Pinned
Supply [V]	0.9	1.2 / 2.8 / 3.3	0.8	0.4	0.5	-	3.3 (Pixel) 0.9/1.5 (SS ADC -LP/HQ) 0.9 (Digital) 1.2 (TX driver)
Core power [μW]	45.5	-	19.9	157	8.8	193k	301 (LP) 932 (HQ)
Core power FoM [pJ/pixel]	34.3	-	15.4	65.4	16.78	8.04k	56.8 (LP)
Total Power consumption w/ PLL & TX [mW]	-	-	-	-	-	-	2.030 (LP) 2.848 (HQ)
Random noise [LSB]	0.58	73 [μV]	0.95	3.96	8.32	112 [μV]	0.47 (w/o CMS @LP) 0.27 (w/ 4 CMS @LP)
CMS	-	O	-	-	-	O	O
ADC	8-bit	11-bit	8-bit	12-bit	10-bit	15-bit	8-/10-/12-bit
CFPN [%]	0.89	-	1.35	0.069	-	0.009	0.1
Integrated TX	X	X	X	X	X	X	O

The measured differential eye diagrams of the four-stacked driver outputs are depicted in Fig. 11. The output impedance was matched by adjusting the number of drivers to turn on because the output driver of the transmitter was implemented as a segmented type, as mentioned in the previous section. The designed transmitter had an area of 1.02 mm^2. The power supply voltage was 1.5 V in the PLL, 0.9 V in the data path, and 1.2 V in the driver stage. The transmitter transmitted the image signals at a rate of 400 Mbps using four channels. Because the sensor core provides image signals of 640 × 480 × 12 bits at 15 fps, the image signals were transmitted for only 16% of the total operating time. When no image signals were transmitted, all of the transmitter circuits, including the static driver circuit, were deactivated to reduce power consumption. Consequently, the transmitter consumed only 0.423 mW when transmitting 12-bit image signals owing to the stacking driver and driver idle mode. Including the power consumption from the sensor core, TX, and PLL, the total chip power consumption was 2.03 mW in the LP mode and 2.848 mW in the HQ mode.

Table 1 lists the chip characteristics and performance comparison with previous studies. All characteristics were measured at 15 fps. Power consumption was compared using the figure-of-merit (FoM), which was defined by the energy consumed by each pixel. Thus, the FoM of the proposed prototype sensor exhibited 56.8 pJ/pixel at LP mode. The FoM of the proposed CMOS imager was slightly higher than that reported in some previous studies because of the high supply voltage (3.3 V) for the pixel array that was used to support the operation of the PPDs. Because the proposed sensor employs a PPD with an nMOS source follower as is the case with a contemporary CIS, a small pixel pitch is achievable. Accordingly, the proposed architecture is applicable to high-resolution CISs. However, some previous LP sensors employed pMOS transistors and additional in-pixel circuits that are compatible with low supply voltage [4], [5], [6]. Even though the power consumption of the sensor core is slightly higher, the total chip power consumption was optimized by employing the four-stacked charge recycling drivers in the transmitter because dominant power consumption of the CIS comes from the interface circuits, which involves high-frequency switching with significant loads. In addition, only the proposed sensor employs an integrated transmitter to reduce the power consumption from the interface.

V. CONCLUSION

We implemented a dual-mode CMOS image sensor system with an integrated transmitter. Power reduction was achieved by employing a low-supply voltage of 0.9 V, LP SS ADCs with power-cutoff and dual references, and LP CMS schemes. In addition, an integrated transmitter with a four-stacked charge-recycling driver reduced the interface power. A prototype CIS with 680 × 520 pixels was fabricated using the 110-nm CIS process for verification. The sensor consumes less power (<301 μW at 15 fps) with a supply voltage of 0.9 V in the LP mode while providing low noise under 0.27 LSBs. An integrated transmitter that supports up to 400 Mbps consumes only 0.423 mW. The proposed CIS has the potential for use in low-power imaging applications, such as mobile AR and image recognition-based security solutions.

REFERENCES

[1] J. Choi, J. Shin, D. Kang, and D.-S. Park, "Always-on CMOS image sensor for mobile and wearable devices," *IEEE J. Solid-State Circuits*, vol. 51, no. 1, pp. 130–140, Jan. 2016.

[2] J. Choi, S. Park, J. Cho, and E. Yoon, "A 3.4-μW object-adaptive CMOS image sensor with embedded feature extraction algorithm for motion-triggered object-of-interest imaging," *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 289–300, Jan. 2014.

[3] J. Choi, S. Park, J. Cho, and E. Yoon, "An energy/illumination-adaptive CMOS image sensor with reconfigurable modes of operations," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1438–1450, Jun. 2015.

[4] S.-F. Yeh, K.-Y. Chou, H.-Y. Tu, C. Y.-P. Chao, and F.-L. Hsueh, "A 0.66e_{rms}^- temporal-readout-noise 3-D-stacked CMOS image sensor with conditional correlated multiple sampling technique," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 527–537, Feb. 2018.

[5] A. Y.-C. Chiou and C.-C. Hsieh, "An ULV PWM CMOS imager with adaptive-multiple-sampling linear response, HDR imaging, and energy harvesting," *IEEE J. Solid-State Circuits*, vol. 54, no. 1, pp. 298–306, Jan. 2019.

[6] N. Couniot, G. de Streel, F. Botman, A. K. Lusala, D. Flandre, and D. Bol, "A 65 nm 0.5 V DPS CMOS image sensor with 17pJ/frame.pixel and 42 dB dynamic range for ultra-low-power SoCs," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2419–2430, Oct. 2015.

[7] N. Chen, S. Zhong, M. Zou, J. Zhang, Z. Ji, and L. Yao, "A low-noise CMOS image sensor with digital correlated multiple sampling," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 1, pp. 84–94, Jan. 2018.

[8] S.-H. Kim, H. Shin, Y. Jeong, J.-H. Lee, J. Choi, and J.-H. Chun, "A 12-Gb/s stacked dual-channel interface for CMOS image sensor systems," *MDPI Sensors*, vol. 18, no. 8, pp. 1–14, Aug. 2018.

[9] W. Bae, "Supply-scalable high-speed I/O interfaces," *MDPI Electron.*, vol. 9, no. 8, pp. 1–21, Aug. 2020.

[10] *Specification for D-PHY, Version 3.0*, MIPI Alliance, Piscataway, NJ, USA, Jul. 2021.

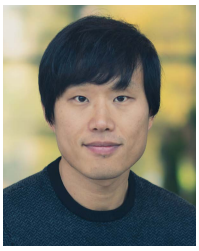
[11] *Specification for C-PHY, Version 2.1*, MIPI Alliance, Piscataway, NJ, USA, Jul. 2021.

[12] Y. Lim, K. Koh, K. Kim, H. Yang, J. Kim, Y. Jeong, S. Lee, H. Lee, S.-H. Lim, Y. Han, J. Kim, J. Yun, S. Ham, and Y.-T. Lee, "A 1.1e^- temporal noise 1/3.2-inch 8Mpixel CMOS image sensor using pseudo-multiple sampling," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2010, pp. 396–397.

[13] Y. Chen, Y. Xu, Y. Chae, A. Mierop, X. Wang, and A. Theuwissen, "A 0.7e^-_{rms}-temporal-readout-noise CMOS image sensor for low-light-level imaging," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 384–385.
[14] M. Sakakibara, "A back-illuminated global-shutter CMOS image sensor with pixel-parallel 14b subthreshold ADC," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 80–82.
[15] C. Xu, Y. Mo, G. Ren, W. Ma, X. Wang, W. Shi, J. Hou, K. Shao, H. Wang, P. Xiao, Z. Shao, X. Xie, X. Wang, and C. Yiu, "5.1 A stacked global-shutter CMOS imager with SC-type hybrid-GS pixel and self-knee point calibration single frame HDR and on-chip binarization algorithm for smart vision applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 94–96.
[16] C.-L. Chen, S.-W. Chu, B.-J. Chen, Y.-F. Lyu, K.-C. Hsu, C.-F. Liang, S.-S. Su, M.-J. Yang, C.-Y. Chen, S.-L. Cheng, H.-D. Liu, C.-T. Lin, K. P. Petrov, H.-W. Chen, K.-C. Chu, P.-C. Wu, P.-T. Huang, N. Na, and S.-L. Chen, "5.3 An up-to-1400 nm 500 MHz demodulated time-of-flight image sensor on a Ge-on-Si platform," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 98–100.

SANG-HOON KIM (Member, IEEE) received the B.S. degree in semiconductor system engineering and the Ph.D. degree in electrical engineering from Sungkyunkwan University, Suwon, South Korea, in 2013 and 2020, respectively. In 2021, he joined Samsung Electronics, Hwaseong, South Korea, where his focus was on the design of DRAM, such as GDDR6. His research interests include analog and digital circuit design for low-power and high-speed serial links, CMOS imager systems, and memory interfaces.

YONGSUNG CHO (Member, IEEE) received the B.S. and M.S. degrees in semiconductor system engineering from Sungkyunkwan University, Suwon, South Korea, in 2018 and 2020, respectively. In 2020, he joined Samsung Electronics, Hwaseong, South Korea. His research interests include analog and digital circuit design for low-power CMOS image sensors.



JIWON LEE (Member, IEEE) received the Ph.D. degree from the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2013. From 2013 to 2018, he was a Senior Researcher at Samsung Electronics, Yongin, South Korea. From 2018 to 2022, he was with IMEC, Leuven, Belgium, as a Principal Member of Technical Staff. Since 2022, he has been an Associate Professor with the Department of Photonics and Nanoelectronics, Hanyang University (ERICA Campus). His research interest includes novel image sensor pixel development for various applications.

JUNG-HOON CHUN (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1998 and 2000, respectively, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, USA, in 2006.

From 2000 to 2001, he was with Samsung Electronics, Hwasung, South Korea, where he developed a BiCMOS RF front-end IC for wireless communication. From 2006 to 2008, he was with Rambus Inc., Los Altos, CA, USA, where he was involved in the development of high-speed serial interfaces, such as FlexIO, XDR, and XDR2. He is currently a Professor with Sungkyunkwan University, Suwon, South Korea. He is a Co-Founder and the Chief Technical Officer with SolidVue Inc., Suwon, which is commercializing solid-state LiDAR sensors. His current research interests include high-speed serial links, CMOS imagers, on-chip ESD protection and I/O design, and new memory devices.

Dr. Chun was a recipient of the IEEE SOI Conference Best Paper Award, in 2010, the IEEE CICC Best Paper Award, in 2008, the Benhamou SGF Fellowship, from 2003 to 2005, and the Gold Medal from the Humantech Thesis Competition, in 1998. He served on the Technical Program Committee for IEEE A-SSCC, from 2009 to 2011, and from 2014 to 2021.

JAEHYUK CHOI (Member, IEEE) received the B.S. degree in electrical engineering from Yonsei University, Seoul, South Korea, in 2004, the M.S. degree in electrical engineering and computer science from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2006, the M.S. degree in electrical and computer engineering from the University of Minnesota, Minneapolis, MN, USA, in 2008, and the Ph.D. degree from the University of Michigan, Ann Arbor, MI, USA, in 2013.

From 2013 to 2015, he was a Research Staff Member with the Samsung Advanced Institute of Technology (SAIT), Samsung Electronics, Suwon, Korea, where he performed research related to depth sensors and low-power image sensors. In 2015, he joined the Department of Semiconductor Systems Engineering, Sungkyunkwan University, Suwon, South Korea, as an Assistant Professor. He is currently a Co-Founder and the Chief Executive Officer with SolidVue Inc., Suwon, which is commercializing solid-state LiDAR sensors. His research interests include low-power circuits, CMOS sensors, and mixed-signal integrated circuits.