# Exploration of Scandium Doping in $Sb_2Te_3$ for Phase Change Memory Application

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*Abstract*—**In this work we fabricate and electrically demonstrate a 65nm technology- compatible PCM pillar device using Sc- doped SbTe (ST) instead of GeSbTe (GST), for the first time fabricated on 300mm wafer in 1T1R configuration. ST was chosen over GST to achieve a higher speed and endurance due to its faster crystallization speed and reduced volume variation during switching. Detailed knobs how to improve stack in terms of CD, thickness (of electrode and chalcogenide material) and Sc doping are presented. The optimized stack shows AC switching from 300ns-1µs for SET and RESET with current in the order of mA and programming voltage less than 2.5V. The endurance shows marginal memory window degradation up to 1E8 cycles and more than 1hour retention at 85°C is achieved for the optimized stack of C:Si /50nm ST:Sc 6%. The fabricated devices show potential to extend PCM technology towards high-speed SCM applications.**

*Index Terms*— **Emerging Memory Technology, Nonvolatile Memory, PCM, Chalcogenide, GeSeTe, SbTe, doping Sc, SCM**

## I. INTRODUCTION

Phase change random access memory (PCRAM) is a mature non-volatile memory and commercially available [1] which represents a high-density solution for SCM. It can cover a wide range of products/applications divided in memory-type or storage-type SCM [1,2], embedded memory [3], as well as neuromorphic computing [4]. To be compatible for SCM application, PCM must show high density, good reset power/current density, endurance, set speed, adequate crosstalk robustness and good reliability [4-10].

PCM material is sandwiched between 2 metal electrodes and can change its state from disordered amorphous (high resistance state-HRS) to ordered crystalline (low resistance state -LRS), when electrical current is applied through the device. This contrast in resistivity can be translated into transition from logic "1" to logic "0" and can be repeated many times without degrading the performance of the devices. The contrast between these HRS/LRS can be up to 4 orders of magnitude. The amorphization or RESET operation requires high voltage and short pulse duration, while Crystallization or SET operation needs smaller but longer pulse. That's why the cell performance is mostly limited by the SET Operation [11-13].

Our target is to improve the SCM performance, thus we need the pillar structure for high density integration. Current materials (GST, doping GST, etc.) when integrated in the pillar structures usually show poorer performance (slower switching speed and worse endurance) than mushroom structures. Slower speed in pillar structures happens as there are more crystallites in the amorphous states of the mushroom cell and these surrounding crystallites facilitates its crystallization process [14-16]. Hence, we need to study new materials to improve the PCM performance. As reported in literature, scandium-doped antimony telluride ($Sb_2Te_3$:Sc) in the mushroom structure showed superb switching speed (nearly 10x faster than the GST baseline data using the same fabrication conditions), due to the strong Sc-Te bonds which introduce more nuclei and effectively enhance the stability of nucleation embryos, prolonging the lifetime against thermal fluctuations [8,17].

In this work, we integrate the material in the pillar structure and investigate the switching behavior, endurance, and retention properties. Some optimization methods are suggested in the conclusion section to improve the device performance.

## II. PCM THIN FILM CHARACTERIZATION AND PROPERTIES

In this paper, we investigate the Sc doped $Sb_2Te_3$ as PCM stack where physical properties and Sc doping are evaluated while the Sb/Te ratio is kept fixed. During the thin film development, Sc doping is varied from 0.6% to 8.9% using RF source power for concentration less than 3% and DC power for higher concentration. Rutherford Back-Scattering (RBS) measurements are used to verify the Sc concentration in the blanket film. The Sb/Te is about 0.77 instead of 0.67 according to Particle Induced X-ray Emission (PIXE) measurements, so we assume to have a Sb-rich film. To study the transition of the material from amorphous to a crystalline phase upon thermal treatment, Rs (Sheet Resistance) and X-ray diffraction (XRD) analysis is done. For Rs measurements, samples of 2x2cm are cut and annealed for 10min in $N_2$ at atmospheric pressure at fixed temperature ranging from 100 to 550°C. XRD measurements are done in-situ on a gradually heated sample. The sample is heated on a chuck from room temperature to 650°C in a He atmosphere with a ramp up rate of 0.2°C/s. During heating the diffracted X-rays are detected with a line detector in a 10–50-degree 2Theta window. The results are summarized by the colormap in Fig.1 where the intensity of the diffraction patterns is represented by a color change from blue (low count) to red (high count). Crystallization is clear by the formation of 3 high intensity regions (2θ: ~18°, ~26°, ~45°) when the temperature is above 200°C, which correspond to planes (006), (009) and (0015), respectively in agreement to [18]. With the increase in the Sc doping concentration, there is a slight shift to the right for all those peaks, indicating a higher crystalline temperature.

## III. FABRICATION OF 1T1R DEVICES

### A. PCM stack composition and fabrication

The schematic with layer details and the TEM of the fabricated device are shows in Fig. 2(a) and Fig. 2(b), respectively. The device is integrated between two metallization lines in the back end of line (BEOL) of a 300-mm 65nm CMOS-compatible process flow. The pillar device
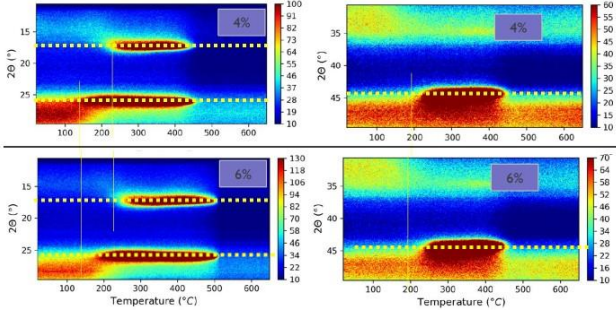


Fig.1 XRD colourmap at different temperatures for 2 different compositions of Sc in a 50nm ST film. The dotted lines represent the crystallization peaks position at $2\theta$: ~18°, ~26°, ~45°.

consists of a Sc-doped $Sb_2Te_3$ layer deposited by physical vapor deposition (PVD), sandwiched between the top electrode (TE) and the bottom electrodes (BE), both consists of TiN layer. An additional Si-doped carbon liner is deposited directly at top and bottom of the PCM film as heater element. Sc-doped $Sb_2Te_3$ layers and Si-doped carbon layers were deposited in an Anelva C-7100GT magnetron sputter system, by respectively co-sputtering Sc and $Sb_2Te_3$ and silicon plus carbon in a multi-cathode chamber at room temperature, using an Ar plasma. The Sc sputter power was varied to obtain different Sc concentrations. The TE stack includes a Ru etch stop layer used for patterning purposes.
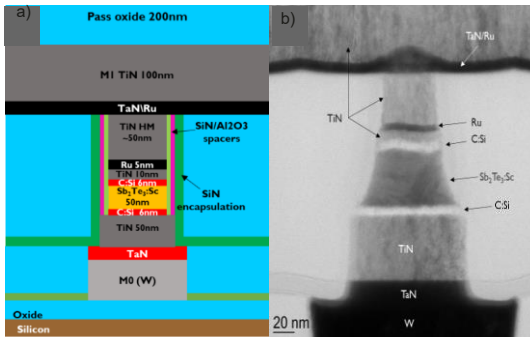


Fig.2 SbTe:Sc stack layer details (a) and TEM image (b).

The pillar is patterned by reactive ion etch (RIE) using $Si_3N_4$ and $Al_2O_3$ spacers. After the RIE etch, the pillar is encapsulated with a $Si_3N_4$ layer. From the RIE process, the pillar acquires a 18.89°sidewall slope. The detailed patterning of Sc doped SbTe (SbTe:Sc) using RIE process is given in the next section. The thicknesses split of the Sc doped $Sb_2Te_3$ layer was 35 nm and 50 nm, respectively. The thickness splits of the C-Si based liner of 6 nm and 10 nm respectively are investigated.

### B. Patterning of Sc doped SbTe (SbTe:Sc)

The SbTe:Sc layer is patterned using a hard mask (HM) stack. The HM consists of (from the top) 50 nm $SiO_2$/15 nm Ru/65 nm TiN/5 nm Ru as described in Fig.2a. In addition, 2 nm TaN are deposited on Ru to act as an adhesion layer for $SiO_2$. A F-based chemistry is used to etch the top $SiO_2$. The chemistry is then switched to an $O_2$-based mixture to etch the Ru layer. The etch of the Ru layer uses a gas chemistry which is different from that of the $SiO_2$ and TiN parts of the HM. Therefore, as the $SiO_2$ on top of the pillar is consumed during the $Cl_2$-based TiN etching, the Ru layer on top of the TiN layer acts as an etch stop layer.

An over-etch of the TiN layer is performed to ensure a uniform etch across the entire wafer. Due to the presence of the bottom Ru layer, the over-etch step does not negatively impact the surface and patterning of the SbTe:Sc layer. The bottom Ru layer is finally etched with $O_2$-based chemistry again prior to the patterning of SbTe:Sc-based active layer. The C:Si electrodes are patterned using an $O_2$/Ar-based chemistry. The SbTe:Sc layers is patterned using an $HBr$/$C_2H_4$ mixture.

After the HM opening, the SbTe:Sc active stack is patterned in two steps using a spacer approach. First, the top electrode and the SbTe:Sc layers are patterned, followed by a $SiN$/$Al_2O_3$ ex-situ encapsulation and further etching of the bottom electrode (BE). This method is used to protect the SbTe:Sc from any $Cl_2$-induced lateral chemical damage during the etching of TiN BE.

Considerable amount of $C_2H_4$ passivation is used during the etch of the SbTe:Sc layer in order to protect its sidewalls. This is because chalcogenides are highly volatile when exposed to halogens and, thus, highly prone to chemical damage [19]. The anisotropic etching of the SbTe:Sc layer is ensured by using high bias and low pressure. However, the Sc present in small percentages in the chalcogenide is expected to be sputtered as it does not form any volatile etch by-product with any of the halogen etchants. Final step of the stack patterning is the removal of any remaining Ru layer from the top of the HM to access and connect the active device to the next metal layer of connections. The width of the pillar at the location of the C-Si based liner is taken as the pillar width. Different cells with pillar widths of 65nm, 80nm and 100nm were fabricated.

## IV. DEVICE PROPERTIES

Three different device structures are used for the electrical characterization: 1R, 1R1R and 1T1R. 1R structures are used as process monitors to validate the pillar functionality and Within Wafer (WIW) variability. Considering a statistic of 16 devices for each measurement, the following device DoE has been



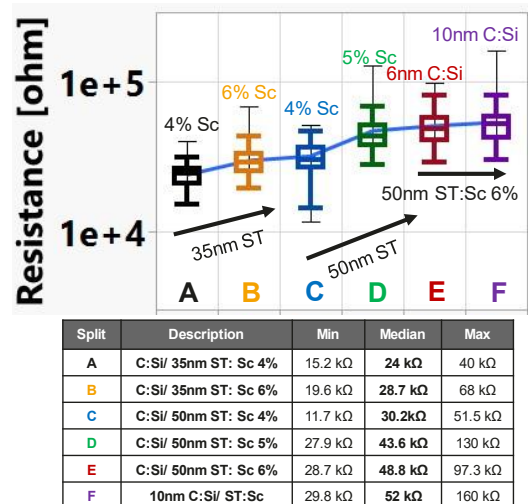| Split | Description | Min | Median | Max |
|---|---|---|---|---|
| A | C:Si/ 35nm ST: Sc 4% | 15.2 kΩ | 24 kΩ | 40 kΩ |
| B | C:Si/ 35nm ST: Sc 6% | 19.6 kΩ | 28.7 kΩ | 68 kΩ |
| C | C:Si/ 50nm ST: Sc 4% | 11.7 kΩ | 30.2kΩ | 51.5 kΩ |
| D | C:Si/ 50nm ST: Sc 5% | 27.9 kΩ | 43.6 kΩ | 130 kΩ |
| E | C:Si/ 50nm ST: Sc 6% | 28.7 kΩ | 48.8 kΩ | 97.3 kΩ |
| F | 10nm C:Si/ ST:Sc | 29.8 kΩ | 52 kΩ | 160 kΩ |

Fig.3 Initial Resistance vs split comparison. The table contains the median values and the min/max for split comparison.

analyzed: Pillar CD (65nm, 80nm, 100nm), chalcogenide thickness (35 and 50 nm); Sc doping concentration (4, 5, 6%) and C:Si electrode thickness (6 and 10 nm). Fig.3 shows the initial leakage current for ST 50nm 1R devices where the Sc doping concentration was varied from 4 to 6%. The increase of the Sc doping concentration leads to increase of initial resistance similar to reference [14]. Then we fix our doping to 6% and modulate the chalcogenide thickness from 35 to 50nm. The extracted median in Fig.3 confirms the trend that by increasing ST thickness we can increase the initial resistance of our devices. If we fix thickness and doping of our chalcogenide to 50nm and 6% respectively, we modulate electrode thickness C:Si from 6 to 10nm and it does not change the device property as the initial resistance is comparable for both thicknesses.

## V. DEVICE PERFORMANCE

### A. Electrical Characterization Methodology

In this section, the AC switching and endurance test is described in detail. Same method is used for both 1R1R and 1T1R structures, but few changes are done to optimize the correct operating of each structure since we have 2 and 3 terminal devices respectively as shown in the testing sequence of Fig 4 and 5.
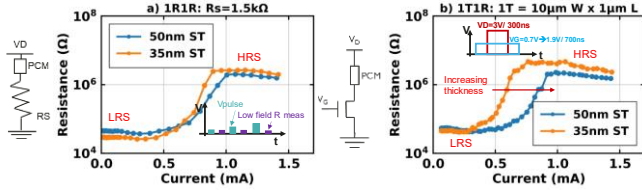
Fig.4 Device and Testing schematic for a) 1R1R and b) 1T1R for SET-RESET sequence in AC mode – median R trend of 16 devices.

In 1R1R structures, series resistance is chosen after correct calibration to achieve the correct current range. In our case it is 1.5 kΩ/1mA as reported in Fig.4a. In 1T1R devices, $V_G$ modulation allows to modulate the programming current at constant $V_D$=3V/300ns by controlling the transistor gate voltage. The switching is performed using ISPP method through a pulse generator. $V_G$ is increased progressively from 0.7V to 1.9V at 700ns. Programming time is defined by $V_D$ pulse of 300ns (rise and fall time are equal at 10ns) as demonstrated in Fig.4b.

The phase change material can be switched from low to high conductive state, and vice-versa, through applying electrical current pulses. The electrical pulse used to switch the device from low- resistance crystalline (LRS)

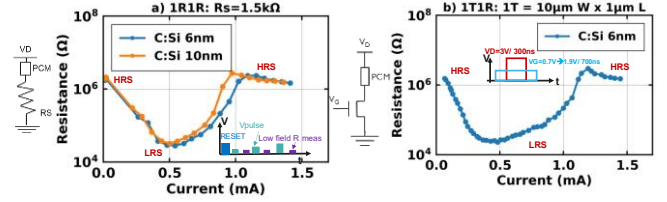to the high-resistance amorphous state (HRS) is referred

Fig.5 Device and Testing schematic for a) 1R1R and b) 1T1R for RESET-SET-RESET sequence in AC mode.

to as RESET pulse. We extract the resistance value by measuring the electrical resistance of the PCM device at low field of 0.1V. For RESET-SET-RESET operation: we use another set of 16 pristine devices with as deposited structures in low resistive state LRS. The AC pulse used to switch the device from high resistance amorphous to the low-resistance crystalline state is referred to as SET pulse. This can be done by using a RESET-SET-RESET sequence. Since the devices as deposited are in crystalline LRS we perform an initial RESET operation with 3V fixed at 300ns as shown in Fig.5a. Then we apply the ISPP sequence for the RESET –SET operation with increasing V to maximum 3V with fixed pulses of 1µs. The resistance is read after each operation in DC through a SMU by applying a low readout voltage of 0.1V. The testing scheme for 1T1R structures is shown in Fig.5b. Different from 1R1R structures where the voltage applied on top electrode is variable, in 1T1R structures is fixed and we modulate the gate voltage instead.

We noticed that 1R1R and 1T1R behavior are similar as shown Fig.4 and 5 for SET-RESET and RESET-SET-RESET test respectively. So, in the next paragraph we will mainly focus in 1R1R devices for AC switching and first test of endurance.

### B. SET/RESET AC Operation 1R1R

We have studied the impact in AC behavior of 65 nm CD devices with series R of 1500 Ω. In Fig.6a we report median resistance of 16 devices as a function of current for different splits used in our DoE. By fixing a factor 10*LRS, we can extract the RESET current for each split. Same factor is used to extract the RESET voltage. Then for each split we calculate the total energy as the product of programming current, voltage and pulse duration fixed at 300ns. This value is normalized by the reference stack and reported in Fig.6b for RESET1 operation. RESET 1 is the operation switching the device from as-deposited (LRS in our case) to HRS at pulses of 300ns. We use this parameter as a comparison metrics between splits to identify trends and the stack with optimized electrical properties.
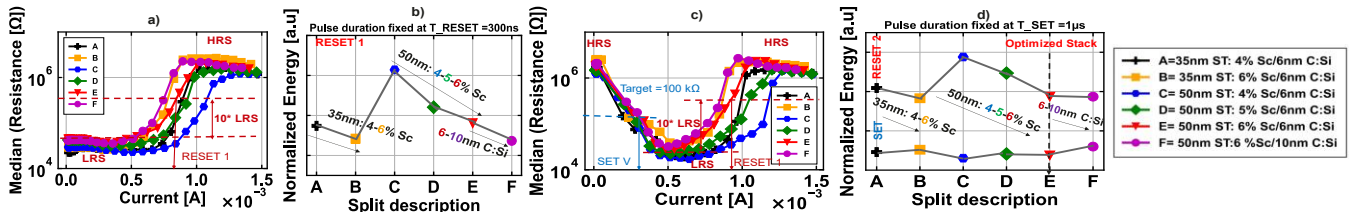
Fig. 6 (a) Median R (LRS to HRS) as a function of programming current for different splits at CD=65nm. (b) Normalized Energy for RESET1 operation for each split using factor 10*LRS as a criterion to extract RESET current for each split. c) Median R as a function of programming current (HRS -LRS- HRS) for different splits at CD=65nm. (d) Normalized Energy for SET and RESET2 operation for each split using factor 10*LRS as a criterion to extract RESET current for each split.

The results in Fig6a and b can be interpreted as follows:

**Sc-doping:** Smaller Reset current is shown with increasing Sc content from 4-6% for both 50nm and 35nm thicknesses.

**ST-thickness**: Steeper transition SET to RESET is shown for 35nm ST:Sc layer, suggesting better thermal efficiency (better thermal coupling between C:Si electrodes and chalcogenide volume) current density for 65nm CD. Devices with 50nm ST can achieve 15MA/cm$^2$ RESET current density.

**C:Si electrode:** Steeper transition SET to RESET is demonstrated for thicker C: Si layer, suggesting better thermal efficiency (enhanced joule heating and less heat loss from ST layer) for 10nm thickness.

From the graph in Fig.6a and b, 10nm C:Si/50nm ST:Sc 6% is the optimized stack for RESET1 Normalized Energy.

### C. RESET/SET/RESET AC Operation 1R1R

RESET-SET-RESET operation is shown for 65nm CD devices with series R of 1500 Ω. We perform a RESET operation of 3V/300ns to switch our devices in HRS. The testing sequence reported in Fig.5 is applied and studied for 1μs. Similar to section A, we extract the RESET2 programming current (and voltage with similar approach) for each split using a factor 10*LRS as shown in Fig.6c. RESET 2 is the operation needed to switch the device from LRS (programmed with a previous SET operation at 1μs) to HRS. While we keep a target R value of 100 kΩ to extract the SET programming parameters. These values are used to calculate the energy needed during SET and RESET 2 operations reported in Fig. 6d.

The main learning from graph Fig.6c and Fig. 6d are:

**Sc-doping:** smaller Reset current is shown when increasing Sc content. It requires 1.2mA-1mA-0.8 mA to achieve HRS=10*LRS when increasing doping content from 3%-5%-6%.

**ST-thickness**: Steeper transition SET to RESET for thinner ST:Sc layer, suggesting better thermal efficiency (better thermal coupling between C:Si electrodes and chalcogenide volume).

**C:Si electrode**: steeper SET RESET transition for thicker C:Si layer, suggesting better thermal efficiency.

Finally, from Fig.6 we identify similar trend for RESET 1 and 2 confirming the normalized E can be used as a comparison metrics for different splits. SET Normalized Energy shows slightly different trend for doping content but confirms that the optimized stack is 6nm C:Si/50nm ST:Sc 6% if we consider the overall impact on SET and RESET2 Normalized Energy.

### D. Optimization of SET – Operation 1T1R

From sections A, we have identified our optimized stack in terms of switching speed and power. We think we can further improve AC switching by using an optimized testing scheme where we fix pulse amplitude and increase pulse width from 1ns to 3ms as shown in Fig.7. Programming pattern consists of a double pulse and low field resistance measurement at 0.1V. Constant RESET pulse (3V, 300ns) is used to initialize the cell to a known RESET state. Variable SET pulse consists of $V_{SET}$ = {1.5V, 1.7V, 1.9V} with 30ns<$T_{SET}$ <2.9μs.
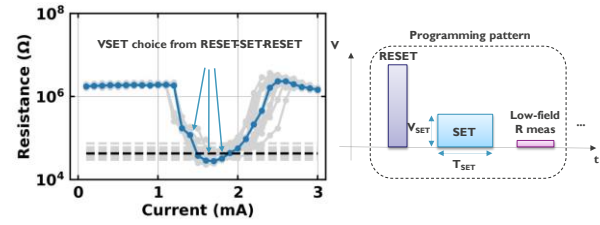


Fig.7 Optimization testing scheme for SET operation varying programming voltage and pulse duration.

Results are reported in Fig.8. Resistance gradually decreases with increasing SET pulse width. At least 1μs is necessary for full SET operation with 100% yield. While for a HRS of 100 kΩ, 300ns programming time can be enough. The trend does not seem to depend on SET programming Voltage.
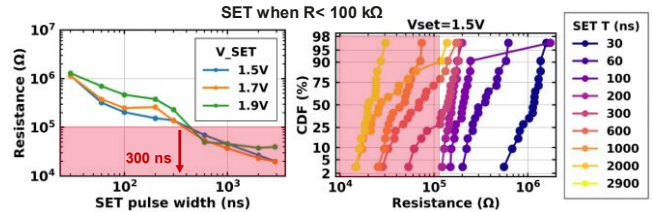


Fig.8 (left) Resistance vs SET pulse width and (right) CDF distribution dependence on pulse width using optimized SET scheme for 50nm ST:Sc 6% and CD=65nm.

We have tested splits with increasing doping Sc content from 4% to 6% for stack with 50nm ST to better understand the SET pulse impact on doping. The results are in Fig.9. SET speed increases (SET pulse width decreases) with increasing Sc-doping content from 4%-6% for single devices using a criterion HRS/LRS>10.

We need to further improve our technology to reach high speed performance. Our hypothesis is that this can be done by increasing further doping >6% for PCM thickness of 50nm and CD=65nm based on the projected trend.

### E. Comparison of ST film with GST ref

In this section we compare our ST material with standard GST in terms of electrical properties.

The graph in Fig. 10 shows the median of 16 tested devices programmed at 300ns pulse with ISPP method for the RESET Resistance versus RESET current.
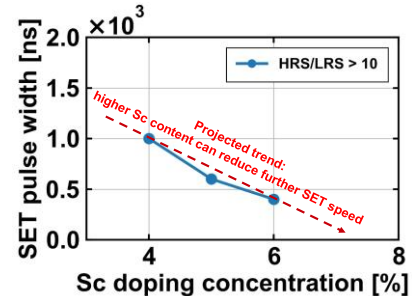


Fig.9 SET pulse width vs Sc doping content for 50nm ST:Sc and CD=65nm. Projection trend shows that shorter SET pulses can be achieved by increasing Sc-doping > 6%.

Resistance value on the vertical axis is the low field resistance measured at 0.1V after each Voltage pulse. The current on the horizontal axis is the max current flowing through the device during the application of each Voltage pulse (from oscilloscope

waveform voltage drop on a 50Ω series resistor). Smaller RESET current of 0.8mA is shown compared to GST reference 1.1mA to reach a factor 10*LRS for a similar device with CD=65nm. This is consistent with larger initial resistance of ST film. AC Endurance of 1R1R (series R of 1.5kΩ, CD=65nm) schematic is shown in Fig. 11. We test 16 devices using the SET/RESET sequence up to 1E8 cycles. For the first 10 cycles it is read after each operation, while for the next cycles it is read only 3 times for decade.
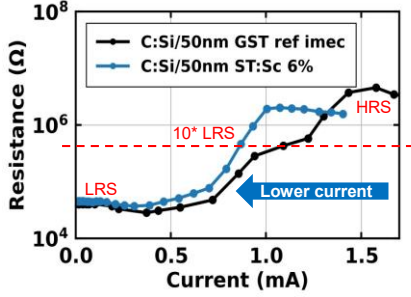


Fig.10 Comparison of AC switching during SET-RESET operation for pillar 50nm GST ref and 50nm ST:Sc 6%. ST needs lower programming current to reach a factor 10*LRS than GST reference.

Fig.12a reports the endurance results for GST imec reference devices. We can compare the GST endurance behavior with the ST film shown in this work. Fig.12c reports the endurance behavior of our ST stack when the SET is programmed at 1.2V/1µs. This is also the same programming condition used to SET both GST and ST devices. For ST film we can improve endurance behavior by increasing the SET pulse from 1V as reported in Fig.12b to 1.2V reported in Fig.12c. ST devices show more stable endurance behavior compared to GST reference as shown in Fig12a and c.

The results for optimized ST (1T1R pillar structure) are summarized and benchmarked with other PCM materials in pillar 1R and 1T1R structures in Table 1 [15-16,20].



Fig.11 Schematic for LRS and HRS endurance test up to 1E8 cycles.

## VI. RELIABILITY

In this section, we will discuss about reliability study of our 1T1R structures namely endurance (up to 1E8 cycles SET/RESET) and retention at high T (85 and 125ºC />24 hours). Transistor with dimension of W=10µm, L=1µm is chosen to achieve correct device operation at mA ranges. The optimized stack used for the measurement is C: Si/50nm ST:Sc 6%/C:Si with CD=65nm and 16 devices are tested during LRS and HRS-state. To program each state, we use $V_{G-SET}$=1V/1µs and $V_{G-RESET}$=1.9V/300ns and we repeat the sequence SET/RESET for 1E8 cycles. After each operation, we read the state at low V of 0.1V. The results in Fig.12b show median of 1-decade LRS/HRS ratio after 1E8 cycles, but degradation of MW occurs during the subsequent cycles. The degradation is noticed for LRS (still stable behavior in median value) due to material segregation. We further increase the programming current during SET operation to further improve the endurance behavior. We program LRS at 270µA reported in Fig.12b and 470µA in Fig.12c obtained by increasing Gate Voltage from 1V to 1.2V at pulse width of 1µs. RESET conditions are maintained fixed for 2 tests at 1.9V/300ns. As we can deduct from the graph, by increasing $I_{SET}$, we can improve the endurance of LRS and HRS States. After endurance test is finished, a post-cycling switching is applied to verify if failed devices can still recover their initial HRS state. Graph in Fig.12d represents devices pre- and post-cycling. The initial resistance state can be recovered after stress, but we need higher programming current of 1.3mA, while initially we could reach factor 10*LRS at 0.8mA. As the cycled device becomes more conductive and more current is needed to reset the device [20-21]. In Fig.13 we extract memory window – MW factor calculated as ratio between HRS over LRS for 3 conditions of programming current during cycle 1, intermediate cycle 1E4 and final cycle 1E8. As we can see for 1st cycle if we increase programming current, memory window increases from 1 decade to 27. Increasing number of cycles to 1E4 decreases the MW for all programming conditions but after 1E8 cycles, MW is increased further from 17 to 45. MW increases due to LRS decrease with cycling as confirmed by Fig.12c. The next test is retention at high temperatures to evaluate the thermal stability of our PCM devices. We study both LRS and HRS with programming conditions: RESET state programmed with single pulse $V_D$=3V/300ns, $V_G$ =1.9V/ 700ns. SET state programmed with ISPP routine $V_D$ = 3V/1µs, $V_G$ is increased from 0.7V to 1.2V/2.3µs until it reaches the target resistance value of $R_{threshold}$ =33k Ω. The statistics of
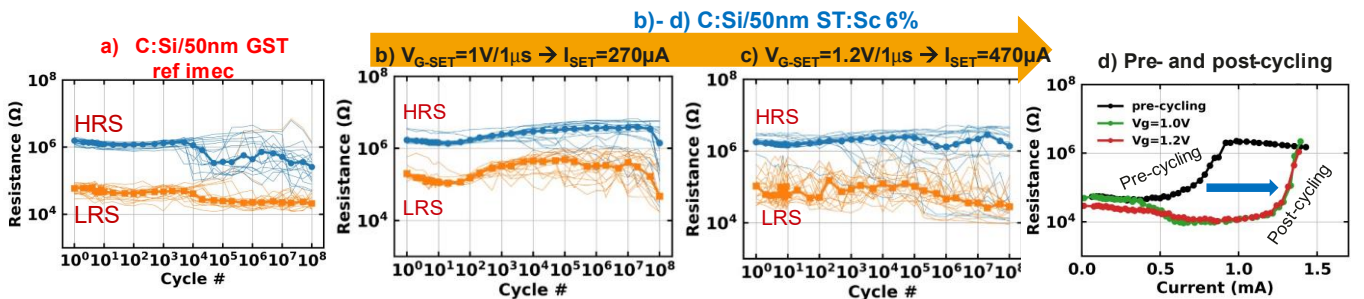


Fig.12 Comparison of evolution of LRS and HRS during 1E8 cycling experiment for a) C:Si/50nm GST reference at imec. Endurance performance for 50nm ST:Sc 6% at CD=65nm for b) $V_{G-SET}$=1V and c) $V_{G-SET}$ =1.2V. (d) HRS post-cycling for $V_{G-SET}$=1 and 1.2V reaches same level as pre-cycling at higher programming current for 50nm ST:Sc 6%.

tested devices is 35-40 devices per condition. After programming LRS and HRS states, the devices are put in oven at 85ºC for 1hour (Fig.14a). The resistance is read at room temperature and low field of 0.1V. Then the test is repeated for total accumulated time of more than 4 hours.
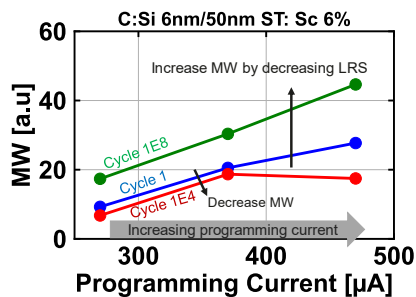


Fig.13 MW as a function of increasing programming current for Fig. 12c.

The LRS is very stable, but HRS has more variability and degrades already after 1 hour. Even if the memory window is degraded, there is at least 1 decade in median between LRS and HRS States. After 4 hours the HRS states degrade further overlapping of the SET and RESET distributions as shown in Fig. 14a but does not close completely the memory window at median values.
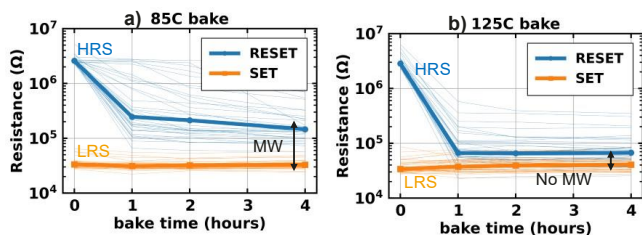


Fig.14 (a) Retention test at 85ºC and b) Retention at 125ºC for LRS and HRS for same stack of 50nm ST:Sc 6% and CD=65nm devices.

If we increase the temperature >125ºC/4hrs (Fig. 14b), the HRS degrades even faster degrading the memory window. These results indicate that the failure mechanism is due to temperature accelerated crystallization of the amorphous RESET state.
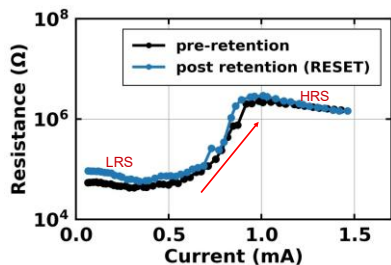


Fig. 15 AC switching of 10 devices post-retention at 85°C showing no degradation for HRS compared to pre-retention state.

We need to improve further the thermal stability of our devices in the future. After retention, we performed a post-retention switching test to see if we can still recover our devices undergone high temperature test at 85°C and the results show very good overlap of AC switching graphs pre- and post-retention for RESET-HRS state shown in Fig. 15. High temperature induces loss of stored data without impacting the

properties of the device.

| Materials | GST: N[15] | GST[16] | GST:X[20] | ST:Sc This Work |
|---|---|---|---|---|
| Pillar CD (nm) | 75 | ~40 | ~90 | 65 |
| Deposition | PVD | ALD | PVD | PVD |
| HRS/LRS ratio | 10X | 10X | 10X~1000X | 100X |
| $I_{RESET}$ (µA) | 900 | >600 | N.A. | 700 |
| $T_{RESET}$ (ns) | 65 | N.A. | N.A. | 300 |
| $I_{SET}$ (µA) | 100 | N,A, | N.A. | 300 |
| $T_{SET}$ (ns) | 300 | >2E3 | 500 | 1E3 |
| Endurance | >1E6 | 2E12 | >1E10 | >1E8 |
| Retention@85°C | N.A. | N.A. | N.A. | >1hr |
| Configuration | 1R1R Rs=10kΩ | 1T1R | 1T1R | 1T1R |

Table 1. Benchmarking of PCM pillar properties [15-16,20].

## CONCLUSION

In this work we presented our latest result on PCM technology. The devices were fabricated in 300mm tool and 65nm technology node in pillar 1T1R configuration. We presented a full analysis of material and device study of SbTe Chalcogenide doped with Sc content 4-6%. Electrical performance in terms of AC switching with pulse width of 300ns, endurance up to 1E8 cycles/1 decade of memory window and retention at 85ºC/1hr show promising results. Our optimized stack is C:Si 10nm/ 50nm ST:Sc 6% with CD=65nm. Compared to GST reference, our ST devices show lower programming RESET current and better endurance properties. We believe the stack can be further improved by process engineering (etch, encapsulation), further increasing the Sc concentration and PCM thickness scaling down to 15nm together with a CD reduction below 55nm.

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