Vapor deposited thin organic-inorganic capping layers preventing copper line oxidation in polymer-based RDL technologies

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Abstract

Hybrid organic-inorganic and inorganic multilayer films were deposited using a combination of CVD and ALD processes to develop an ultra-thin barrier to prevent copper oxidation in a polymer-based RDL technology. ALD layers are known to be effective permeation barriers due to their uniformity and pinhole-free morphology. However, the low deposition temperature, required by the presence of polymers in the final product, increases their susceptibility to degradation by water. In this study, polymer-embedded copper lines protected by ultra-thin vapor deposited cappings, processed at temperatures below or equal to 100 °C, were exposed to oxidation and corrosion stress tests for more than 1000 hours. Above a critical thickness of 8 nm, copper oxidation is fully blocked. In addition, it is demonstrated that some of these ultra-thin layers can withstand a corrosion stress test paving the road for their integration in polymer-based RDL technologies.

Keywords: Capping layer, Atomic layer-deposited, copper oxidation, RDL technology

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1. Introduction

Customer needs for faster electronic products with enhanced features and smaller form factors have pushed the industry toward advanced packaging technologies relying heavily on heterogeneous integration. To meet the requirements for the ever increasing number of connections between adjacent chips, redistribution layers (RDL) are a key enabler. To minimize the routing complexity and reduce the number of metal layers, the critical dimensions of the RDL lines must be decreased [1–3]. Among the different options, the most promising involves a dual damascene approach where copper lines are embedded in a high-resolution photo-sensitive polymer [3, 4]. Nevertheless, this approach induces serious reliability challenges, amidst them, the polymer inability to block atmospheric oxygen being the most critical as it results in copper oxidation at elevated temperature [5–9]. Indeed, copper is known for its ease to oxidize even at relatively low temperatures, i.e. below 200 °C [10–12]. While a self-limiting oxidation process is generally assumed [5, 13–15], evidence suggests that an initial oxide layer does not protect from further oxidation [16, 17]. As the increasing demand for more complex systems constantly reduces the critical dimensions [4], high rates of oxidation in the copper lines become a major reliability concern [18].

While capping solutions have been extensively studied in standard CMOS technologies (e.g. SiN for corrosion protection [19–21], SiCN, SiCO and $MnSiO_3$ as copper diffusion barrier [22–27], CuSi and cobalt cappings to increase reliability performance [28–31]. . .), their high process temperature prevents them from being used in a polymer-based RDL process. As a result, protective barrier coatings, based on low temperature atomic layer-deposited (ALD) thin films have found an application in the field of organic electronic devices [32–36]. ALD is based on sequential and self-limiting surface chemical reactions, resulting in extremely conformal, highly dense and pinhole-free films [37, 38]. The low defect concentrations found in these films create excellent gas permeation barriers and their suitability against moisture diffusion has been demonstrated [39–41]. Although deposition temperatures below 120 °C are now commonly achieved [32, 35, 42–45], the resulting films generally present degraded barrier performances due to an increased defect density [39, 43] as well as an enhanced susceptibility to corrosion [40, 46, 47] leading to larger critical thicknesses. Since a decrease of the deposition temperature results in extended processing times, achieving thinner reliable capping layers is of pri-

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mary importance.

In this study, thin nanolaminates have been processed on top of copper RDL lines and their performance as potential capping layers have been assessed after oxidation and corrosion stress tests.

2. Experimental

These investigations were performed on polymer based RDL samples manufactured using a damascene approach and 300 mm silicon wafers. The dielectric used in this study is a negative tone thermoset phenol-based photosensitive polymer manufactured by JSR Corporation. Normal TMAH developer is used for the development. Subsequently, the material is cured at 200 °C, which is below the glass transition temperature (T_g).

The RDL stack starts on top of an initial insulating layer with the coating of the polymer, and the subsequent exposure and development steps to open the trenches for the RDL metal layer. A multistep curing process with a maximum temperature of 200 °C is then applied to cure the polymer. Afterwards, a 30 nm Ti thin film followed by a 150 nm Cu seed layer are deposited using a Physical Vapor Deposition (PVD) process. The Ti layer acts as a copper adhesion and diffusion barrier layer. Filling of the line is performed by growing electrochemically deposited (ECD) copper on top of the seed layer while a CMP process is used to flatten the stack and remove the excess copper. At this point, the wafers are diced into coupons of around 2.0 by 2.5 cm to enable the testing of several capping solutions.

Capping layers have been processed directly on top of the RDL layer in a SPTS MVD300 chamber at temperatures below or equal to 100 °C. The Molecular Vapor Deposition (MVD®) method used in this study was previously described in [48]. Prior deposition, two splits received an argon–hydrogen plasma pretreatment for 10 minutes using a remote downstream microwave plasma (unbiased samples). The plasma power was set at 3 kW, while the chamber was maintained at a pressure around 0.5 to 1 Torr under a 10,000 sccm gas flow. The various capping layer splits tested in this study are summarized in table 1. To mimic the final product, the coating and curing of an additional polymer layer was performed. The full process flow is summarized on Fig. 1 while more process details are available in [4].

Prior to the capping deposition, the polymer surface was characterized by atomic force microscopy (AFM). Using a Bruker Dimension Edge, AFM micrographs were recorded in tapping mode by an Olympus micro cantilever OMCL-AC160TS-R3, with a reflective Al coating, a spring constant set at 26 N/m, and a resonant frequency around 300 kHz. Gwyddion version 2.56 [49] was used to process the AFM images and extract roughness profiles. As shown in Fig. 2a, the surface roughness was measured in an area around 10 µm by 10 µm presenting a succession of copper lines embedded in polymer. As shown in Fig. 2b, at the end of the CMP process, the surfaces of the polymer and metal lines are relatively smooth with a total roughness root mean square below 2 nm.

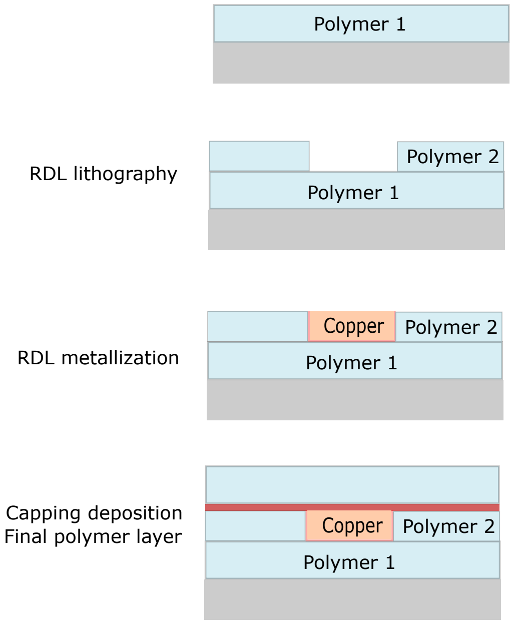


Figure 1: Schematic description of the dual damascene process flow used in this study.

Table 1: Summary of the different capping layer thicknesses used in the study.

#	Laminate	Temperature (°C)	Plasma	Thickness (nm)
1	A	≤ 100	-	33
2	A	≤ 100	Ar/H_2	33
3	B	≤ 100	-	12
4	C	≤ 100	Ar/H_2	10
5	D	≤ 100	-	8
6	E	≤ 100	-	8
7	F	≤ 100	-	6

Capping layer thicknesses were assessed through ellipsometry using a Woollam M-2000DI ellipsometer using wavelengths ranging from 193 to 1690 nm at incident angles of 50°, 60° and 70°. The copper substrate, copper oxide layer, and the capping layer were modeled with B-spline, Tauc-Lorentz, and Cauchy models respectively. The characterizations were achieved on silicon or copper substrates placed along with the RDL coupons in the MVD chamber.

Three different reliability stresses have been used to trigger and study the failure mechanisms of interest in capping layers. Copper oxidation was induced through high-temperature storage (HTS) performed at 150 °C for 1000 h in a nitrogen-rich dry air environment using a Thermo Scientific Heraeus UT6060 oven. The oxygen content in the oven during the oxidation process was 2 %. A thermal cycling (TC) stress consisting of 1000 cycles between -50 °C and 125 °C enabled potential mechanical issues at the interface between the capping layer and the copper lines or the polymer to appear. TC cycles were conducted in a

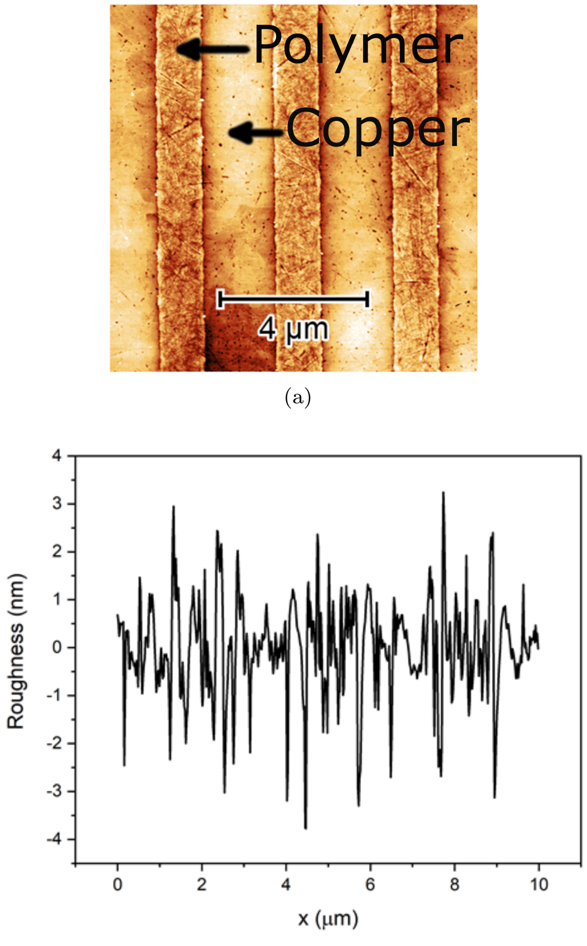


Figure 2: Roughness of polymer and copper surface measured by AFM. The characterization was performed after the RDL layer CMP. a) Characterization was performed in a 10 µm by 10 µm area presenting multiple copper lines embedded in polymer. b) Resulting roughness profile.

Weisstechnik TempEvent T/270/70/20. Finally, the capping layer susceptibility to degradation by water was assessed by performing a temperature-humidity stress (TH) executed at 85 °C and 85 % RH in a climate chamber WEISS SB22 for 1000 h followed by a HTS stress at 150 °C for 1000 h. This dual stage reliability stress enabled moisture to travel to the interface of the polymer/capping layer to trigger a potential chemical reaction between the capping layer base material and water, ultimately resulting in the degradation of the barrier properties [40]. The HTS step is then used to induce copper oxidation and reveal the presence of pin holes in the capping layer as it is known from previous reliability studies that TH alone will not induce the growth of a significant copper oxide layer [18]. At the end of the stresses, the presence of copper oxide on top of the lines was verified by performing cross-sections of the copper lines by focused ion beam (FIB) milling using a FEI Helios Dual Beam system.

Tests and stress conditions were selected in accordance with the AEC-Q100 standard [50].

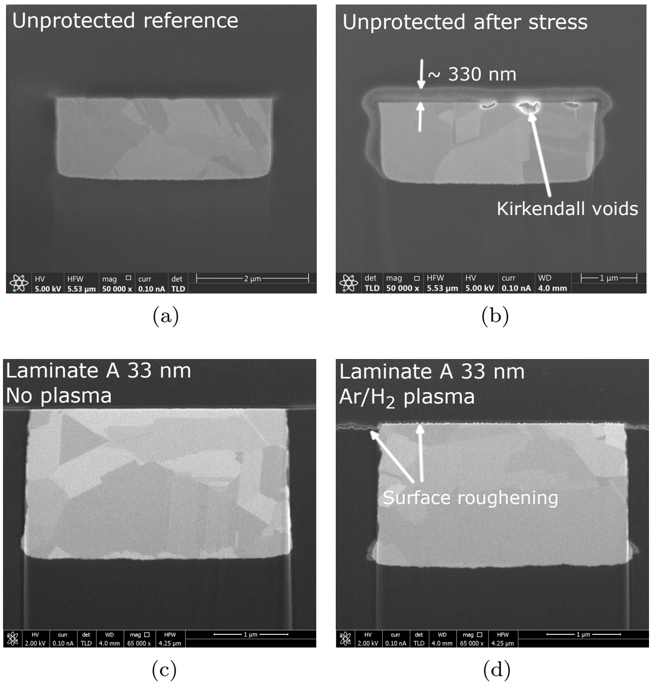
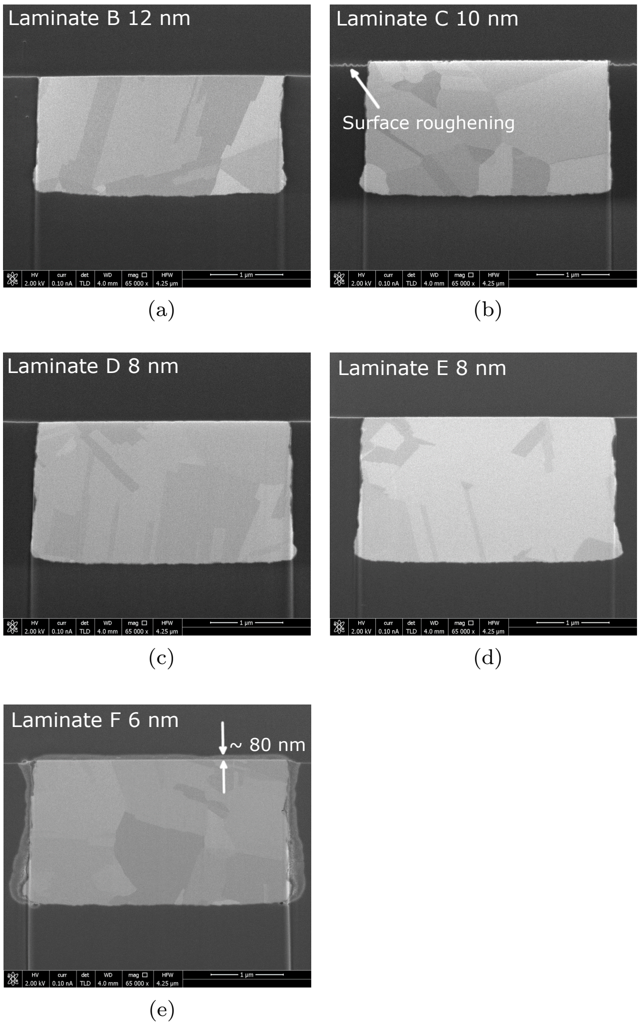


Figure 3: FIB cross-sections of a copper metal line encapsulated in polymer. a) Reference unstressed sample. b) After 1000 hours spent at 150 °C, a 330 nm thick oxide layer is present at the top of the metal line and Kirkendall voids appeared at the interface copper–oxide. c) and d) A copper oxide layer is not detected on top of the metal lines after 1000 hours of stress at 150 °C when the line is protected by a 33 nm thick capping layer. Roughening of the polymer–metal surface is observed after the plasma pretreatment.

3. Results and discussions

The impact of a high temperature storage stress, performed at 150 °C for 1000 hours, on unprotected copper lines is shown in Fig. 3a and 3b. While the presence of copper oxide at the top of the metal lines is not observed before the stress (Fig. 3a), after storage at high temperature, a 330 nm thick layer of oxide is visible on top of the lines (Fig. 3b). In comparison, oxidation is fully blocked on copper lines covered with a 33 nm thick nanolaminate as presented in Fig. 3c and Fig. 3d. To minimize the deposition time and increase the throughput, as well as to simplify the via opening process needed to connect to the next metal layers, a drastic reduction of the capping thickness is needed. Nevertheless, as seen on Fig. 3d, when a plasma pretreatement is applied before the deposition, a roughening of the polymer and metal surface is observed which could ultimately lead to non-continuous capping layers when their thicknesses are decreased and therefore limit the achievable critical thickness.

Fig. 4 displays the FIB cross-sections obtained on samples protected with thinner capping layers and stored at 150 °C for 1000 hours. When the capping thickness is above 8 nm, copper oxidation is fully blocked (Fig. 4a to Fig. 4d). On the contrary, with a capping layer thickness reduced to 6 nm, an 80 nm thick oxide layer is de-

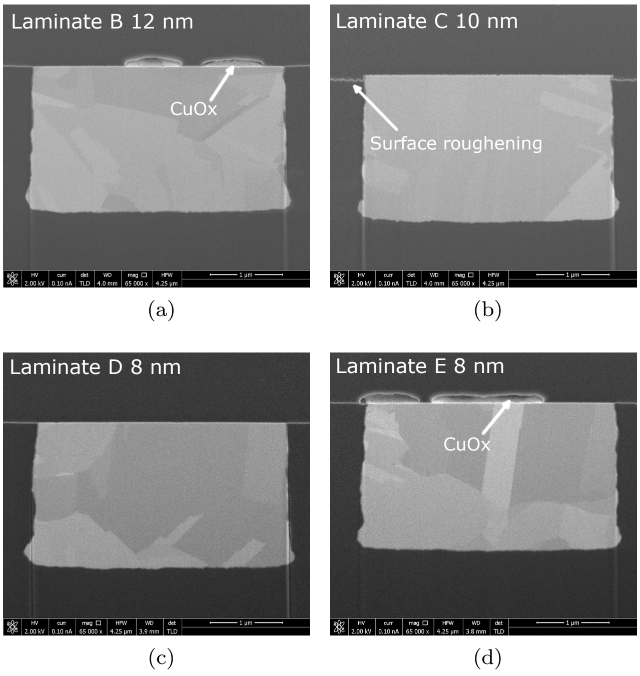


(a) (b) (c) (d) (e)

Figure 4: a), b), c) and d) After HTS, oxidation is not observed on lines protected by a capping layer thicker than 8 nm. e) On the contrary, a 6 nm thick capping layer is insufficient to protect copper from oxidation.

tected on top of the copper line resulting in a decrease of the oxide thickness by a factor 4 compared to an unprotected sample (Fig. 4e). These observations confirm that a 6 nm thin capping layer does not completely seal the copper surface, most likely due to the high defect density observed in thin ALD layers deposited at low temperature [43, 51]. It follows that for these films and process conditions, the critical thickness is around 7 to 8 nm, in good agreement with values previously reported in the literature for these deposition temperatures (7.5 nm with a deposition at 100 °C by Carcia et al. [43], or 5-10 nm at 80 °C by Klumbies et al. [35]).

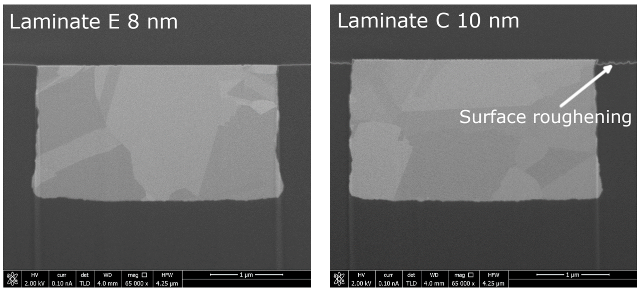
FIB cross-sections performed at the end of the corrosion stress are presented in Fig. 5. These samples have been subjected to a sequence of reliability stresses: first they underwent a TH stress to trigger a potential chemical reaction between the capping layer and moisture resulting in a weakening of the barrier properties. Subsequently, HTS is used to oxidize the copper line in areas where the capping layer has been attacked. As shown in Fig. 5a and Fig. 5d, copper oxide islands are found on top of the lines when they are protected by 12 nm of laminate B or 8 nm of laminate E. On the other hand, oxidation is not observed when the lines are protected by 8 nm of laminate D (Fig. 5c), confirming that the susceptibility to corrosion by water is a property of the laminate material as previously reported by Singh et al. [52]. Despite the roughening of the polymer and copper surfaces due to the plasma pretreatment, oxidation is not observed on copper lines after the corrosion stress when the sample is protected by a 10 nm thick laminate C (Fig. 5b). In all likelihood, the integrity of the barrier is not affected by the topology of the surface, owing to the excellent conformality of the ALD process [38]. Therefore, using a plasma pretreatment to enhance the adhesion properties of the capping layer on the hybrid polymer–copper interface, should not represent a reliability risk.



(a) (b) (c) (d)

Figure 5: Capping layer resistance to corrosion was assessed using a dual stage stress (TH stress followed by HTS). a) and d) At the end of the sequence, traces of oxidation were found on lines protected with laminate B and E, evidencing their susceptibility to corrosion. b) and c) Laminate C and D were not found to be sensitive to corrosion by moisture.

Finally, Fig. 6 displays FIB cross-sections of the metal lines performed after TC stress. Oxidation of the line is not observed at the end of the stress regardless of the laminate type, when its thickness is above 8 nm (Fig. 6a). This suggests that the integrity of the barrier is not affected by the thermal cycles as the presence of cracks or pin holes in the capping layer would have resulted in copper oxidation. In addition, using a plasma pretreatment does not induce



(a) (b)

Figure 6: After 1000 cycles of TC stress, oxidation is not detected on top of copper lines protected by capping layer thicker than 8 nm regardless of the presence of a plasma pretreatement. a) No pretreatment applied before capping deposition. b) Plasma pretreatment performed.

higher reliability risks as shown in Fig. 6b.

4. Conclusion

Ultra-thin inorganic/organic vapor deposited layers processed at a temperature below or equal to 100 °C have been employed in a polymer-based RDL technology to prevent copper oxidation. The presence of a capping layer as thin as 8 nm on top of the metal lines fully protects from oxidation during high temperature storage stresses. Additionally, some of these thin layers have demonstrated resistance toward moisture-based corrosion while no reliability issues have been observed during thermal cycling stresses, paving the way to their integration in polymer-based RDL technologies.

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Declaration of interests

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

References

[1] J. H. Lau, Fan-Out Wafer-Level Packaging, Springer Singapore, 2018. `doi:10.1007/978-981-10-8884-1`.

[2] W. W. Flack, R. Hsieh, H.-A. Nguyen, J. Slabbekoorn, C. Lorant, A. Miller, One micron redistribution for fan-out wafer level packaging, in: Electronics Packaging Technology Conference (EPTC), IEEE, 2017, pp. 1–7. `doi:10.1109/eptc.2017.8277536`.

[3] W. W. Flack, R. Hsieh, H.-A. Nguyen, J. Slabbekoorn, S. Suhard, A. Miller, A. Hiro, R. Ridremont, One micron damascene redistribution for fan-out wafer level packaging using a photosensitive dielectric material, in: Electronics Packaging Technology Conference (EPTC), IEEE, 2018, pp. 395–400. `doi:10.1109/eptc.2018.8654363`.

[4] E. Chery, J. Slabbekoorn, N. Pinho, A. Miller, E. Beyne, Advances in photosensitive polymer based damascene RDL processes: Toward submicrometer pitches with more metal layers, in: Electronic Components and Technology Conference (ECTC), 2021, pp. 340–346. `doi:10.1109/ECTC32696.2021.00064`.

[5] H. Lee, J. Yu, Study on the effects of copper oxide growth on the peel strength of copper/polyimide, Journal of Electronic Materials 37 (8) (2008) 1102–1110. `doi:10.1007/s11664-007-0317-z`.

[6] H. Noma, K. Okamoto, K. Toriyama, H. Mori, HAST failure investigation on ultra-high density lines for 2.1D packages, in: International Conference on Electronic Packaging and iMAPS All Asia Conference (ICEP-IAAC), IEEE, 2015, pp. 161–165. `doi:10.1109/icep-iaac.2015.7111020`.

[7] Y. Shoji, H. Araki, Y. Koyama, Y. Masuda, K. Hashimoto, K. Isobe, R. Okuda, M. Tomikawa, Higher reliability for low-temperature curable positive-tone photosensitive dielectric materials, in: CPMT Symposium Japan (ICSJ), IEEE, 2017, pp. 103–106. `doi:10.1109/icsj.2017.8240099`.

[8] C.-L. Liang, Y.-S. Lin, C.-L. Kao, D. Tarng, S.-B. Wang, Y.-C. Hung, K.-L. Lin, Electromigration failure study of a fine-pitch 2 µm/2 µm L/S Cu redistribution line embedded in polyimide for advanced high-density fan-out packaging, in: Electronic Components and Technology Conference (ECTC), 2020, pp. 361–366.

[9] E. Chery, F. F. C. Duval, M. Stucchi, J. Slabbekoorn, K. Croes, E. Beyne, Photosensitive polymer reliability for fine pitch RDL applications, in: Electronic Components and Technology Conference (ECTC), 2020, pp. 1234–1240, iSSN: 2377-5726. `doi:10.1109/ECTC32862.2020.00197`.

[10] M. O'Reilly, X. Jiang, J. T. Beechinor, S. Lynch, C. NíDheasuna, J. C. Patterson, G. M. Crean, Investigation of the oxidation behaviour of thin film and bulk copper, Applied Surface Science 91 (1) (1995) 152–156. `doi:10.1016/0169-4332(95)00111-5`.
URL `https://www.sciencedirect.com/science/article/pii/0169433295001115`

[11] C. Zhong, Y.-M. Jiang, D.-M. Sun, J. Gong, B. Deng, S. Cao, J. Li, Oxidation kinetics of nanoscale copper thin films at low temperature characterized by sheet resistance and optical transmittance, Chinese Journal of Physics 47 (3) (2009) 253–260.

[12] S. Choudhary, J. V. N. Sarma, S. Pande, S. Ababou-Girard, P. Turban, B. Lepine, S. Gangopadhyay, Oxidation mechanism of thin Cu films: A gateway towards the formation of single oxide phase, AIP Advances 8 (5) (2018) 055114. `doi:10.1063/1.5028407`.
URL `https://aip.scitation.org/doi/10.1063/1.5028407`

[13] N. Cabrera, N. F. Mott, Theory of the oxidation of metals, Reports on Progress in Physics 12 (1) (1949) 163–184. `doi:10.1088/0034-4885/12/1/308`.
URL `https://doi.org/10.1088%2F0034-4885%2F12%2F1%2F308`

[14] J. C. Yang, B. Kolasa, J. M. Gibson, M. Yeadon, Self-limiting oxidation of copper, Applied Physics Letters 73 (19) (1998) 2841–2843. `doi:10.1063/1.122608`.

[15] Y. S. Chu, I. K. Robinson, A. A. Gewirth, Comparison of aqueous and native oxide formation on Cu(111), The Journal of Chemical Physics 110 (12) (1999) 5952–5959. `doi:10.1063/1.478495`.
URL `https://aip.scitation.org/doi/abs/10.1063/1.478495`

[16] M. Ronay, P. Nordlander, Barrier to oxygen penetration on metal and oxide surfaces, Physical Review B 35 (17) (1987) 9403–9406. `doi:10.1103/PhysRevB.35.9403`.
URL `https://link.aps.org/doi/10.1103/PhysRevB.35.9403`

[17] S. Suzuki, Y. Ishikawa, M. Isshiki, Y. Waseda, Native Oxide Layers Formed on the Surface of Ultra High-Purity Iron

and Copper Investigated by Angle Resolved XPS, Materials Transactions, JIM 38 (11) (1997) 1004–1009. `doi:10.2320/matertrans1989.38.1004`.

[18] E. Chery, F. F. C. Duval, M. Stucchi, J. Slabbekoorn, K. Croes, E. Beyne, Reliability Study of Polymers Used in Sub-4-μm Pitch RDL Applications, IEEE Transactions on Components, Packaging and Manufacturing Technology 11 (7) (2021) 1073–1080. `doi:10.1109/TCPMT.2021.3079515`.

[19] G. L. Schnable, W. Kern, R. B. Comizzoli, Passivation Coatings on Silicon Devices, Journal of The Electrochemical Society 122 (8) (1975) 1092. `doi:10.1149/1.2134402`.
URL `https://iopscience.iop.org/article/10.1149/1.2134402/meta`

[20] R. B. Comizzoli, L. K. White, W. Kern, G. L. Schnable, D. A. Peters, C. E. Tracy, R. D. Vibronek, Corrosion of Aluminum IC Metallization with Defective Surface Passivation Layer, in: International Reliability Physics Symposium, 1980, pp. 282–292, iSSN: 0735-0791. `doi:10.1109/IRPS.1980.362955`.

[21] T. Wada, M. Sugimoto, T. Ajiki, The Influence of Passivation Layer on Aluminum Corrosion on Simulated Microelectronics Circuit Pattern, Journal of The Electrochemical Society 136 (3) (1989) 732. `doi:10.1149/1.2096720`.
URL `https://iopscience.iop.org/article/10.1149/1.2096720/meta`

[22] H. Miyazaki, H. Kojima, K. Hinode, Passivation effect of silicon nitride against copper diffusion, Journal of Applied Physics 81 (12) (1997) 7746–7750. `doi:10.1063/1.365380`.

[23] K. Prasad, X. Yuan, C. Li, R. Kumar, Evaluation of diffusion barrier layers in Cu interconnects, in: Conference on Optoelectronic and Microelectronic Materials and Devices, 2002, pp. 373–376, iSSN: 1097-2137. `doi:10.1109/COMMAD.2002.1237268`.

[24] K. Goto, H. Yuasa, A. Andatsu, M. Matsuura, Film Characterization of Cu diffusion barrier dielectrics for 90 nm and 65 nm technology node Cu interconnects, in: International Interconnect Technology Conference, 2003, pp. 6–8. `doi:10.1109/IITC.2003.1219696`.

[25] M. Vilmay, D. Roy, F. Volpi, J. M. Chaix, Characterization of low-k SiOCH dielectric for 45nm technology and link between the dominant leakage path and the breakdown localization, Microelectronic Engineering 85 (10) (2008) 2075–2078. `doi:10.1016/j.mee.2008.04.045`.
URL `https://www.sciencedirect.com/science/article/pii/S0167931708002463`

[26] L. Zhao, M. Lofrano, K. Croes, E. V. Besien, Z. Tőkei, C. J. Wilson, R. Degraeve, T. Kauerauf, G. P. Beyer, C. Claeys, Evaluations of intrinsic time dependent dielectric breakdown of dielectric copper diffusion barriers, Thin Solid Films 520 (1) (2011) 662–666. `doi:10.1016/j.tsf.2011.08.073`.

[27] C. Byrne, B. Brennan, A. P. McCoy, J. Bogan, A. Brady, G. Hughes, In situ XPS chemical analysis of $MnSiO_3$ copper diffusion barrier layer formation and simultaneous fabrication of metal oxide semiconductor electrical test MOS structures, ACS Applied Materials & Interfaces 8 (4) (2016) 2470–2477. `doi:10.1021/acsami.5b08044`.

[28] K. Chattopadhyay, B. Schravendijk, T. Mountsier, G. Alers, M. Hornbeck, H. Wu, R. Shaviv, G. Harm, D. Vitkavage, E. Apen, Y. Yu, R. Havemann, In-situ formation of a copper silicide cap for TDDB and electromigration improvement, in: International Reliability Physics Symposium Proceedings, IEEE, 2006, pp. 128–130. `doi:10.1109/relphy.2006.251203`.

[29] T. Nogami, J. Maniscalco, A. Madan, P. Flaitz, P. DeHaven, C. Parks, L. Tai, B. S. Lawrence, R. Davis, R. Murphy, T. Shaw, S. Cohen, C.-K. Hu, C. Cabral, S. Chiang, J. Kelly, M. Zaitz, J. Schmatz, S. Choi, K. Tsumura, C. Penny, H.-C. Chen, D. Canaperi, T. Vo, F. Ito, O. Straten, A. Simon, S.-H. Rhee, B.-Y. Kim, T. Bolom, V. Ryan, P. Ma, J. Ren, J. Aubuchon, J. Fine, P. Kozlowski, T. Spooner, D. Edelstein, CVD Co and its application to Cu damascene interconnections, in: International Interconnect Technology Conference (IITC), 2010, pp. 1–3, iSSN: 2380-6338. `doi:10.1109/IITC.2010.5510584`.

[30] C.-C. Yang, F. Baumann, P.-C. Wang, S. Lee, P. Ma, J. AuBuchon, D. Edelstein, Characterization of Copper Electromigration Dependence on Selective Chemical Vapor Deposited Cobalt Capping Layer Thickness, IEEE Electron Device Letters 32 (4) (2011) 560–562. `doi:10.1109/LED.2011.2108260`.

[31] C.-C. Yang, B. Li, H. Shobha, S. Nguyen, A. Grill, W. Ye, J. AuBuchon, M. Shek, D. Edelstein, In Situ Co/SiC(N,H) Capping Layers for Cu/Low- k Interconnects, IEEE Electron Device Letters 33 (4) (2012) 588–590. `doi:10.1109/LED.2012.2183850`.

[32] A. P. Ghosh, L. J. Gerenser, C. M. Jarman, J. E. Fornalik, Thin-film encapsulation of organic light-emitting devices, Applied Physics Letters 86 (22) (2005) 223503. `doi:10.1063/1.1929867`.
URL `https://aip.scitation.org/doi/10.1063/1.1929867`

[33] M. D. Groner, S. M. George, R. S. McLean, P. F. Carcia, Gas diffusion barriers on polymers using Al_2O_3 atomic layer deposition, Applied Physics Letters 88 (5) (2006) 051907. `doi:10.1063/1.2168489`.
URL `https://aip.scitation.org/doi/full/10.1063/1.2168489`

[34] J. Meyer, D. Schneidenbach, T. Winkler, S. Hamwi, T. Weimann, P. Hinze, S. Ammermann, H.-H. Johannes, T. Riedl, W. Kowalsky, Reliable thin film encapsulation for organic light emitting diodes grown by low-temperature atomic layer deposition, Applied Physics Letters 94 (23) (2009) 233305. `doi:10.1063/1.3153123`.
URL `https://aip.scitation.org/doi/full/10.1063/1.3153123`

[35] H. Klumbies, P. Schmidt, M. Hähnel, A. Singh, U. Schroeder, C. Richter, T. Mikolajick, C. Hoßbach, M. Albert, J. W. Bartha, K. Leo, L. Müller-Meskamp, Thickness dependent barrier performance of permeation barriers made from atomic layer deposited alumina for organic devices, Organic Electronics 17 (2015) 138–143. `doi:10.1016/j.orgel.2014.12.003`.
URL `https://www.sciencedirect.com/science/article/pii/S1566119914005515`

[36] Y. Li, Y. Xiong, H. Yang, K. Cao, R. Chen, Thin film encapsulation for the organic light-emitting diodes display via atomic layer deposition, Journal of Materials Research 35 (7) (2020) 681–700. `doi:10.1557/jmr.2019.331`.

[37] S. M. George, Atomic Layer Deposition: An Overview, Chemical Reviews 110 (1) (2010) 111–131. `doi:10.1021/cr900056b`.
URL `https://doi.org/10.1021/cr900056b`

[38] V. Cremers, R. L. Puurunen, J. Dendooven, Conformality in atomic layer deposition: Current status overview of analysis and modelling, Applied Physics Reviews 6 (2) (2019) 021302. `doi:10.1063/1.5060967`.
URL `https://aip.scitation.org/doi/full/10.1063/1.5060967`

[39] J. Meyer, P. Görrn, F. Bertram, S. Hamwi, T. Winkler, H.-H. Johannes, T. Weimann, P. Hinze, T. Riedl, W. Kowalsky, Al_2O_3/ZrO_2 Nanolaminates as Ultrahigh Gas-Diffusion Barriers—A Strategy for Reliable Encapsulation of Organic Electronics, Advanced Materials 21 (18) (2009) 1845–1849. `doi:10.1002/adma.200803440`.
URL `https://onlinelibrary.wiley.com/doi/abs/10.1002/adma.200803440`

[40] A. A. Dameron, S. D. Davidson, B. B. Burton, P. F. Carcia, R. S. McLean, S. M. George, Gas Diffusion Barriers on Polymers Using Multilayers Fabricated by Al_2O_3 and Rapid SiO_2 Atomic Layer Deposition, The Journal of Physical Chemistry C 112 (12) (2008) 4573–4580. `doi:10.1021/jp076866+`.
URL `https://doi.org/10.1021/jp076866+`

[41] J. Meyer, H. Schmidt, W. Kowalsky, T. Riedl, A. Kahn, The origin of low water vapor transmission rates through Al_2O_3/ZrO_2 nanolaminate gas-diffusion barriers grown by atomic layer deposition, Applied Physics Letters 96 (24) (2010) 243308. `doi:10.1063/1.3455324`.
URL `https://aip.scitation.org/doi/full/10.1063/1.3455324`

[42] M. D. Groner, F. H. Fabreguette, J. W. Elam, S. M. George, Low-Temperature Al_2O_3 Atomic Layer Deposition, Chemistry of Materials 16 (4) (2004) 639–645. `doi:10.1021/cm0304546`.

URL `https://doi.org/10.1021/cm0304546`

[43] P. F. Carcia, R. S. McLean, M. H. Reilly, Permeation measurements and modeling of highly defective Al_2O_3 thin films grown by atomic layer deposition on polymers, Applied Physics Letters 97 (22) (2010) 221901. `doi:10.1063/1.3519476`.
URL `https://aip.scitation.org/doi/full/10.1063/1.3519476`

[44] L. H. Kim, K. Kim, S. Park, Y. J. Jeong, H. Kim, D. S. Chung, S. H. Kim, C. E. Park, Al_2O_3/TiO_2 Nanolaminate Thin Film Encapsulation for Organic Thin Film Transistors via Plasma-Enhanced Atomic Layer Deposition, ACS Applied Materials & Interfaces 6 (9) (2014) 6731–6738. `doi:10.1021/am500458d`.
URL `https://doi.org/10.1021/am500458d`

[45] M.-H. Tseng, H.-H. Yu, K.-Y. Chou, J.-H. Jou, K.-L. Lin, C.-C. Wang, F.-Y. Tsai, Low-temperature gas-barrier films by atomic layer deposition for encapsulating organic light-emitting diodes, Nanotechnology 27 (29) (2016) 295706. `doi:10.1088/0957-4484/27/29/295706`.
URL `https://doi.org/10.1088%2F0957-4484%2F27%2F29%2F295706`

[46] A. I. Abdulagatov, Y. Yan, J. R. Cooper, Y. Zhang, Z. M. Gibbs, A. S. Cavanagh, R. G. Yang, Y. C. Lee, S. M. George, Al_2O_3 and TiO_2 Atomic Layer Deposition on Copper for Water Corrosion Resistance, ACS Applied Materials & Interfaces 3 (12) (2011) 4593–4601. `doi:10.1021/am2009579`.
URL `https://doi.org/10.1021/am2009579`

[47] A. Bulusu, H. Kim, D. Samet, S. Graham, Improving the stability of atomic layer deposited alumina films in aqueous environments with metal oxide capping layers, Journal of Physics D: Applied Physics 46 (8) (2013) 084014. `doi:10.1088/0022-3727/46/8/084014`.
URL `https://doi.org/10.1088/0022-3727/46/8/084014`

[48] A. J. Ben-Sasson, G. Ankonina, M. Greenman, M. T. Grimes, N. Tessler, Low-temperature molecular vapor deposition of ultrathin metal oxide dielectric for low-voltage vertical organic field effect transistors, ACS Applied Materials & Interfaces 5 (7) (2013) 2462–2468. `doi:10.1021/am3026773`.

[49] D. Nečas, P. Klapetek, Gwyddion: an open-source software for SPM data analysis, Open Physics 10 (1). `doi:10.2478/s11534-011-0096-2`.

[50] AEC - Q100 Rev - H: Failure Mechanism Based Stress Test Qualification For Integrated Circuits, Automotive Electronics Council.
URL `http://aecouncil.com/Documents/AEC_Q100_Rev_H_Base_Document.pdf`

[51] Z. Chai, Y. Liu, J. Li, X. Lu, D. He, Ultra-thin Al_2O_3 films grown by atomic layer deposition for corrosion protection of copper, RSC Adv. 4 (92) (2014) 50503–50509. `doi:10.1039/c4ra09179e`.

[52] A. K. Singh, K. Adstedt, B. Brown, P. M. Singh, S. Graham, Development of ALD Coatings for Harsh Environment Applications, ACS Applied Materials & Interfaces 11 (7) (2019) 7498–7509. `doi:10.1021/acsami.8b11557`.
URL `https://doi.org/10.1021/acsami.8b11557`