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The Impact of Width Downscaling on the High-Frequency Characteristics of InGaAs Nanowire FETs

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ABSTRACT This work demonstrates the high-frequency characteristics of $In_{0.53}Ga_{0.47}As$ nanowire with scaled wire width by implementing TCAD simulations. The physical models and correlated parameters have been calibrated to the experiments (Ko et al., 2022). As the width of the nanowire is scaled to 10 nm, the electron density peaks are no longer located close to the oxide/semiconductor interface. Instead, the peaks merge and volume inversion effects appear due to the strong quantum confinement. The volume inversion effects lead to higher cut-off frequency due to the reduced total transport delay time. To have a better understanding of this phenomena, the high-frequency properties of nanowire were quantified with the assistance of small-signal analysis and delay time analysis using TCAD. It is found that the channel charging delay increases with narrower wire width due to the raise of source/drain resistance. Regarding the extrinsic and intrinsic delay, they increase with smaller wire width and drop at width of 10 nm due to the volume inversion effects. Electron distribution which aims to clarify the above-mentioned observation is also plotted.

INDEX TERMS III-V semiconductor materials, MOSFET, high-k gate dielectrics, cutoff frequency, TCAD.

I. INTRODUCTION

The development of high-frequency transistors based on III-V materials, which possess outstanding properties such as high electron mobility and high injection velocity [1], [2], [3], has made significant advances in the past 20 years. From sub-THz GaAs-based [4] to THz domain InP-based [5] high electron mobility transistors (HEMTs), the III-V devices have been extensively used in the high-frequency applications. However, the complexity of the epi structure and fabrication process makes the III-V HEMTs difficult to be integrated with commercial Si CMOS technology for system on a chip (SOC) applications. Therefore, a surface channel device with CMOS compatible process emerges to be necessary. For the surface channel transistors, the high-frequency properties have been greatly improved by scaling down the effective channel length (L_{eff}) due to the reduced spacing from the source edge to the drain [6] and [7]. Unfortunately, the benefits are deteriorated by the short channel effects (SCEs) such as large subthreshold swing (SS), drain induced barrier lowering (DIBL) and threshold voltage roll-off. To keep scaling the device channel length while maintaining gate control, multi-gate field-effect transistors (MuFETs) such as FinFETs, nanowire and nanosheet with high-κ dielectric are implemented [8], [9], [10], [11] due to their higher area-to-volume ratio and thus good immunity to the SCEs. The gate control can be further enhanced by scaling down the width of the transistors [12] and [13]. An additional benefit of

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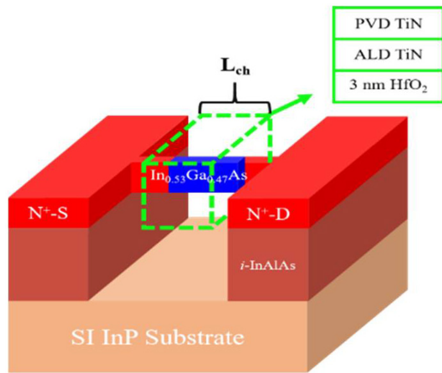

FIGURE 1. Device structure of $In_{0.53}Ga_{0.47}As$ nanowire. The composition of gate stack is also shown.

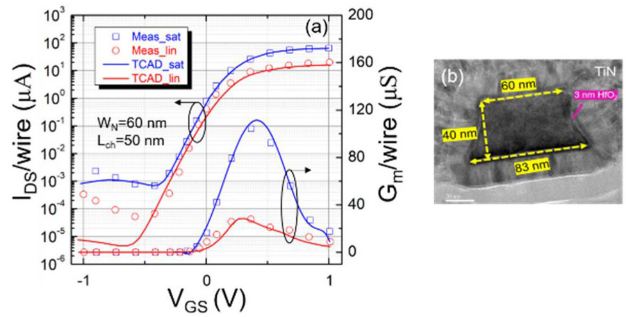

FIGURE 2. (a) I_{DS}-V_{GS} and G_m-V_{GS} measurement results per nanowire and fitting results from TCAD simulations at L_{ch} = 50 nm, W_N = 60 nm at linear (V_{DS} = 0.05 V) and saturation (V_{DS} = 0.5 V) region. (b) TEM image of the device structure, which shows wire top width of 60 nm, InGaAs thickness of 40 nm and HfO_2 of 3 nm.

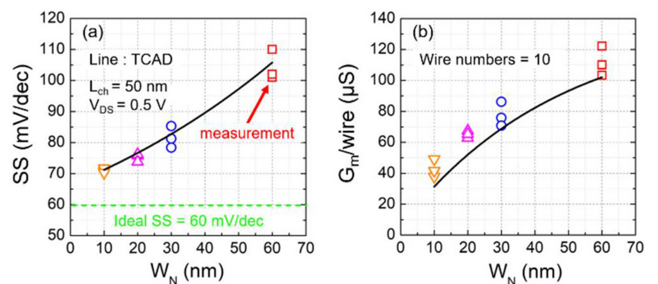

FIGURE 3. Scaling matrix of (a) minimum SS, and (b) peak G_m per wire. The TCAD fitting results demonstrate the accuracy of device models with width scaling.

scaling down the width is the reduction of power consumption. However, the high-frequency properties can be dramatically sacrificed in devices with smaller width [14]. So far, there are several research works demonstrating the high-frequency properties of InGaAs MuFETs [15], [16], [17], [18] from the results of experiments and the circuit simulations. Nevertheless, there are less research work discussing about the impact of device width on the high-frequency properties of the InGaAs transistors especially for widths down to merely 10 nm. In this work, we demonstrate the impact of scaled width on the high-frequency properties of $In_{0.53}Ga_{0.47}As$ nanowire with the assistance of TCAD simulations. The DC properties have been calibrated to the experiments carried out on devices [19] with a good agreement while the high-frequency properties are simulated with the help of small-signal analysis of the device admittance (Y). Our attention is focus on the device cut-off frequency (f_T) since it is directly related to the intrinsic transistor properties. The strong quantum effects in very small device dimension are also taken into consideration. It is found that the nanowire width scaling is necessary to suppress the SCEs and that the overall transport delay can be improved when the device width is scaled to 10 nm. Therefore, the high-frequency properties can be less sacrificed.

II. DEVICE STRUCTURE AND SIMULATIONS SET-UP

The device structure for fabrication and simulation is shown in Fig. 1 and the details of the fabrication process can be referenced elsewhere [11], [20]. The 3-nm HfO_2 gate dielectric was deposited using atomic layer deposition (ALD) technique and followed by post remote-plasma (NH_3/N_2) treatment [21], [22], [23]. A thin ALD-TiN and physical vapor deposition (PVD) TiN were deposited as gate metal.

To investigate the high-frequency properties, the DC simulations were carefully fitted to the experiments in the literature [19]. The fitting results based on the DC measurements of the transfer characteristics of the device biased at drain to source voltage (V_{DS}) at linear (0.05 V) and saturation (0.5 V) regions and the transmission electron microscope (TEM) image of the nanowire are shown in Fig. 2(a) and (b). The device channel length (L_{ch}) is 50 nm while the top width (W_N) and thickness (T_N) are 60 nm and 40 nm, respectively. The simulated results show excellent agreement with measurements reported in reference [19]. As for the physical models, Fermi-Dirac statistics is applied. Density gradient is used for the quantum corrections. Impurities scattering, phonon scattering and surface roughness scattering are considered by applying the Inversion and Accumulation Layer (IAL) mobility model. The Coulomb scattering induced by interface traps is also considered. The conduction band non-parabolicity and multi-valley models are also taken into consideration. The subthreshold and off-state properties are captured by Shockley-Read-Hall, Auger recombination and Hurkx band-to-band tunneling models. The doping profile and the mobility models have been carefully calibrated to the planar configuration as shown in [24]. Though the device configuration is different, with a slight modification of the mobility models we can achieve at good fitting results. Critical parameters used for calibration are shown in Table 1. It is worth noting that default parameters are used if not reported in the Table. The number of mid-gap traps is relatively high due to non-optimized interfacial treatment. The interface quality can be further improved by changing the species of the plasma or the insertion of interfacial layers.

Fig. 3 shows the accuracy of the applied physical models with scaled width for (a) minimum SS versus W_N

TABLE 1. Parameters for TCAD Calibration.

Symbol	Quantity	Value
μ_{imp}	impurities scattering mobility	7581 cm²/V·s at low doping[1] 4041 cm²/V·s at medium doping[2] 1815 cm²/V·s at high doping[3]
δ	surface roughness scattering mobility	1×10^{14} cm²/V·s
V_{sat}	saturation velocity	3.2×10^{7} cm/s
ρ_c	contact resistivity	5×10^{-6} Ω-cm²
γ	quantum correction	1.776
D_{it}	mid-gap traps	5.88×10^{12} cm^{-2} eV^{-1}
ϕ_m	metal work function	4.88 eV

[1] 1×10^{17} cm^{-3}, [2] 1×10^{18} cm^{-3}, [3] 1×10^{19} cm^{-3}

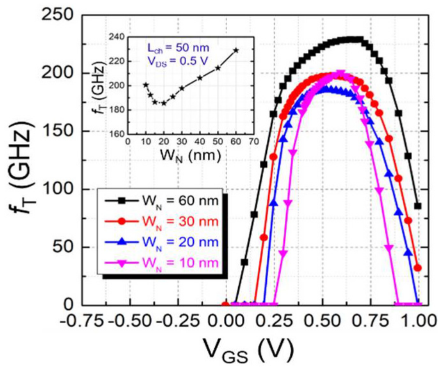

FIGURE 4. Cut-off frequency of InGaAs nanowire with scaled wire width. Inset shows the peak value of f_T following width shrinkage. More points are simulated to show a clear tendency of the f_T with scaled width.

and (b) peak G_m per wire versus W_N. The measurement data of three device is taken for each width. From the plots, the good agreement between the experiments carried out on devices and simulation results is observed. Based on the successful prediction of scaling tendency, we can extend to the high-frequency domain with the assistance of small-signal AC simulations.

III. RESULTS AND DISCUSSIONS

Fig. 4 presents the device cut-off frequency (f_T) as a function of the V_{GS}, calculated from the small-signal admittance (Y) at $L_{ch} = 50$ nm and $V_{DS} = 0.5$ V with various wire widths. f_T is the frequency where the device current gain degrades to 0 dB. To avoid the high-frequency distortion that might affect our extracted f_T, a -20 dB/dec extraction methodology is implemented. The peak f_T of the device is shown to be 229 GHz with $W_N = 60$ nm. From Fig. 4 we see that f_T degrades from $W_N = 60$ nm to $W_N = 20$ nm, while from $W_N = 20$ nm to $W_N = 10$ nm, the f_T raises to an even higher value than $W_N = 30$ nm. Inset shows the peak f_T versus various W_N. More data points from the simulations have been provided to show a clear tendency of f_T as a function of wire width.

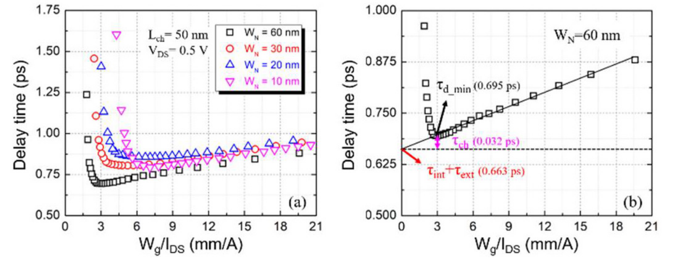

FIGURE 5. Total delay time (τ_d) versus W_g/I_{DS} with scaled nanowire width at $L_{ch} = 50$ nm, $V_{DS} = 0.5$ V. (b) Zoom in of Fig. 5 (a) with $W_N = 60$ nm and the extraction of $\tau_{int} + \tau_{ext}$ and τ_{ch}.

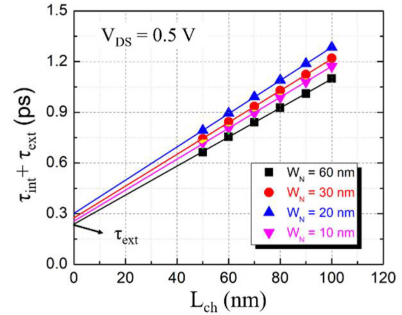

FIGURE 6. Extraction of τ_{ext} of different nanowire width in according to the channel length.

To further understand the mechanisms, we analyzed the delay time of the nanowire based on [25] and [26]. Fig. 5(a) shows the total delay time (τ_d) versus the reciprocal of the drain current density (W_g/I_{DS}) with different wire widths. W_g is the perimeter of the gate, defined as $2(W_N + T_N)$. The formula of τ_d is as shown in [26]:

$$\tau_d = 1/(2 \times \pi \times f_T) = \tau_{int} + \tau_{ext} + \tau_{ch}. \quad (1)$$

where τ_{int}, τ_{ext} and τ_{ch} are the intrinsic, extrinsic and channel charging delay, respectively. The sum of intrinsic and extrinsic delay ($\tau_{int} + \tau_{ext}$) can be extracted by extrapolating the linear curve, which passes through the minimum total delay (τ_{d_min}), to the intercept of infinite drain current density as shown in Fig. 5(b). τ_{ch} is the difference between τ_{d_min} and $\tau_{int} + \tau_{ext}$. The total delay time is high in lower drain current density because of the low conductance in the channel. In high drain current density, the total delay time increases due to the degradation of transconductance and the extraction method is no longer applicable.

The value of extrinsic delay is extracted from the linear extrapolation of $\tau_{int} + \tau_{ext}$ according to the channel length as shown in Fig. 6. When the channel length is reduced to 0 nm, the intrinsic delay no longer exists and there remains only the extrinsic delay.

The extracted delay time components are shown in Fig. 7, in which we notice that the intrinsic delay and extrinsic delay increase with reduced wire width but drop at 10 nm. On the other hand, the channel charging delay increases monotonously with narrower wire width. Paying attention to delay components of widths 10 nm and 20 nm in Fig. 7,

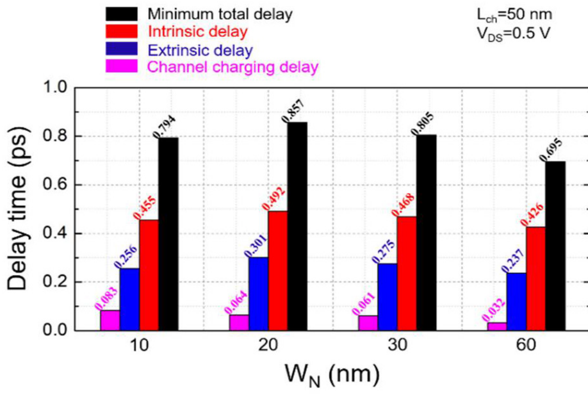

FIGURE 7. Components of the InGaAs nanowire delay time including minimum total delay (τ_{d-min}), intrinsic delay (τ_{int}), extrinsic delay (τ_{ext}) and channel charging delay (τ_{ch}) with different wire width.

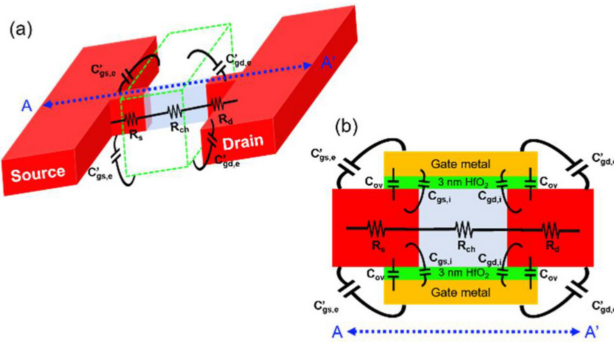

FIGURE 8. (a) Components that lead to the transport delay of InGaAs nanowire. Substrate effects are excluded in this paper. (b) Cross-section view of (a) cut in the A-A' direction.

we can observe that the decreases of intrinsic and extrinsic delays are larger than the increase of channel charging delay when we move from 20 nm to 10 nm. This is the reason why there is an increase in the f_T at 10 nm.

The sketch of the components that contribute to the transport delay of the device are shown in Fig. 8 (a) and (b). $C'_{gs,e}$ and $C'_{gd,e}$ are the extrinsic gate-to-source and gate-to-drain capacitances, $C_{gs,i}$ and $C_{gd,i}$ are the intrinsic gate-to-source and gate-to-drain capacitances, C_{ov} is the overlap capacitance, R_s is the source resistance, R_{ch} is the channel resistance and R_d is the drain resistance.

From reference [26], the intrinsic, extrinsic and channel charging delay are shown in eqs. (2)-(10):

$$\tau_{int} = (C_{gs,i} + C_{gd,i})/g_{m,i}. \quad (2)$$

$$\tau_{ext} = (C_{gs,e} + C_{gd,e})/g_{m,i}. \quad (3)$$

$$\tau_{ch} = (R_s + R_d) \times [C_{gd} + (C_{gs} + C_{gd}) \times (g_{sd}/g_{m,i})] \quad (4)$$

$$C_{gs,e} = C'_{gs,e} + C_{ov} \quad (5)$$

$$C_{gd,e} = C'_{gd,e} + C_{ov} \quad (6)$$

$$C_{gs} = C_{gs,i} + C_{gs,e} \quad (7)$$

$$C_{gd} = C_{gd,i} + C_{gd,e} \quad (8)$$

$$g_{sd} = \partial I_{DS}/\partial V_{DS} \quad (9)$$

$$C_{gg,i} = C_{gs,i} + C_{gd,i} \quad (10)$$

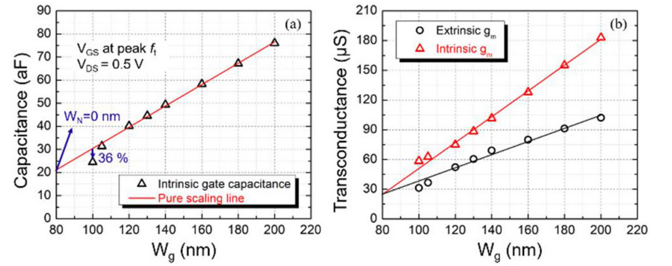

FIGURE 9. (a) Intrinsic gate capacitance ($C_{gg,i}$) and trendline proportional to the gate perimeter (W_g) of the nanowire. (b) Extrinsic and intrinsic peak transconductance according to the W_g of the nanowire. The black and red solid curves are trendlines proportional to W_g.

where $g_{m,i}$ is the intrinsic transconductance, $C_{gs,e}$ and $C_{gd,e}$ are the extrinsic gate-to-source and gate-to-drain capacitances. C_{gs} and C_{gd} are the overall gate-to-source and gate-to-drain capacitances, respectively. g_{sd} is the output conductance and $C_{gg,i}$ is the intrinsic gate capacitance. $C_{gs,i}$, $C_{gd,i}$, $g_{m,i}$ and R_{ch} can be obtained by de-embedding the parasitic components of the transistors (including extrinsic capacitance, R_s and R_d). These components are extracted when the device is in the cold-FET state ($V_{DS} = 0$ V). The extraction methodology can be referred to [27] while the de-embedding process can be referred to [28].

For the intrinsic delay, the values of $C_{gg,i}$ are shown in Fig. 9(a). It is very clear that the intrinsic gate capacitance at 100 nm gate perimeter does not follow the trendline (pure scaling) proportional to the scaling of capacitance due to total gate perimeter. The gap between the pure scaling line and the $C_{gg,i}$ is broaden with narrower W_g. There is a 36 % decrease of $C_{gg,i}$ compared to the pure scaling line at $W_g = 100$ nm (W_N is 10 nm) due to the volume inversion effects [29]. Fig. 9(b) shows the comparison of extrinsic transconductance ($g_{m,e}$) and the intrinsic transconductance where their relationship is shown in eq. (11) from reference [30].

$$g_{m,i} = g_{m,e}/[1 - g_{m,e} \times Rs - g_{sd} \times (R_s + R_d)] \quad (11)$$

The intrinsic transconductance show nearly twice of the extrinsic transconductance due to the exclusion of the source/drain resistance. The source/drain resistance are extracted from the voltage drop in the source/drain region. It is very interesting to notice that the intrinsic transconductance degrades at a slower rate than gate perimeter scaling at smaller W_g, which is opposite to the behavior of extrinsic transconductance. The phenomenon is due to the reduced carrier scattering in the inversion channel and the improvement of the effective mobility [29], [31] and [32] from volume inversion effects. However, these benefits are hidden when the source/drain resistance are considered.

This phenomenon can be investigated through the electron distribution in Fig. 10. The 2D cross-section view shown in Fig. 10 (a) is a cut plane in the middle of the channel and the direction is perpendicular to the current flow. The 1D electron density distribution cut in the A-A' direction is shown in Fig. 10 (b). The electron density has been normalized to the peak value of $W_N = 10$ nm. Due to

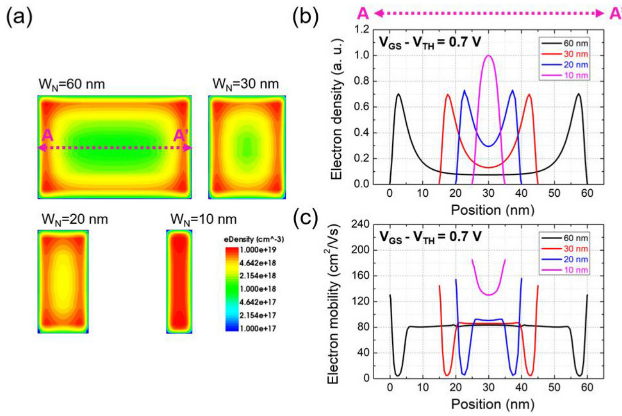

FIGURE 10. (a) 2D cut of electron distribution cut right in the middle of channel and perpendicular to the current flow with different wire width. (b) normalized 1D electron density with different nanowire width cut along A-A' direction. (c) 1D electron mobility distribution with different nanowire width cut along A-A' direction.

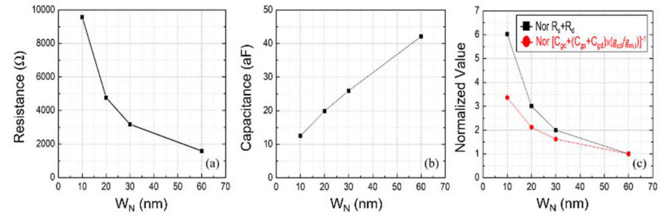

FIGURE 11. (a) $R_s + R_d$ for different wire widths. (b) The capacitive components that affect to the channel charging delay with different wire width. (c) The comparison between normalized $R_s + R_d$ and $[C_{gd} + (C_{gs} + C_{gd}) \times (g_{sd}/g_{m,i})]^{-1}$ with different wire width.

the enhancement of quantum effects with scaled width, the electrons are pushed away from the oxide/semiconductor interface and finally merge at the center, this is referred as the volume inversion effect. This effect results in the increase of capacitance equivalent thickness (CET) and thus a drop of $C_{gg,i}$ [33]. Fig. 10 (c) shows the electron mobility (μ_e) distribution cut in the A-A' direction. Obviously, the electron mobility at $W_N = 10$ nm shows the highest value. Since the channel carriers are pushed away from the interface, the surface roughness scattering effects and the interface traps scattering effects are mitigated. These can be used to describe the tendency of intrinsic transconductance that we observed in Fig. 9(b).

As for the extrinsic delay, Fig. 7 shows that the extrinsic delay component follows the same trend as the intrinsic delay. This behavior is related to same mechanism of volume inversion effects previously described for the intrinsic delay. Since there is an overlap region in the nanowire (Fig. 8b), it also suffers from the quantum confinement effects from the gate dielectric. The volume inversion also occurs at these overlap regions.

For the channel charging delay, equation (4), the value of $R_s + R_d$ is shown in Fig. 11(a) while the term including capacitive components $[C_{gd} + (C_{gs} + C_{gd}) \times (g_{sd}/g_{m,i})]$ is shown in Fig. 11(b). The device suffers from huge S/D series resistance when the dimension is scaled. The $R_s + R_d$ and $[C_{gd} + (C_{gs} + C_{gd}) \times (g_{sd}/g_{m,i})]^{-1}$ for each width are normalized corresponding to their value at 60 nm for clearer comparison as shown in Fig. 11(c). Although the overall capacitance reduces with smaller width, the huge R_s and R_d still lead to the monotonous increase of channel charging delay.

IV. CONCLUSION

The high-frequency InGaAs nanowire FETs with scaled wire width have been systematically investigated with the assistance of TCAD simulation tools. It is found that the width scaling is effective in suppressing the device short channel effect without greatly sacrifice the cut-off frequency. Due to the strong quantum and volume inversion effects in smaller dimensions, the transport delay of the transistors can be improved with respect to the expected RF performance when only traditional width scaling is considered. These could be used as a potential knob for future RF optimizations of high-frequency III-V electronic devices.

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