Thermal analysis of advanced back-end-of-line structures and the impact of design parameters

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***Abstract*— In this paper, we present a thermal analysis of advanced back-end of line (BEOL) structures. This analysis includes an assessment of the equivalent out-of-plane thermal conductivity of the BEOL stack, the Joule heating of metal lines inside the BEOL stack, and a benchmark study of the impact of different design parameters, material properties, via layout, and an evaluation of the specific impact of barriers. The thermal analysis is conducted with 3D finite element models of two BEOL stack examples. The comprehensive sensitivity analysis of material properties shows that the dielectric thermal conductivity strongly impacts the BEOL thermal performance, and that the metal electrical resistivity has the strongest impact on Joule heating. In addition, the metal thermal conductivity and the barriers' electrical resistivity also give significant contributions. The via density DOE shows dramatic changes in BEOL thermal conductivity. The thermal impact of the barrier is also studied for different prototypical hybrid interconnect structures.**

Keywords*— *back-end-of-line, material property, via density, barrier, FEM, thermal modeling

NOMENCLATURE

A	area, m^2
k_{equ}	equivalent thermal conductivity, W/m-K
q	heat flux, W/m^2
R_{th}	thermal resistance, K/W
th	thickness, m
ΔT	temperature difference, K
κ	material thermal conductivity, W/m-K
ρ	material electrical resistivity, Ω·nm

Subscripts

z	out of plane

Acronyms

BEOL	back-end of line
BTE	Boltzmann transport equation
CD	critical dimension
CPI	chip-package interaction
FE	finite element
FEOL	front-end-of-line
IMD	intermetal dielectric
OSG	organosilica glasses

I. INTRODUCTION

The back-end-of-line (BEOL) stack consists of multilayers of densely routed thin and narrow metal lines and vias surrounded by intermetal dielectric (IMD), connecting transistors to the outer bond-pads. Its thermal resistance increases for scaling technology nodes [1], mainly due to the smaller dimensions of the metal lines and vias [2]-[3], and the lower thermal conductivity of low permittivity dielectrics (so-called low-κ: material with a small relative dielectric constant relative to silicon dioxide) [4]. Meanwhile, in 3D technology, the inter-die bonding interface thickness shrinks with developing integration technology [5], making the BEOL the dominant contributor to the overall thermal resistance in advanced packages [6] (> 90% of the total inter-die resistance for hybrid bonding [7]). The scaling-caused increase in current density and metal resistivity also raises the concern for Joule heating [8]. Moreover, the BEOL thermal management is crucial to the reliability of integrated circuits since the reliability degradations of the BEOL (i.e., electromigration, stress-migration) and the FEOL (i.e., Negative Bias Temperature Instability and Hot-Carrier Injection) are accelerated by high temperatures [9]-[11].

Therefore, it is important to accurately characterize the thermal properties of the BEOL stack. To further provide guidance to the thermal-aware interconnect design, it is meaningful to gain fundamental understandings of the impact from the material properties and the design-related and technology-related impacts.

Several studies have been focused on the FE modeling and experimental measurements of the BEOL thermal resistance. Based on different BEOL test structures, the extracted equivalent BEOL thermal conductivities are reported in a wide range (in work by Colgan et al. [12], k_{equ}=0.7-3.3 W/m-K; in work by Yan et al. [13], k_{equ}=2-12 W/m-K; and in work by

Bury et al. [14], k_{equ} =0.1-10 W/m-K). This big difference reflects the design specific nature of the BEOL structures. In addition, the high resistance barriers technically used to prevent diffusions of interconnects occupy a relatively larger volume in smaller interconnects [15], while they are often ignored in the thermal analysis [12]-[14]. Therefore, a detailed model is required to characterize the thermal properties of advanced BEOL structures and gain fundamental understandings of the thermal impact of material properties, the design-related via distributions, and the local interconnect barriers.

In this paper, we present a thermal analysis of the out-of-plane thermal conductivity and the Joule heating of advanced BEOL structures, and a benchmark study of the impact of various design parameters. In Section II, the 3D finite element models of two BEOL stack examples are introduced: 1) An unit cell of a 12-metal-layer advanced BEOL structure, representative for the 3 nm logic technology node; 2) A more versatile 4-metal-layer test chip design with 90 nm metal pitch and 17 different via configurations allowing a via density DOE on three via levels. The thermal modeling methodology is demonstrated in Section III. In Section IV, the material property sensitivity is benchmarked, and the impact of via distribution is discussed. The thermal impact of the barrier is also studied in-depth and benchmarked for different prototypical hybrid interconnect structures.

II. FE MODELS OF BEOL STACK EXAMPLES:

The thermal analysis is conducted with 3D finite element models of two BEOL stack examples:

A. *BEOL stack example 1:*

A unit cell of a 12-metal layer advanced BEOL structure [8], representative for the 3 nm logic technology node, is taken as an example for the thermal performance evaluation and general trend exploration of advanced BEOL stacks. A 3D finite element model with 2.94×10^6 elements is built based on a representative area of this advanced BEOL stack, as shown in Fig. 1. The footprint of the FE model is fixed at 1×0.5 μm^2, considering the balance between the computational time and the complexity to include all the key features of advanced BEOL.

The M_{int} is the smallest layer connecting the transistors, and the M_1-M_{12} are the 1st to the 12th metal layer in the BEOL stack. The dimensions of layers increase for higher levels, and the metal pitch varies from 21 nm to 80 nm. The Ru local interconnects in M_{int}-M_2 levels are considered barrierless, and the M_4-M_{12} levels on the top have Cu interconnects with TaN barriers. The dielectrics surrounding the interconnects are low-k dielectric except for the top layer with SiO_2 as the top passivation. This is an extreme example with a large portion of low-k, and it will be used to study the impact of the dielectrics in the BEOL.

Moreover, the dielectrics in the adjacent metal layers are separated by a thin SiCN layer, which works as an etch stopper for the subsequent via-opening process. The barrier thickness (2.5–5 nm) and the etch-stop thickness (5-17 nm) vary with the metal width.

The model includes a vertically connected powerline in the center from the bottom line M_{int} to the top line M_{12} to enable the self-heating investigation. The line density and the via density are fixed at a representative configuration of 50% and 1%, respectively. The barriers are simplified to be the via-bottom layers only.

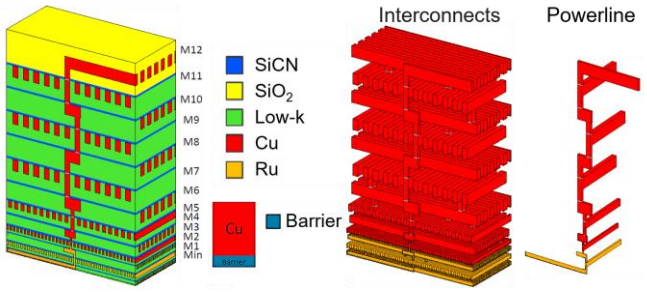

Fig. 1. FE model of BEOL stack example 1 for the 12-layer BEOL stack [8]

B. *BEOL stack example 2:*

To further investigate the thermal impact of design-related parameters, instead of adapting groups of structural changes on the large, complex model with the entire 12-metal layer advanced BEOL stack, a smaller scale and more versatile modeling test case has been used. The configuration of a 4-metal layer test chip design includes a DOE of via densities for 3 via layers.

The technical details of this test chip with 90 nm metal pitch and full Cu metallization are listed in TABLE I. The BEOL DOE tilings are originally designed for CPI investigation [16] but also suitable for the purpose of thermal investigation on the via density impact. As shown in Fig. 2, the test chip has 18 via configurations (17 of them are different) allowing a via density DOE on three via layers V_0, V_1, and V_2. There are 4 levels of via density configuration in each via layer over a wide density range (0.26%-4.15%). The top layer V_3 has a fixed via density of 1.38% due to the tiling area limit. The line density in all layers is also fixed at around 50%.

TABLE I. TECHNOLOGY DETAILS OF THE TEST VEHICLE PTCR (NM) [16]

Layer	Pitch	CD	Height	Dielectric
M4/V3	1080	540	2050	SiO_2
M3/V2	180	90	335	OSG 3.2
M2/V1	90	45	80	OSG 2.4
M1/V0	90	45	80	OSG 2.4
IM	360	180	100	SiO_2

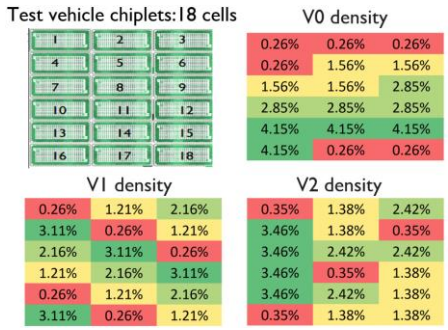

Fig. 2. Via density distribution on the 18 chiplets of BEOL stack example 2 [17]

The 3D FE model of this test structure shown in Fig. 3 is built based on the BEOL DOE tilings layout. The footprint is 1.5×1.5 μm^2. The vias are uniformly distributed throughout the plane at the designed via density and do not include the powerline functionality.

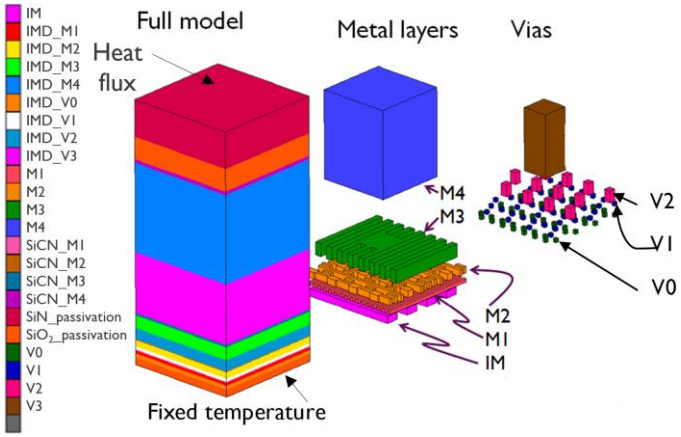

Fig. 3. FE model of PTCR BEOL [17]

III. THERMAL MODELING METHODOLOGY

A. *Material properties and boundary conditions*

For the dimensions considered in this thermal analysis of BEOL stacks, the nano-scale thermal effects cannot be ignored. Due to the internal and interfacial scattering of the heat carriers (phonons in semiconductors, and both electrons and phonons in metals), the effective thermal conductivity of materials decreases for smaller dimensions. The effective thermal material properties of metals have been extracted as a function of line and via dimensions from dedicated Monte Carlo BTE simulations shown in Fig. 4 [18]. Similarly, the nano-scale electrical effects should be considered, and the electrical resistivity values have been extracted from dedicated electrical measurements of scaled lines [3].

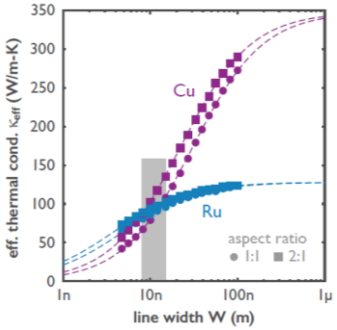

Fig. 4. Cu and Ru thermal conductivity extracted as a function of metal dimensions from dedicated Monte Carlo BTE simulations [18]

Fig. 5 shows the boundary conditions applied to different types of thermal analysis:

In the application, the heat generated in the transistors in the front-end-of-line (FEOL) needs to be transferred through the BEOL stack. The consequent temperature rise is determined by the equivalent out-of-plane thermal properties. In order to extract the equivalent out-of-plane thermal conductivity of the BEOL, an uniform external heat flux q is forced to go vertically through the stack. The average temperature of the upper and lower surfaces is used to extract the temperature difference across the equivalent medium in the Z direction (the vertical direction along the stack), as in (1). The equivalent out-of-plane thermal properties are calculated according to the Fourier law of 1D heat conduction, as in (2) and (3):

$$\Delta T = T_{top} - T_{bottom} \tag{1}$$

$$k_{equ} = q \cdot th/\Delta T \tag{2}$$

$$R_{th} = th/(q \cdot A) \tag{3}$$

For the BEOL self-heating evaluation, the thermal performance is assessed by the maximum temperature increase in the BEOL stack, as in (4). A 100 μA current is injected from the bottom line (M_{int}) to the top line (M_{12}) to mimic the behavior of a power line. There are three possibilities for the boundary conditions: bottom-side cooling, top-side cooling, and dual-side cooling. As an example, the cooling from the top side of the BEOL is applied in the Joule heating study. While in the application, a suitable boundary condition should be applied to mimic the package and cooling conditions.

$$\Delta T = T_{max} - T_{min} \tag{4}$$

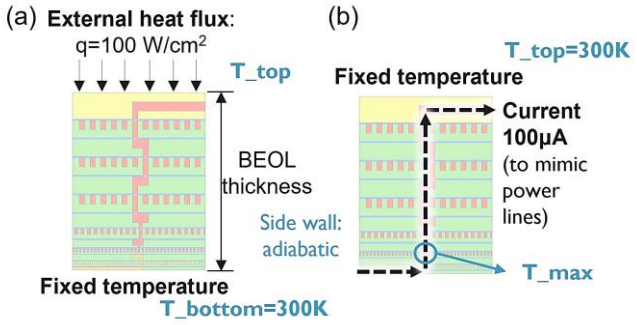

Fig. 5. Boundary conditions applied for (a) the extraction of the equivalent out-of-plane thermal conductivity and (b) Joule heating of the BEOL stack

B. *Local model for barrier impact investigation*

The two BEOL stack examples introduced above could provide representative thermal property estimates of the whole BEOL stack. However, they could be less flexible in exploring the local impact of barriers. Instead, a local 2-line BEOL model with a single via in between (20 nm CD with 2 nm thick barrier, 420 nm footprint) is built to evaluate the barrier impact on self-heating specifically. Fig. 6 shows the Dual-Damascene scheme: a conformal barrier layer is deposited simultaneously on the sidewall and the bottom of V_1M_2 trenches. Therefore, a 2 nm barrier is added in the local model at these places. A 100 μA current is injected from M_2 to M_1 for Joule heating investigation.

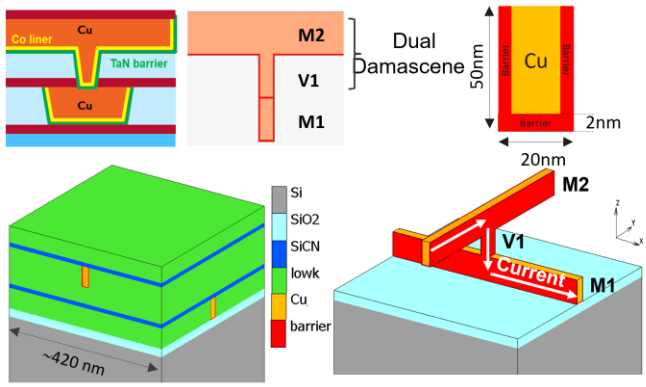

Fig. 6. Dual-Damascene scheme [15] and a local 2-line BEOL model for barrier impact investigation

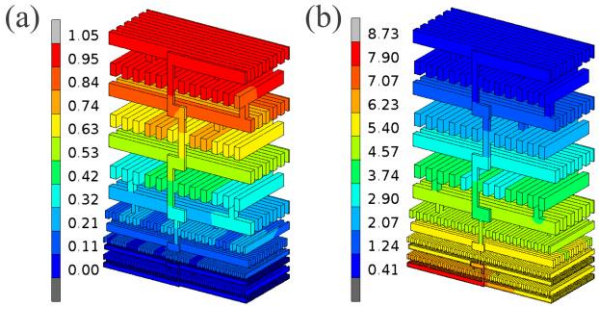

Fig. 7. Temperature maps of the reference BEOL structure under different boundary conditions: (a) external heat flux and (b) Joule heating

IV. THERMAL ANALYSIS RESULTS

A. *Material property sensitivity benchmarking*

A comprehensive sensitivity analysis of material properties is performed on the BEOL stack example 1 with the entire 12-metal layer advanced BEOL design. It is conducted on both BEOL thermal properties: $k_{equ,z}$ and Joule heating temperature. Fig. 7 shows the temperature distribution of the reference structure under the two different boundary conditions, and the reference results are $k_{equ,z}$=1.53 W/m-K and ΔT_{max}= 8.73°C.

In the sensitivity study, the material parameters are varied with respect to their reference value. These input reference values and the output sensitivities on the equivalent thermal conductivity and Joule heating temperature are listed in TABLE II. The sensitivity of output factor Y with respect to the input factor X is defined as in (5):

$$S_Y(X) \equiv \frac{\Delta Y/Y}{\Delta X/X} \tag{5}$$

The IMD thermal conductivity presents a strong impact on the BEOL thermal performance for both heating scenarios. It could be explained by the poor thermal conductivity of this porous dielectric and the high volumetric percentage it takes in the BEOL stack (~74.5%). For the interconnect metals, the metal thermal conductivity has a relatively smaller impact on the BEOL thermal properties, while the metal electrical resistivity shows a dominant impact on Joule heating since it determines the total heat generated inside the BEOL stack. Besides these two main components, the barrier and the etch-stop layer are extremely thin, but their material properties also show unignorable impacts. The thermal property of the etch-stop layer has a comparable impact with that of the interconnect metals, highlighting the potential benefits of the etch-stop layer in the BEOL thermal management as a dielectric with relatively high thermal conductivity covering all interconnects. Moreover, the electrical resistivity of the barrier largely contributes to the Joule heating of metal lines inside the whole BEOL stack. In order to assess the local temperature increase caused by the barrier and understand the detailed impacts, an in-depth investigation with a local model is required.

TABLE II. MATERIAL PROPERTY SENSITIVITY STUDY FOR BEOL EQUIVALENT THERMAL CONDUCTIVITY AND JOULE HEATING

Parameter	BEOL $k_{equ,z}$ Sensitivity	Joule heating Sensitivity	Reference value
k_low-k	0.50	-0.45	0.3 W/m-K
k_metal	0.17	-0.21	65-230 W/m-K depending on metal CD
k_etch-stop	0.14	-0.21	5 W/m-K
k_barrier	0.07	-0.05	5 W/m-K
ρ_metal		0.97	49-175 Ohm·nm depending on metal CD
ρ_barrier		0.22	1200 Ohm*nm

B. *Impact of via distribution*

With the versatile 4-metal layer BEOL stack example 2 introduced in Section II.B, a via density DOE on three via levels V_0, V_1, and V_2 is performed for the 17 different via density configurations. As shown in Fig. 8, a general trend of the BEOL $k_{equ,z}$ is observed as a function of average via density. When the average via density of the test cases varies from 0.3% to 2.6%, the equivalent BEOL thermal conductivity shows a dramatic increase from 2.2 W/m-K to 6.5 W/m-K, resulting in a BEOL $k_{equ,z}$ magnification of 3 times. the thermal performance deviation at the same average via density increases with the via density, at the maximum average via density ~2.6%, the BEOL $k_{equ,z}$ deviation reaches 2.5 W/m-K, indicating the very strong contribution of the detailed via distribution and local connections to the metal lines. This indicates that a simplified prediction based on average via density is not sufficient, and a more detailed analysis is required.

The via density DOE of the V_2 layer, as an example, shows the individual impact of a single layer's via density in Fig. 9. An overall trend is observed as a function of the V_2 density: the BEOL $k_{equ,z}$ changes rapidly with the V_2 density at low-level density and tends to saturate at high-level density. The impact of

the V_2 density is also observed to be related to the via density configurations of the layers above and below (V_0 and V_1). A high via density configuration in the adjacent layers magnifies the V_2 density impact. These trends can be explained by the series connectivity of the thermal resistance in the adjacent layers. However, some abnormal data points are found in the curves of Fig. 9. Comparing the point 1) and 2), the BEOL $k_{equ,z}$ doesn't increase with the V_2 density; and comparing the point 1) and 3), the BEOL $k_{equ,z}$ doesn't increase with the V_1 density. The vertical via alignment between the adjacent layers can explain the phenomenon. Most of the heat flux towards the lower levels is concentrated in the vias of the V_3 layers, making the central lines connected to V_3 a vertical heat conduction highway. As a result, the lack of vias connecting the central metal lines reduces the heat conduction in this thermal highway. Therefore, the local connections of the vias to the metal lines significantly impact the thermal performance of the entire BEOL stack.

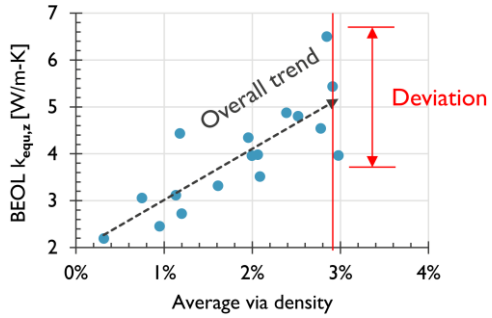

Fig. 8. Via density DOE: BEOL $k_{equ,z}$ as a function of the average via density

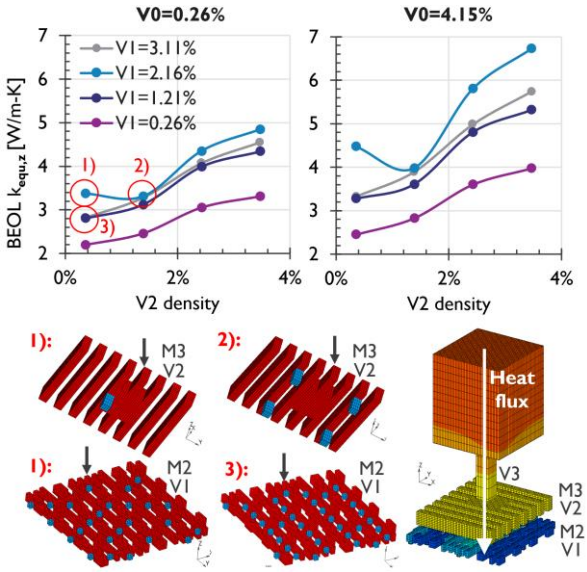

Fig. 9. Trends of the impact of V_2 density

The extracted thermal resistances of the individual layers in this BEOL test structure are listed in Fig. 10. The total thermal resistance of all via layers is 4-5 times higher than that of all metal-line layers, indicating the nature of the BEOL that the total thermal resistance is dominated by the via layers. It explains the significant impact of the detailed via distribution and local connections to the metal lines.

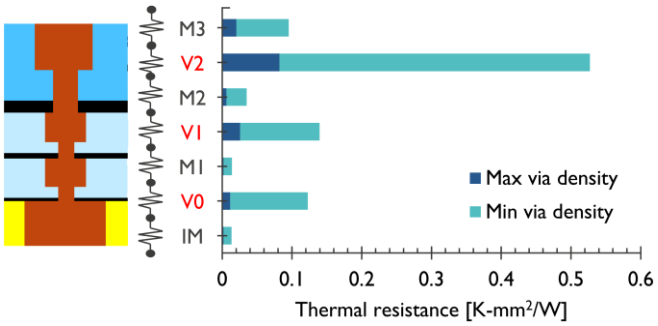

Fig. 10. Layer thermal resistance extracted from the BEOL FE model

The sensitivity analysis in Section IV.A. shows a dominant impact of the IMD thermal conductivity on the BEOL equivalent thermal conductivity. Therefore, a low-k DOE is also performed for this BEOL test structure to explore the impact of the IMD thermal conductivity at different via density configurations. Since there are two groups of low-k dielectrics in the M_1V_0-M_3V_2 levels (details in TABLE I.), the low-k DOE is also conducted on these two groups of layers. For each group of layers, two levels of via density are studied. The graphs in Fig. 11 show that the IMD thermal conductivity impacts more on the BEOL layers with lower via density, where more heat needs to pass through the IMD due to the limited heat conduction area in the metal.

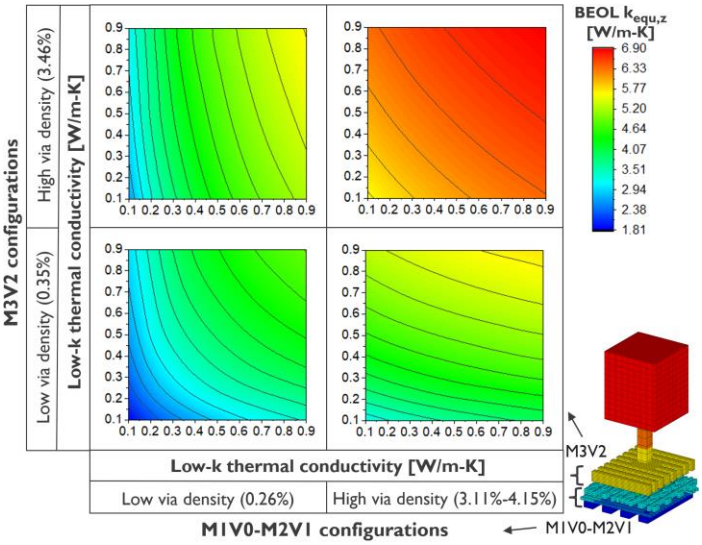

Fig. 11. Low-k DOE on two groups of layer: x-axis: M_1V_0-M_2V_1 dielectric, y-axis: M_3V_2 dielectric

C. Impact of barrier

The sensitivity benchmark study of material properties in Section IV.A shows a significant impact of the barriers, especially for the Joule heating of metal lines inside the BEOL stack. A further comparison is performed in this section on the BEOL stack example 1 (12 metal layer stack) with an artificial barrierless configuration at the reference values of the material parameters. It is found that the presence of the barrier at the via bottom (barrier thickness from 2.5 nm to 5 nm) reduces the BEOL $k_{equ,z}$ by 13.3% and increases the Joule heating temperature by 14.3%. It significantly impacts the thermal properties of the BEOL stack, even though the barrier only exists

in some of the 12 layers (the most resistive small metal layers M_{int}-M_2 in Ru are barrierless). In this Joule heating scenario, only one of the many vias per layer has a 100 μA current injection mimicking the behavior of a power line. While in an application scenario, the signal lines also carry current, resulting in a more significant impact of the barrier on the Joule heating since more vias are injected with the current. Therefore, an in-depth investigation of the detailed impact of the barrier is required. The specific local and flexible model with a full barrier configuration has been demonstrated in Section III.B.

Based on the local FE model including the full barrier configuration (Section III.B, Fig. 6), a DOE study of the barrier thermal and electrical properties is performed as shown in Fig. 12. The Joule heating is evaluated by the temperature increase at the M_2 top center point. The Joule heating temperature dramatically changes with both of the input parameters within the studied range. It suggests that the barrier electrical resistivity has a larger impact at limited thermal conduction, and the barrier thermal conductivity has a more significant impact when more heat is generated. Two extreme barrier material cases at the two corners of this DOE domain have been selected as examples for the case studies in the following investigation: 1) a highly resistive barrier, such as TiN with low thermal conductivity and high electrical resistivity (example 1: 0.92 W/m-K and 3000 Ω·nm); and 2) a low resistance barrier, such as TaN with high thermal conductivity and low electrical resistivity (example 2: 5 W/m-K and 1200 Ω·nm).

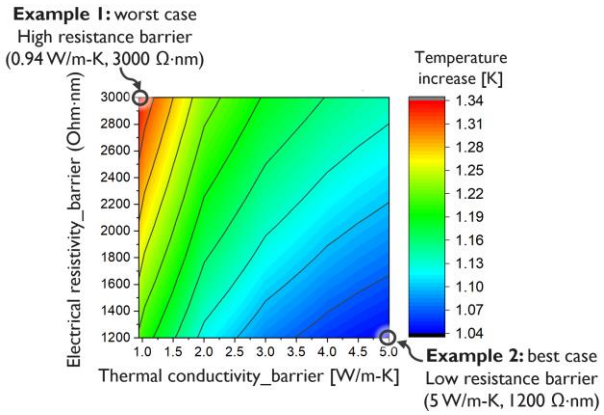

Fig. 12. DOE of material properties of the barrier

For the example case study, the temperature curves along the central vertical line across M_2, V_2 and M_1 (z-direction) are plotted in Fig. 13, while a barrierless configuration is modeled for comparison. For these two extreme barrier examples, the presence of the barrier leads to a 170%-260% temperature increase for the local Joule heating. In the full-barrier cases, the large temperature increase in V_1M_2 indicates that the barrier causes extra heat sources due to resistive heating in the barrier material. Furthermore, the large temperature offset at the barrier location between M_1 and V_1 indicates the extra thermal resistance caused by the barrier. Therefore, the presence of the barrier further increases the thermal resistance of the via layer, which is already the dominating contributor to the overall BEOL thermal resistance. In addition, as shown in the cross-sectional diagrams of the interconnects in Fig. 13, the outer width of the metal line is 20 nm, while the width of the central Cu fill is 16 nm surrounded by a 2 nm barrier. The volumetric reduction of the central Cu fill caused by the barrier's existence increases the current density and heat flux in the central Cu fill. Due to smaller dimensions, the central metals' effective thermal and electrical resistivity also worsens.

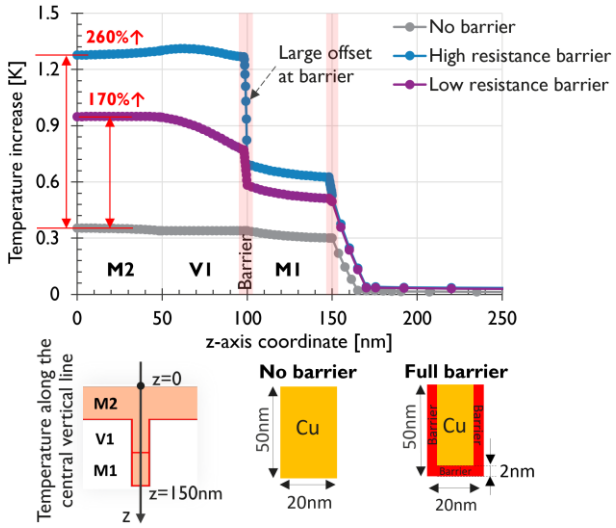

Fig. 13. Temperature curves along the central vertical line of the local model, and the schematics of no-barrier and full-barrier interconnects

An impact study of the barrier thickness is shown in Fig. 14. The barrier thickness strongly impacts the Joule heating temperature, especially for the high resistivity barrier example. The central Cu fill shrinks with the increase of the barrier thickness. Consequently, the temperature offset at the barrier location, and the heating inside the interconnects increases. For the high resistivity barrier example, a local temperature peak is observed at the barrier location between the V_1 and the M_1 for a thick 3 nm barrier configuration. It can be explained by the heat localization at this place due to the increased heat generation and the limited local heat conduction.

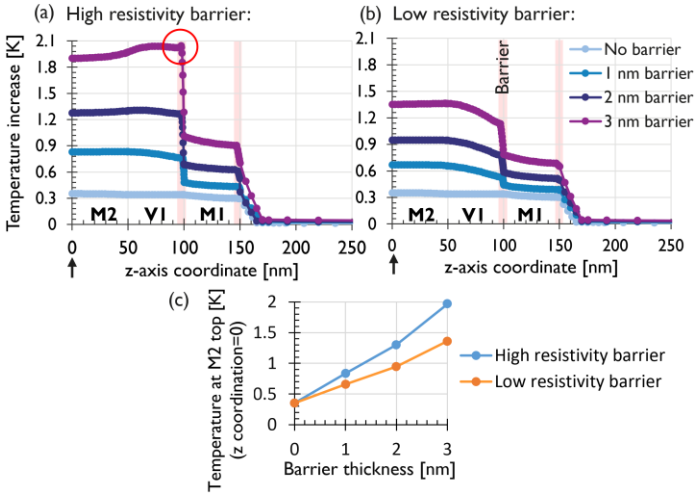

Fig. 14. Impact of barrier thickness: temperature curves along the central vertical line for (a) High resistivity barrier and (b) Low resistivity barrier; (c): the temperature at the M_2 top (z=0) as a function of the barrier thickness

As the previous sensitivity analysis in TABLE II. shows, the Joule heating is strongly affected by the IMD thermal

conductivity. Fig. 15 shows a barrier example case study at different IMD thermal conductivity values. For the test cases with higher IMD thermal conductivity (0.9 W/m-K), the lower temperature increase inside the interconnect metals and the reduced temperature offset at the barriers indicate better heat conduction from the surrounding dielectrics. As a result, a local temperature peak is observed at the barrier between the V_1 and the M_1 for the high resistivity barrier example. However, in advanced BEOL structures, the IMD thermal conductivity tends to be further reduced in exchange for a better permittivity performance. In Fig. 15, when the IMD thermal conductivity decreases from 0.9 W/m-K to 0.3 W/m-K, the Joule heating temperature of the barrierless interconnects slightly increases by 7.4%, while the temperatures of the full-barrier cases significantly increase by 78%-87%. It highlights an even more significant impact of the barriers in advanced BEOL configurations.

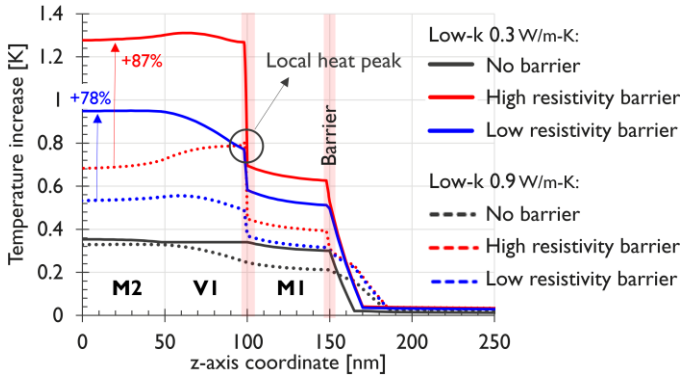

Fig. 15. Impact of the IMD thermal conductivity: temperature curves along the central vertical line for κ_low-k=0.3 W/m-K and κ_low-k=0.9 W/m-K

D. Interconnect barrier thermal benchmarking:

With the available methodology demonstrated in Section IV.C, a thermal benchmark study is performed for a variety of interconnect/barrier configurations that are currently considered for advanced BEOL stacks [15], [19]-[21]. As shown in Fig. 16, the interconnection/barrier configurations are divided into three groups:

1) Full Cu metallization. The scaling of the TaN barriers reduces the Joule heating temperature of metal lines inside the BEOL stack. The impact of barrier thickness has been discussed in Section IV.C (Fig. 14).

2) Hybrid metallization integrating different interconnect metals. At the metal width of this study, the thermal conductivity values of the Cu and the alternative Ru and Co interconnects are in order of $\kappa\_Cu > \kappa\_Ru > \kappa\_Co$ [18], and the electrical resistivity values are in order of $\rho\_Cu < \rho\_Ru < \rho\_Co$ [3]. Therefore, more heat is generated inside the Ru and Co metals compared to Cu at the same width. While the Joule heating temperature decreases are observed in the hybrid configurations d), e), and f). For the slight impacts of Ru M_1 and Ru V_1M_1, although the Ru interconnects have relatively higher thermal and electrical resistance, the barrierless feature of the Ru metallization reduces the crowding of current and heat flow in the metal. The advantage of the barrierless feature also explains the better thermal performance of the special barrierless Co via. Among all the test structures, the highest temperature increase comes from the hybrid interconnect structure g) with Co/TiN M_2V_1 and Ru barrierless M_1. This thermal behavior is explained by the relatively high electrical resistivity and low thermal conductivity of Co interconnects. Furthermore, the high temperature offset at the barrier location of this configuration also indicates a large contribution from the high resistivity barrier.

3) Full Ru metallization. This structure presents the best thermal performance among all the test structures. The full-barrierless configuration is the main contributor to the superior interconnect thermal performance.

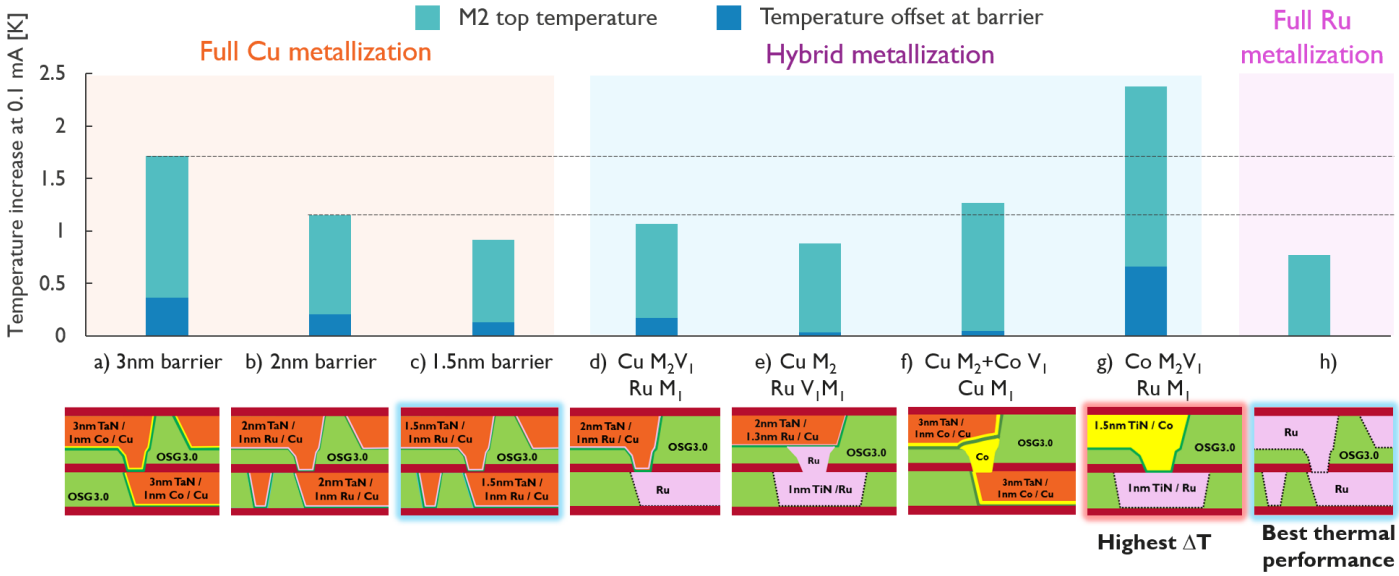

Fig. 16. Thermal benchmarking study of local Joule heating performance on the current representative interconnect/barrier configurations [15], [19]-[21]

V. CONCLUSIONS

In this work, we present a thermal analysis of advanced back-end of line (BEOL) structures. This analysis includes an assessment of the equivalent out-of-plane thermal conductivity of the BEOL stack, the Joule heating of metal lines inside the BEOL stack, and a benchmark study of the impact of different design parameters, material properties, via layout, and an evaluation of the specific impact of barriers.

A comprehensive sensitivity analysis of material properties is first conducted on the unit cell of a 12-metal-layer advanced BEOL structure, representative for the 3 nm logic technology node. It shows that the IMD thermal conductivity strongly impacts the BEOL thermal performance, and that the metal electrical resistivity has the strongest impact on Joule heating. In addition, the metal thermal conductivity and the barriers' electrical resistivity also give significant contributions.

In the next step, a via density DOE is conducted on a smaller scale and more versatile modeling test case with 90 nm metal pitch. It shows dramatic changes in the BEOL thermal conductivity and a very strong contribution of the detailed via distribution and local connections to the metal lines. The extracted thermal resistances of via layers are 3-9 times higher than that of the metal-line layers, revealing the importance of the via impact. Moreover, the close relationship of the via impact with the IMD thermal conductivity is discussed.

With a specific local model, an in-depth investigation of the impact of barrier is also studied. The presence of the barrier leads to a 170%-260% local temperature increase on the via level and a large temperature offset on a single via during Joule heating. It can be explained by the barrier-caused extra heat source, additional thermal resistance, and the increased current density and heat flux in the volumetrically reduced central metal fill. The impact of the barrier thickness and the IMD thermal conductivity variation are further discussed. This study is also extended to the thermal benchmarking for a variety of currently representative hybrid interconnect structures. The barrierless full-Ru interconnect structure presents the most promising thermal performance, while the hybrid interconnect structure with Co interconnect in combination with TiN barrier shows the highest temperature increase inside the interconnect metals.

VI. REFERENCE

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