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A 0.00426 mm^2 77.6-dB Dynamic Range VCO-Based CTDSM for Multi-Channel Neural Recording

Shiwei Wang [1,2], Xiaolin Yang [1,*], Chaohan Wang [3], Anastasios Vilouras [2] and Carolina Mora Lopez [1,*]

[1] IMEC, 3001 Leuven, Belgium
[2] School of Engineering, University of Edinburgh, Edinburgh EH8 9YL, UK
[3] Department of Electrical and Electronic Engineering, Imperial College London, London SW7 2BX, UK
* Correspondence: xiaolin.yang@imec.be (X.Y.); carolina.moralopez@imec.be (C.M.L.)

Abstract: Driven by needs in neuroscientific research, future neural interface technologies demand integrated circuits that can record a large number of channels of neural signals in parallel while maintaining a miniaturized physical form factor. Using conventional methods, it is challenging to reduce circuit area while maintaining the high dynamic range, low noise, and low power consumption required in the neural application. This paper proposes to address this challenge using a VCO-based continuous-time delta-sigma modulator (CTDSM) circuit, which can record and digitize neural signals directly without the need for front-end instrumentation amplifiers and anti-aliasing filters, which are limited by the abovementioned circuit-area performance tradeoff. Thanks to the multi-level quantization and intrinsic mismatch-shaping capabilities of the VCO-based approach, the proposed first-order CTDSM can achieve comparable electrical performance to a higher-order CTDSM while offering further area and power reductions. We prototyped the circuit in a 22-channel test chip and demonstrate, based on the chip measurement results, that the proposed modulator occupies an area of 0.00426 mm^2 while achieving input-referred noise levels of 6.26 and 3.54 μV_{rms} in the action potential (AP) and local field potential (LFP) bands, respectively. With a 77.6 dB wide-dynamic range, the noise and total harmonic distortion meet the requirements of a neural interface with up to 149 mV_{pp} input AC amplitude or up to ±68 mV DC offsets. We also validated the feasibility of the circuit for multi-channel recording applications by examining the impact of cross-channel VCO oscillation interferences on the circuit noise performance. The experimental results demonstrate the proposed architecture is an excellent candidate to implement future multi-channel neural-recording interfaces.

Keywords: neural recording; continuous-time delta-sigma modulator; VCO; multi-channel neural readout

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1. Introduction

Multi-channel neural-recording integrated-circuits are essential in today's electrophysiology tools to enable simultaneous readouts from thousands of neurons in vivo [1,2]. These tools allow neuroscientists to access signals from large neuronal populations across wider brain regions while conducting experiments on freely moving animals, leading to a deeper and more comprehensive understanding of the brain and nervous system [3–6]. The proliferating demand for large-scale neural interfacing has been driving the development of area-efficient neural-recording circuits, which allow the integration of more parallel recording channels in miniaturized systems on a chip [7–11].

Conventionally, a neural-recording channel consists of at least three circuit blocks: an instrumentation amplifier (IA), an anti-aliasing filter (AAF), and an analog-to-digital converter (ADC) [8–10,12–14]. In such architecture, the IA and AAF amplify and condition the input signal before the ADC, thus reducing the requirement of the latter. However, the circuit areas of the IA and AAF are difficult to minimize given the low-noise and high-input-impedance requirements; furthermore, the channel dynamic range is limited.

In recent years, continuous-time delta-sigma modulators (CTDSM) have been used for the direct digitization of neural signals, which achieved good area efficiency [11,15–19]. CTDSMs have implicit anti-aliasing capabilities and can achieve high-input-impedance and low-noise results [20]. Therefore, it is possible to directly use CTDSMs for neural recording, thus eliminating the need for dedicated instrumentation amplifiers (IAs) and anti-aliasing filters while achieving good area efficiency. Furthermore, the capability to achieve a high dynamic range (DR) makes CTDSMs better candidates for implementing artifact-tolerant neural recording compared with conventional architecture, which can be easily saturated with large input artifacts. In Refs. [16,18], input ranges of 300 mV_{pp} and 148 mV_{pp} were achieved, respectively, which are significantly wider than the input ranges of conventional IA-based front ends, which are typically limited to 10 mV_{pp} [8–10,12–14].

The suitability of CTDSMs for direct neural recording can be further improved by using phase-domain integration and multi-bit quantization through voltage-controlled oscillators (VCOs) [18,21–26]. Such VCO-based approaches allow loop filters and quantizers to operate under a low supply voltage, and they have intrinsic mismatch-shaping capabilities to address the linearity issues in multi-bit modulators. Moreover, they can strongly benefit from CMOS technology scaling, since the integrators and quantizers are fully implemented in the digital domain. Thanks to these advantages, previously reported works have achieved ultra-high DR with good area and power efficiencies. Nevertheless, all the existing works only demonstrated VCO-based neural recording on single-channel designs, while its feasibility for multi-channel neural recording is not yet validated. A potential issue of using a VCO-based architecture for multi-channel neural recording is the coupling of VCO oscillation interferences from the nearby channels. This issue can be significant as the reference voltages and supply lines are typically shared among multiple channels, and the VCO center frequencies will be different across channels. This can result in potential broadband interferences that are more difficult to remove. These effects need to be investigated to validate the suitability of VCO-based readout architectures for multi-channel neural-recording applications.

In this paper, we present the design and experimental results of a VCO-based CTDSM for multi-channel neural recording. The modulator provides first-order noise shaping and 30-level quantization by using 15-stage ring oscillators (ROs), and it was tested in a 22-channel prototype chip. We demonstrate that the modulator can achieve equivalently good input-referred-noise, DR, and input-impedance performances compared with a more complex second-order CTDSM neural-recording front-end with two times the sampling rate [18]. The reduced complexity and sampling rate allows further reductions in circuit area and power consumptions. We also measured the effects of multi-channel VCO oscillation interference on the modulator performance. The results indicate an acceptable increase of noise when multiple channels that are densely placed and have shared reference and supply voltages are operating simultaneously. This proves the design is suitable for the target multi-channel applications.

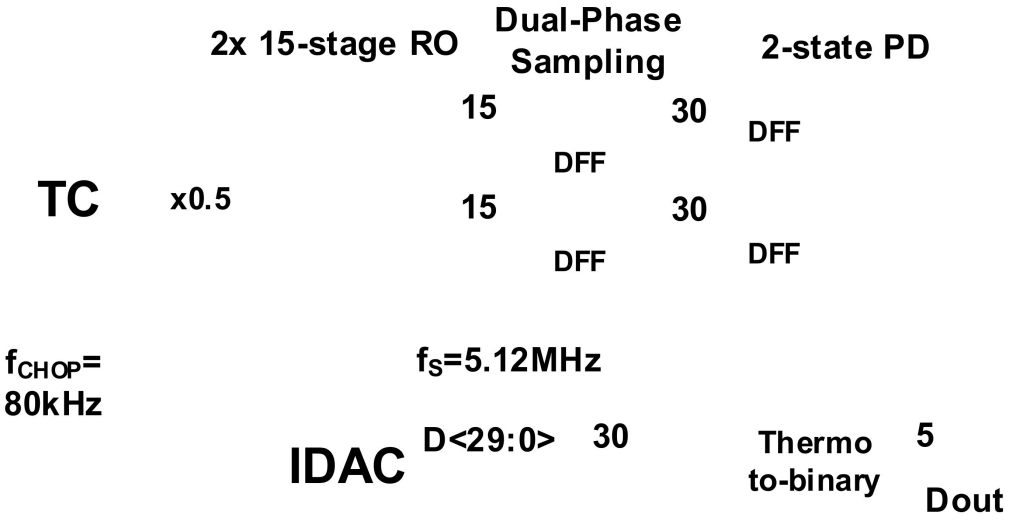
2. Modulator Architecture

The high-level block diagram of the proposed CTDSM is shown in Figure 1a, while the simplified s-domain diagram is given in Figure 1b. The modulator uses a chopper-stabilized transconductance (TC) amplifier as the input stage, which converts input neural potentials into a current signal. The difference between the input current and the current-mode digital-to-analog converter (IDAC) feedback is halved and then used to modulate the supply current of a pair of 15-stage ROs. The RO outputs are sampled with D flip flops (DFFs), and both the non-inverting and the inverting outputs of the DFFs are fed to an array of two-state phase detectors (PD). This results in an effective 30-level quantization. The 30-level quantized results are thermometer-coded, and they are fed back through the IDAC as well as sent to the output through a thermometer-to-binary (Th2Bi) logic. A list

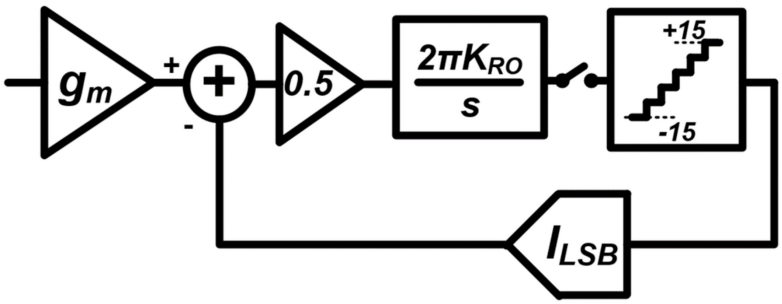
of high-level design parameters is summarized in Table 1. The feed-in coefficient b and feedback coefficient a are derived with the following equations:

$$b = \frac{2g_m \cdot 0.5 \cdot (2\pi K_{RO})}{f_s} \quad (1)$$

$$a = \frac{2I_{LSB} \cdot 0.5 \cdot (2\pi K_{RO})}{f_s} \quad (2)$$



(**a**)



(**b**)

Figure 1. (**a**) Block diagram of proposed VCO-based CTDSM. (**b**) Simplified diagram of modulator.

Table 1. High-level modulator design parameters.

Parameters	Value
TC transconductance (g_m)	30.5 µS
IDAC LSB current (I_{LSB})	200 nA
RO gain (K_{RO})	610 GHz/A
Quantization levels (N)	30
Quantizer gain (k_q)	30/2 π = 4.77
Feed-in coefficient (b)	22.9
Feedback coefficient (a)	0.15
Sampling rate (f_s)	5.12 MHz (256 × OSR)

The modulator is designed to record both local field potentials (LFPs) and action potentials (APs), covering a signal bandwidth of 10 kHz. The AP and LFP signal amplitudes

are typically up to 10 mV_{pp} [1,2,8,9]; however, this design targets a wider input range (up to ~150 mV_{pp}) to accommodate electrode DC offsets and tolerate stimulation/movement artifacts. Therefore, the TC stage, the IDAC least significant bit (I_{LSB}), and the number of quantization levels (which also defines the number of RO stages) are chosen to obtain this required input voltage range, which is determined by N^*I_{LSB}/g_m. The modulator provides first-order noise shaping with an oversampling ratio (OSR) of 256 and 30-level quantization. Thus, ~1 μV_{rms} total input-referred in-band quantization noise can be achieved, which is given by

$$\overline{V_{QN,\,i}{}^2} = \frac{\pi^2 a^2}{36 * OSR^3 b^2} \tag{3}$$

To meet the noise requirements of a neural-recording application, the readout-circuit noise needs to be minimized. Therefore, in this design, the value of g_m is chosen as the optimal trade-off between circuit noise and power consumption.

3. Schematic Design

The schematic design of the modulator is shown in Figure 2, which includes all blocks except the Th2Bi logic. Transistors *MN1-4* and *MP1-10* form a chopper-stabilized current-balancing TC stage, with input impedance boosting achieved using the bootstrapping transistors *MN1-2* [18]. The input transistors *MP1-2* are thick-oxide devices to avoid gate leakage. The g_m is defined by resistor R_1, which has a value of 32.7 kΩ. The IDAC feedback currents are injected at the two terminals of R_1, and the voltage difference across the two terminals is a copy of the input voltage because of the flipped-voltage-follower structure formed by *MP1-6* and *MN1-4*. Therefore, the input voltage is converted to a current by R_1, and the difference between the converted input current and the IDAC feedback current flows through transistors *MP3-6*, gets copied to *MP7-10* with a 2:1 ratio, and is finally injected to the top lines of the two 15-stage ROs. The two ROs are pseudo-differential and both the rising and the falling edges of their outputs can trigger the PDs. In this way, the 30-level quantization is achieved. The quantized outputs from the 30 PDs are fed to the IDAC, which has 30 current-steering elements. Compared with the input TC stage in Ref. [18], this design does not require common-mode feedback circuits, which is another advantage of the VCO-based approach.

The total static current consumption of the modulator is 9.8 μA. The PDs will consume additional dynamic power, which depends on the sampling rate. In this design, the

IDAC and the ROs are embedded in the TC stage and do not consume additional power. The currents of the IDAC (i.e., 15×200 nA on each side when the input voltage difference is 0 V) contribute to the biasing of the input transistor (*MP1-2*), and the ROs are directly biased with the TC output current. A lower RO free-running frequency (f_{RO}) is preferred to reduce the dynamic power consumption of the ROs and PDs, which can be achieved by reducing the TC common-mode (CM) output current or increasing the RO loading capacitance at each inverter stage. The latter is realized by increasing the inverter gate lengths, which enlarges the RO area but reduces the flicker noise. In this design, the TC CM output current is 0.5 μA and, thus, a 370 kHz f_{RO} is achieved while preserving a small RO area. Because I_{LSB} is 200 nA and it determines the RO frequency modulation index, further reducing the TC CM output current will induce large voltage variations on the RO top-line voltage, thus increasing the non-linearity and causing errors due to unmatched logic levels with the following DFFs.

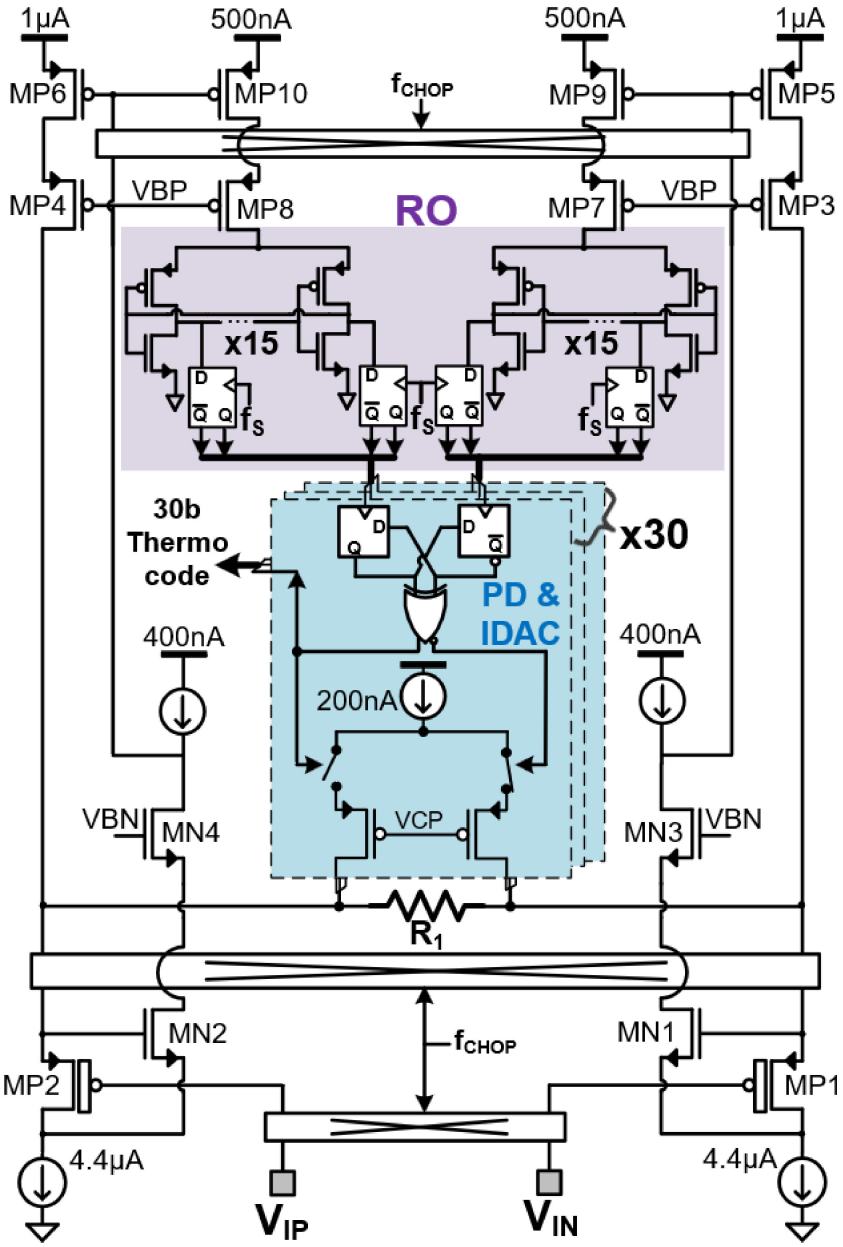


Figure 2. Transistor-level schematic of the proposed VCO-based CTDSM.

4. Results and Discussion

A prototype chip was implemented and fabricated using a 55 nm CMOS technology. The chip micrograph and channel layout details are shown in Figure 3a. Each channel occupies an area of 129 µm × 33 µm. In order to evaluate the influence of the neighboring channels (i.e., VCO oscillation interferences) on the proposed CTDSM readout performance, a total of 22 channels sharing the same biasing voltages and supplies were implemented on the chip. All the channels share the same biasing, supply voltages, and ground lines, which are distributed from left to right to replicate the layout constraints in ultra-dense neural probes [8,9]. In this proof-of-concept prototype, the outputs of only 3 out of the 22 channels are accessible for characterizations. These three channels include two that are right next to the global biasing block (these are the best-case channels) and one that is the farthest from the global biasing block (this is the worst-case channel). In this work, we used the setup shown in Figure 3b to characterize the three channels. The worst-case channel will pick up the highest noise coupling and interferences from the other channels, and the impacts of

these coupling effects and interferences can be quantitatively evaluated by comparing the results in two cases: (i) when all other channels are enabled and (ii) when all other channels are disabled. To test the chip, we developed a custom-printed circuit board using Altium and used a National Instrument module to acquire and analyze the chip output data, while the required decimation filter was implemented in software.

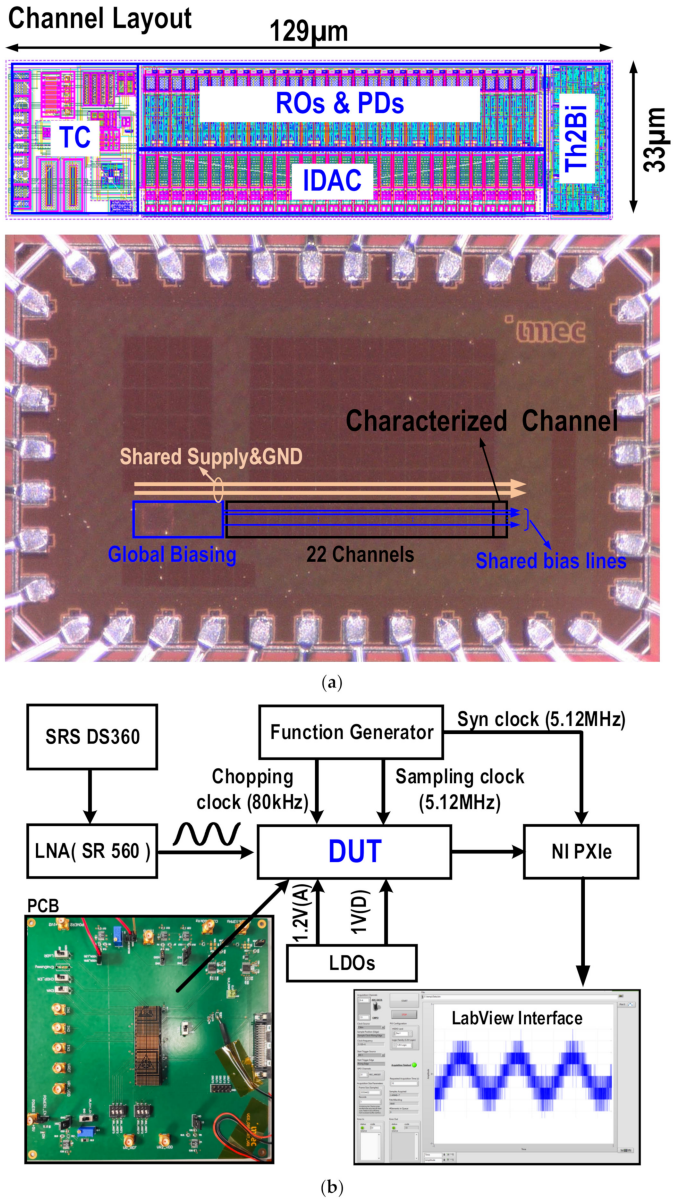


Figure 3. (**a**) Chip micrograph and details of channel layout. (**b**) Diagram of test setup and picture of test board.

The measured noise spectrum and the integrated input-referred noise in the LFP (0.5–1000 Hz) and AP (0.3–10 kHz) bands are shown in Figure 4. The effectiveness of the chopper-stabilization technique is demostrated in this measurement. When the choppers in the TC stage were disabled, the noise is 2.4 times higher in the AP band and 4.65 times higher in the LFP band. Note that a residual low-frequency flicker noise is visible in the noise spectrum, which is because the transistors that form the PMOS current mirror in the TC stage (*MP5-6* and *MP9-10*) are not chopped. This is a design choice made to avoid the aliasing of high-frequency-shaped quantization noise in the IDAC feedback, as elaborated in Ref. [18]. From these results, we can also conclude that the AP and LFP

noise only increases by 11.3% and 27.7%, respectively, in the worst-case channel when all 22 channels were enabled. This increased noise is still below what is acceptable for the application [1,2,8,9], demonstrating the suitability of the proposed VCO architecture for multi-channel operation.

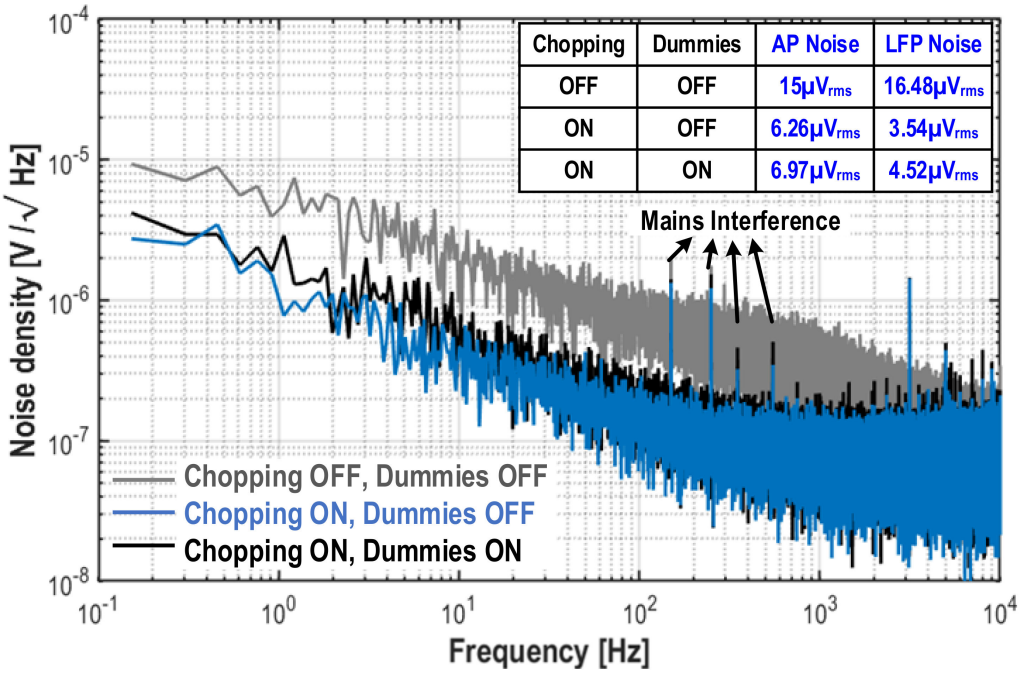


Figure 4. Measured noise density in worst-case channel when all other channels are disabled and enabled, showing effect of chopping stabilization technique.

The power spectral density (PSD) of one channel was measured with a 10 mV_{pp}, 1 kHz sinosoidal input at 0 V input DC offset (Figure 5). The achieved signal-to-noise-and-distortion ratio (SNDR) is 52.7 dB, and the signal-to-noise ratio (SNR) is 54.39 dB. The SNDR and SNR were also measured with different input amplitudes (Figure 6), resulting in a peak SNR of 76.8 dB and an effective dynamic range (DR) of 77.6 dB without any SNR degradation up to 149 mV_{pp}. Even though the SNDR degrades for amplitudes beyond 10 mV_{pp}, the THD remains <1% (acceptable limit in neural-recording applications) for the whole measured amplitude range (150 mV_{pp}). Figure 7 shows the measured DC offset tolerance, indicating that the THD remains well below 1% and the SNDR is close to SNR for a wide DC offset ranging from −68 mV to +68 mV.

Finally, the capability to tolerate movement/stimulation artifacts is demonstrated in Figure 8. In this measurement, a large square signal (60 mV_{pp} amplitude) was superimposed to a small sinewave to emulate the effect of a large stimulation artifact. Such artifacts can commonly happen in bidirectional neural interfaces with concurrent neural recording and stimulation. As shown in the figure, thanks to the wide DR of the design, both the large square artifact signal and the small sinusoidal signal can be recorded without distortion. The small sinusoidal signal information is not lost and can then be recovered in software without degradation. This indicates that when the chip is used in real-life neuromodulation applications, it will be able to record neural signals even in the presence of large stimulation artifacts.

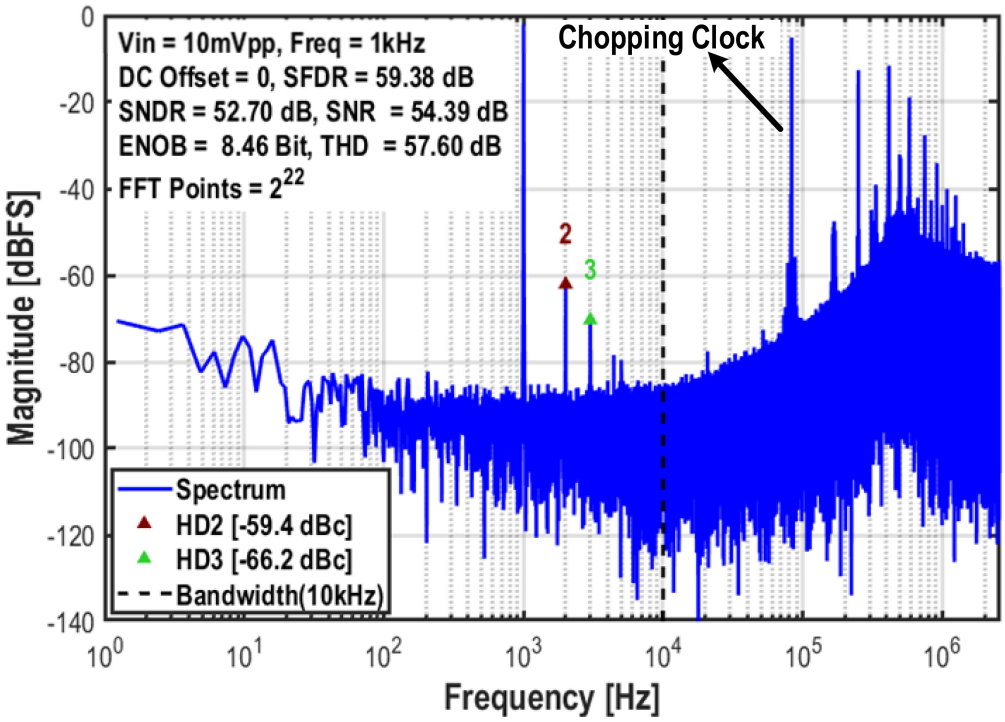


Figure 5. Measured PSD with 1 kHz sine input signal (single channel).

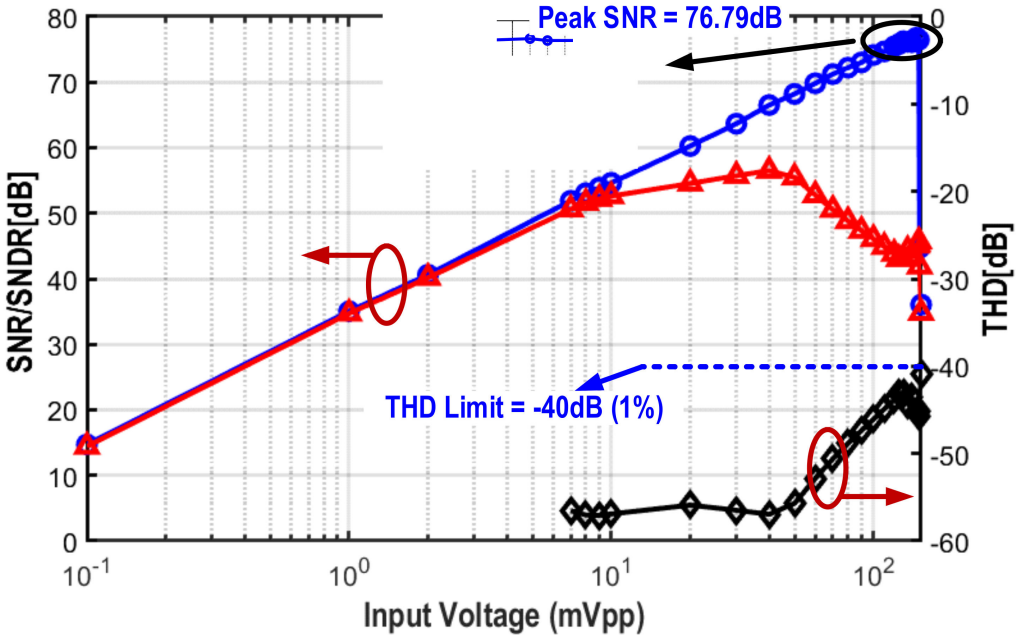


Figure 6. Measured DR over different input amplitudes and 0 mV DC offset (single channel).

Table 2 summarizes the performance of the proposed VCO-based CTDSM and compares it with other direct-digitization neural-recording architectures and VCO-based readouts. Compared with other VCO-based neural-recording circuits [16,24–26], this design achieved a much smaller circuit area, which is critically important in multi-channel neural recording. Compared with the other designs that achieve a small area, this design consumes much less power than the design in Ref. [18] and achieves a much wider input range than that in Ref. [17]. The circuits used for neural interface applications need to meet a wide range of requirements, including area, power, input impedance, and input range, and as is

reflected in the table, this work achieves an excellent compromise between all the important performance metrics.

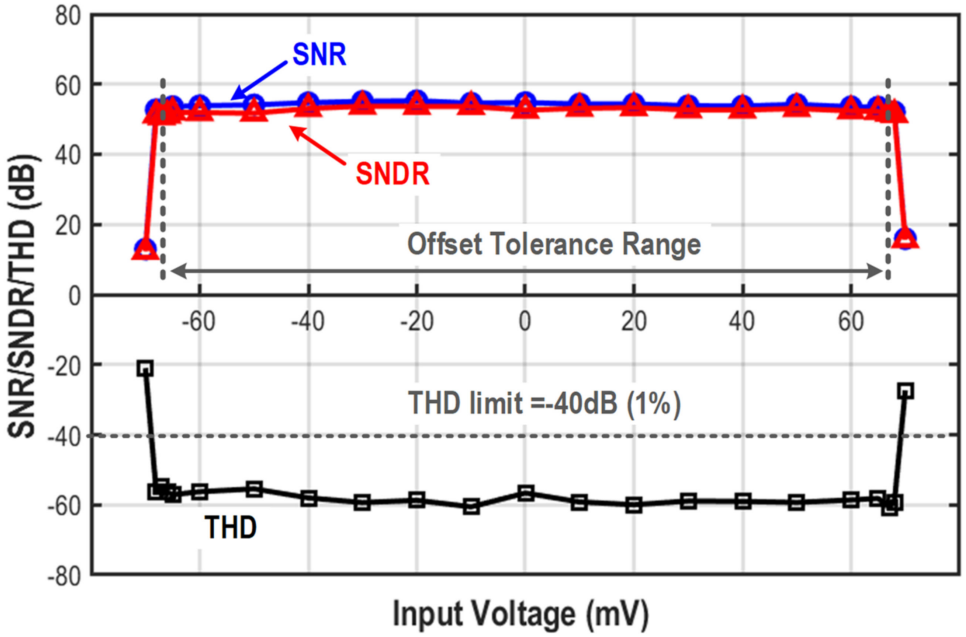


Figure 7. Measured SNDR/SNR/THD with different DC offsets and 10 mV_{pp} sine wave (single channel).

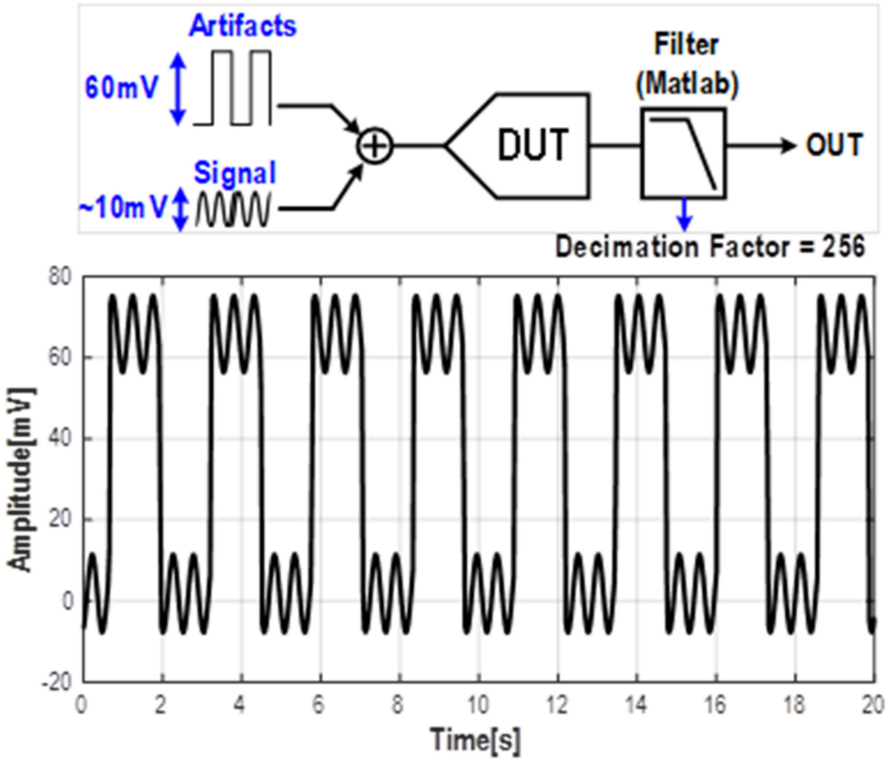


Figure 8. Measured channel output when large transient step (emulating a stimulation artifact) is superimposed to small sine input signal.

Table 2. Comparison with state-of-the-art direct-digitization neural-recording (AP and LFP) architectures and VCO readouts.

Parameters	This Work	[18]	[17]	[16]	[24] ††	[25] ††	[26] ††
Technology	55 nm	55 nm	180 nm	110 nm	40 nm	65 nm	65 nm
Supply voltage (V)	1.2 (Analog)/1.0 (Digital)	1.2	1.8	1.0	0.8 (Analog)/0.6 (Digital)	0.8	0.8
Channel topology	1st-order VCO-based CTDSM	2nd-order Δ-ΔΣ CTDSM	Two-step CT Incremental ΔΣ	2nd-order CTDSM (VCO as 2nd integrator)	2nd-order VCO-PLL hybrid	1st-order VCO-based	3rd-order VCO-based CTDSM
Input Impedance (Ω)	640 M@10 Hz	663 M@10 Hz	∞@DC *	∞@DC *; 13.3 M@10 kHz	222 k ~ 14.2 M *	8 M	Unknown *
Max. input range (mV_{PP})	149	148	15.2	300	100/400	460	1800
THD @1 kHz input	0.09~0.18%@ 10 mV_{PP} AC ± 68 mV DC	0.05~0.44%@ 20 mV_{PP} AC ± 70 mV DC	0.078% @10 mV_{PP}	0.0095% @285 mV_{PP}	0.01% @90 mV_{PP}	<0.002% @460 mV_{PP} (90 Hz)	<0.0025% @1.8 V_{PP} (322 Hz)
Bandwidth (kHz)	10	10	10	10	10	0.5	2.5
AP band noise (μV_{rms})	6.26 †~6.97	5.53	4.46	9.5 (1 Hz~10 kHz) †	3.6 (10 Hz~10 kHz) †	2.6 (10~500 Hz) †	15.8 (1 Hz~2.5 kHz) †
LFP band noise (μV_{rms})	3.54 †~4.52	2.88	2.51				
Power/channel (μW)	13.75 **	48.7	14.62	6.5 **	4.68 **	1.68 **	4.4 **
Area/channel (mm^2)	0.00426 **	0.0077	0.00462	0.078 **	0.025 **	0.056 **	0.1 **

* not measured; ** decimation filter not included; † single-channel operation; †† not optimized for neural recording.

5. Conclusions

This paper presents a scalable VCO-based CTDSM neural-recording architecture that can be used in multi-channel applications. Thanks to the VCO-based approach, this design achieved excellent noise, DR, area, and power consumption performances. We have demonstrated that the VCO oscillation interferences caused by neighboring channels operating simultaneously do not significantly degrade the noise performance. This very promising result opens up the possibility to design scalable neural interfaces that can benefit from the area and power reductions of scaled technologies. The next development step is to implement the digital decimation filter and upscale the number of channels on the chip, as well as to test the chip in in vitro and vivo neural-readout experiments.

Author Contributions: Conceptualization, S.W., A.V. and C.M.L.; methodology, S.W and A.V.; software, X.Y. and C.W.; validation, C.W. and X.Y.; formal analysis, X.Y and C.W.; investigation, all authors; resources, C.M.L.; data curation, X.Y. and C.W.; writing—original draft preparation, S.W.; writing—review and editing, all authors.; visualization, X.Y. and S.W.; supervision, S.W., X.Y. and C.M.L.; project administration, C.M.L. All authors have read and agreed to the published version of the manuscript.

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