# Enabling 3-level High Aspect Ratio Supervias for 3nm nodes and below

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***Abstract*— High aspect-ratio (AR) 3-level Supervias (SV), with a minimum bottom CD of 15.5 nm and AR = 7.7 are successfully integrated in a 3nm node chip. 3-level SV directly connects $M_x$ with $M_{x+3}$ metal layers, without connecting to the intermediate two metal layers. Enabling such high AR SV is achieved by fine tuning the SV etch process to guarantee uniform SV landing and a straight vertical profile. Electrical results show that 3-level Kelvin SVs provide an average resistance of 58 Ω, yielding > 95 % for the best conditions, improving our previously reported yield values of 2-level with enhanced AR [1]. 3-level SVs gave a resistance 13% lower than the conventional 2-level stacked via configuration [2]. Metallization stack used was 0.3 nm of ALD TiOx as an adhesion layer, followed by a Ru CVD deposition of 70 nm. Thermal shock tests of 500 hours, between -50 ℃ and 125 ℃, performed on intervals of 15 min each, showed that the Kelvin resistance values remained virtually unchanged. Therefore, 3-level SV are stable after thermal shock tests, proving that they are a robust scaling booster for the 3nm node.**

***Keywords*— *High-aspect ratio via; Supervia; BEOL; Ru, 3nm node, scaling booster.***

## I. Introduction

As design rules for Back-End of Line (BEOL) and Middle of Line (MOL) layers become more restrictive for smaller nodes, alternative solutions are needed to comply with the constant downscaling, both in terms of chip area per cell unit and in terms of layer thickness of each of the deposited materials. These alternative solutions are known as scaling boosters, and Supervias fall on this category for the 3nm node and beyond. The integration of high AR vias or SV structures may provide several advantages, when compared to a traditional stacked-via approach, like a reduction in resistance and capacitance, leading to an IR-drop, a relaxation on the design constraints, and the possibility to ease the integration process of novel technologies, as in 3D complementary-FET (CFET) devices, as it was reported elsewhere [3]. Our research group previously demonstrated the feasibility of 2-level SV using the same test chip [2], including further development in order to shrink the SV, with increased AR and better control on SV Critical Dimension (CD, in this case SV diameter) [1]. In this manuscript, we extend the SV concept towards a 3-level SV, where two metal levels are skipped, connecting, in our case, M1 metal layer in the BEOL directly to M4. The stack is shown in Fig. 1b. Morphological and electrical results for four different etch processes are reported in this manuscript.

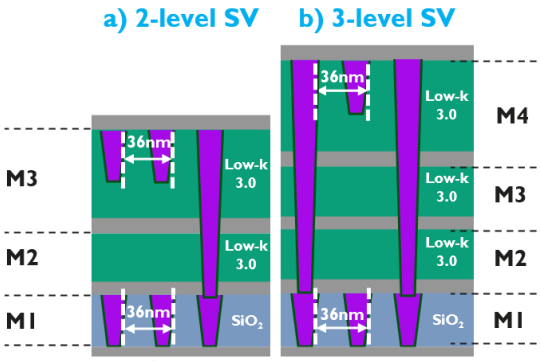


Fig. 1. Stack schematic of 2-level BEOL SV (a) and 3-level SV (b).

## II. Process Integration

In order to simulate a 3-level SV structure, we modified the original test chip stack to include one extra layer, as the test vehicle was originally designed to host 2-level SV only. To speed up the learning cycles, blanket dielectric films were used instead of patterned layers. Therefore, a stack composed of 37 nm of low-k and an etch stop layer of 10 nm of SiCN was used to simulate each of the M2 and M3 layers, as depicted in Fig. 1b. M1 layer was realized through a single-damascene fabrication process, with SiO2 as dielectric and Ru as the metal of choice. Patterning was done by means of EUV lithography step with Line/Space pattern at pitch 36 nm, and line CD of 18 nm. The low-k in M2, M3 and M4 layers is an SiOCH material with a bulk k-value of 3.0 ± 0.1 (Hg-probe). M3 mask (in our experiments, used as M4 layer) uses the same exposure technology as M1 layer, but patterning is done by means of a Dual Damascene (DD) process into the abovementioned low-k. In both M1 and M4 cases, TiN is used as a Hard Mask (HM) to transfer the pattern from the photoresist to the dielectric layers. In the case of M4 patterning, an increased thickness of 30 nm was used to guarantee that the HM would survive during the long SV etch process. Before the DD etch process, trenches are first patterned into TiN, where an average trench CD of 15.3 nm, and a 3σ value of 0.5 nm, were measured using CDSEM inspection. Later, we deposited the lithography stack: Spin-On Carbon (SOC), followed by Spin-On Glass (SOG), and later the photoresist. Wafers are then exposed using argon fluoride immersion lithography process (ArFi). Average SV CD in both X (self-aligned) and Y (non-self-aligned) direction are (60.2, 39.2) nm with 3σ values of (6.1, 3.1) nm respectively. Then, SV are patterned first into the dielectric layers, self-aligned to the TiN lines, going all the way down to the bottom SiCN layer (last layer before M1 Ru layer). It is during this step when TiN HM suffers the most, being the main

challenge of SV patterning. After, SOC is removed dry, exposing the trenches below. For the SV patterning step, we used two different etch chambers, both from Tokyo Electron Limited: the standard chamber, labelled as A and an improved version, labelled as B. Then, the M4 trenches are patterned into the dielectric stack. All wafers used the same chamber A to pattern the trenches, using the Process of Record (POR). Then, TiN HM is removed, and metallization followed, where 0.3 nm of TiO2 were used as an adhesion layer for the 70 nm of CVD Ru. Same metallization scheme was used for both M1 and M4/SV layers. Finally, the wafers go through a Chemical-Mechanical Polishing (CMP) step to enable the metal lines. Lately, electrical properties of SV are characterized using four-probe Kelvin measurements and thermal stress tests.

## III. Morphological Results

TEM and CDSEM techniques are used to characterize the structure and CD of SVs patterned using two different etch chambers. Main parameters to focus on are the SV bottom and top CD (the SV shape), the self-alignment (SA) quality of the SV with respect to the TiN HM, and the percentage of SV landing on M1, a vital aspect that will enable the electrical results shown in the next sub-section.

Figure 2 shows the cross-sectional STEM micrographs, using the High Angle Annular Dark Field (HAADF) detector, of SV processed in chamber A (Fig. 1a) and in chamber B (Fig.1b) after DD etch process but before TiN HM has been removed wet, to better evaluate the SA of the SV with respect to the trenches. In this first iteration, we notice an improved SV profile in the novel chamber B processing, where the sidewall angle is straighter, with less undercut, while CD is also kept much lower, both properties interesting from the integration point of view. A reduced CD allows less M2 lines to be cut [1,2], and therefore, it reduces the interconnect complexity, while a more vertical profile helps reducing the metal voids after Ru filling, resulting in lower SV resistance.

The etch recipe in chamber B was improved in the next iterations, where changes on the SOC recipe, as well as during the ash process (SOC removal after SV etch) were performed to improve the SV SA and landing percentage.

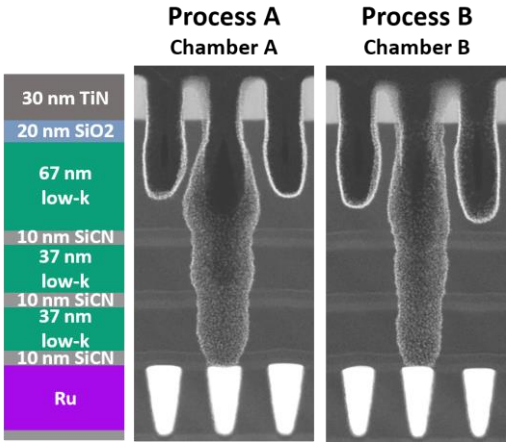


Fig. 2. Stack schematic of 3-level SV structure (left). HAADF-STEM micrographs, of SV processed on chamber A (process A) and the first iteration done on chamber B (process B).

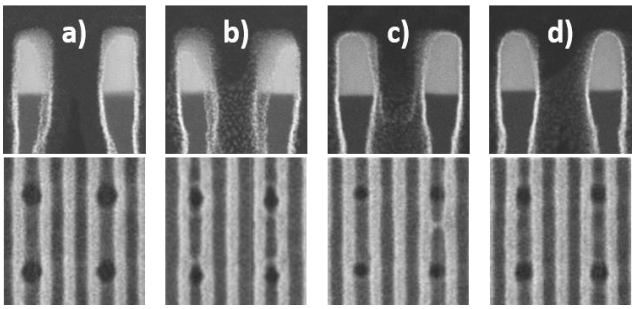


Fig. 3. SV inspection after DD etch, before TiN wet removal. Top row: cross-section HAADF-STEM pictures, focused on Hard Mask erosion. Bottom row: top-down CDSEM pictures after DD and TiN wet removal. From left to right: a) SV etch in chamber A, b) SV etch in chamber B (first iteration), c) SV etch in chamber B (improved SOC etch step), d) SV etch in chamber B (improved SOC and ash etch steps).

Upper row of Fig. 3 shows STEM micrographs after DD etch before TiN removal, focused on the TiN HM shape, to better determine the HM erosion after DD etch (i.e., the SA). We see in Fig. 3a the standard process in the reference chamber. In the first iteration done on the novel chamber B (Fig. 3b), the SA is worsened, due to the SOC etch being too isotropic, leading to SOC undercut and exposing too much TiN to the plasma. By reducing the pressure and lowering the ratio of polymerization gases, the anisotropy of the plasma is improved, and bottom CD at SOC level is back on specification levels, leading to a much better profile, as seen in Fig. 3c. In the first two iterations on chamber B, a significant number of residues was observed between the trenches, likely caused by an incomplete ash process. In the last iteration (Fig. 3d), the RF power of the ash step plasma was increased, aiming to make it more reactive to better remove the residues. Most of them were gone after the last iteration. Top-down CDSEM inspections are displayed in the bottom row of Fig. 3, which help visualize the differences in terms of SA and residue concentration for each of the splits. Further proof of the improved SA can be found on STEM micrographs after Ru filling for the four wafers described in the manuscript (Fig. 4). TEM after Ru filling also helps determining more accurately the % of landing SV onto M1 layer. Main dimensions for each experiment condition are summarized in Table 1.

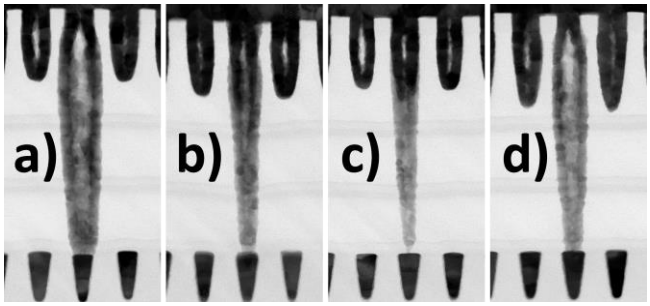


Fig. 4. Annular Bright Field STEM micrographs after Ru metallization. From left to right: a) chamber A baseline, b) chamber B baseline, c) chamber B baseline with improved SOC etch, d) chamber B baseline with improved SOC and ash etch processes.

There is a drawback on the DD etch profile after using the new SOC and new ash processes (process D in the text): the trench depth is increased when compared to other processes, which lowers down the SV height, decreasing in the end the AR. This

effect may be due to the interaction of the more reactive RF plasma with the exposed oxide during the ash process.

Table 1: Bottom and top CD, SV height, AR and percentage of vias connecting M4 to M1, of SV etched using the four different processing conditions described in the text. AR is estimated from the bottom of the trench down to M1 layer.

| Parameter | Supervia morphological properties | | | |
|---|---|---|---|---|
| | ***Process A*** | ***Process B*** | ***Process C*** | ***Process D*** |
| Bottom CD (nm) | 17.3 | 9.2 | 11.2 | 15.5 |
| Top CD (nm) | 23.8 | 21.2 | 22.5 | 22.7 |
| SV height (nm) | 145.0 | 130.4 | 135.4 | 118.5 |
| Aspect Ratio | 8.4 | 14.8 | 12.2 | 7.7 |
| % SV landing | 100 | 56 | 81 | 100 |

Values shown in Table 1 are averaged over a total of 56 SV throughout the whole wafer, which have been automatically extracted using a TEM analysis software. Results indicate a better self-alignment (lower SV top CD) and better sidewall shape on the SV using the new SOC condition (process C), compared to the other conditions. However, the number of SV that are landing is low compared to the best process to record, process D, where even though all CD are larger than in process C, the percentage of landing SV is close to 100 %. Further discussion will follow in the next subsection.

## IV. Electrical Results

### A. *Resistance (R) measurements*

Full wafer average four-point resistance measurements, from Ru-filled kelvin SVs, are plotted in Fig. 5.

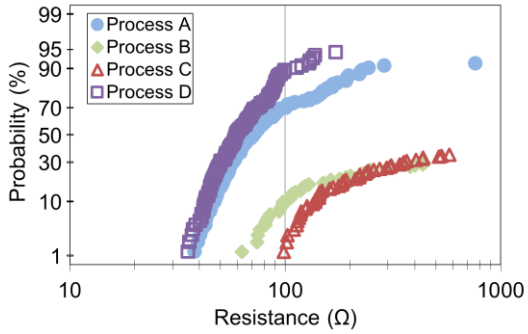


Fig. 5. Kelvin resistance lognormal plot for 3-level SVs processed at different etch conditions.

Table 2: Median SV Kelvin resistance and percentage of electrical yield for each of the etch conditions.

| Parameter | Supervia electrical data | | | |
|---|---|---|---|---|
| | ***Process A*** | ***Process B*** | ***Process C*** | ***Process D*** |
| Resistance (Ω) | 66 | 119 | 183 | 58 |
| % electrical yield | 90 % | 25 % | 30 % | 95 % |

Percentage of electrical yield and average SV Kelvin resistance are summarized in Table 2. Considering the data shown on Table 1 and Table 2, there is a correlation between the electrical yield percentage and the percentage of landing vias. It may point out that SV electrical failure would likely be caused by the non-landing SV, especially at the edge of the wafer and therefore, related to non-uniformity during etch processing. The most remarkable result is the increased electrical yield of the SV etched in chamber B, when etched using the process D, compared to POR process in chamber A (process A). The 95 % electrical yield is our highest reported value ever obtained in a 3-level SV Kelvin structure, surpassing the electrical results of 2-level SV structures with liner deposition and etch back (yield > 70 %) and those of stacked-vias as well (yield > 80 %) [1],[2]. The SA quality, and SV CD of those etched using chamber B are also improved with respect to chamber A, showing the potential of the newest hardware present on the newer chamber B.

### B. *Thermal shock*

Supervias from conditions A and B (baseline on chamber A and the first iteration of chamber B respectively), were exposed to a series of thermal shock tests, aiming to accelerate possible failures in the structures. Samples were submitted to a total of 1000 cycles of temperatures alternating between -50°C and 125°C, with 15 min/cycle at each temperature. After a total of 500 hours, no significant resistance variations were observed, as shown in Fig. 6, indicating a robust integration. These results further support that 3-level SV is a scaling booster approach compatible with the 3nm node technology.

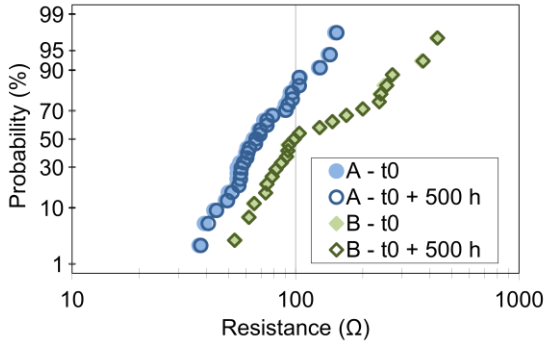


Fig. 6. Thermal shock tests produced no SV failure after 500 hours (1000 cycles) between -50 °C and 125 °C.

## V. Conclusions

Morphological and electrical results of 3-level SV have been demonstrated, using two different etch chambers. The best DD etch condition produced SV with an average bottom CD of 15.5 nm, top CD of 22.7 nm, and an AR of 7.7, where more than 95 % of the SVs yielded, a value that exceeds our previously reported values in 2-level SV with liner deposition. The average resistance value (58 Ω) is 13 % lower than that of a stacked via approach between only two levels (M3 to M1), where 66.3 Ω was measured, showing the significant resistance reduction that can be achieved when using 3-level SV (which connects M4 directly with M1). Thermal shock tests show that no significant damage is found after 500 hours of thermal stress cycles, further supporting that the 3-level SV concept is a robust scaling booster that could be enabled for integrations schemes following the 3nm node rules.

## Acknowledgements

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## References

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[2] V. Vega-Gonzalez et al., IEDM, 2020.
[3] J. Ryckaert et al., VLSI, 2018.