TOKYO ELECTRON

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Enabling 3-level High Aspect Ratio Supervias for 3nm node and below

Daniel Montero, Victor Vega Gonzalez et al.

IITC 2022

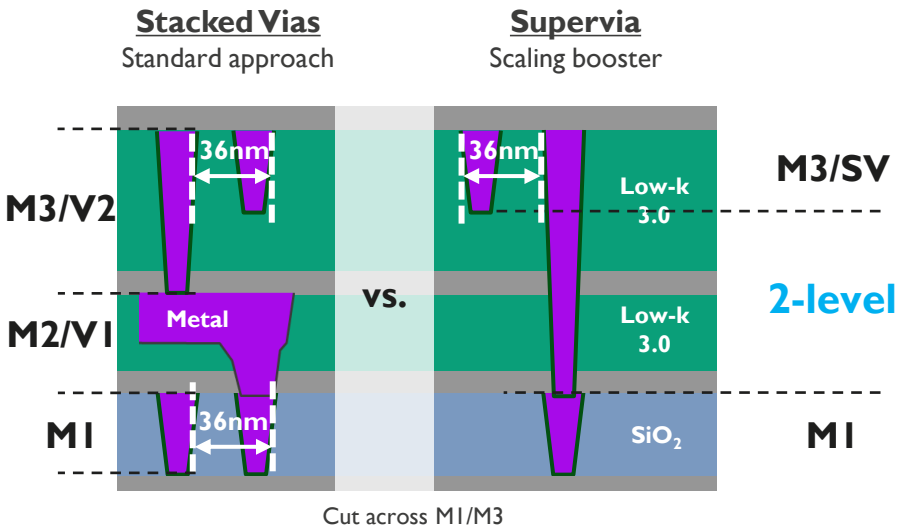
Outline

3-level supervias

- Introduction: What is a Supervia?
- 2-level SV
- Extending the concept → 3-level SV
  - First iteration
  - Failure analysis
  - Second iteration
- Conclusions
- Challenges & future work

What is a Supervia?

BEOL Scaling Booster for 3nm node

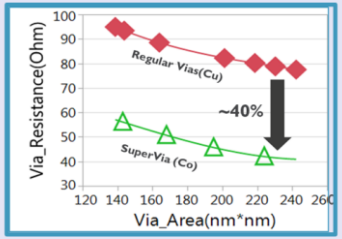


- Supervia: direct connection between M_x and M_{x+2}
- High Aspect Ratio Via
  - **2-level SV**: M3 to M1 → **AR ~ 5**
  - **3-level SV**: M4 to M1 → **AR ~ 10**

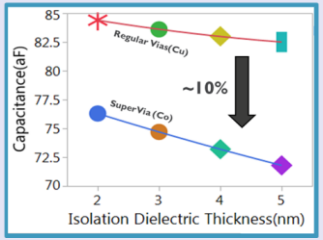
Benefits

(2-level SV)

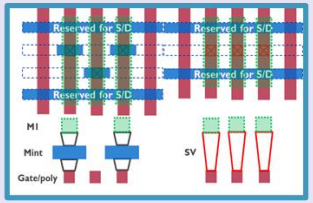
Resistance gain



Capacitance benefits



Relax T2T and minMetal rules



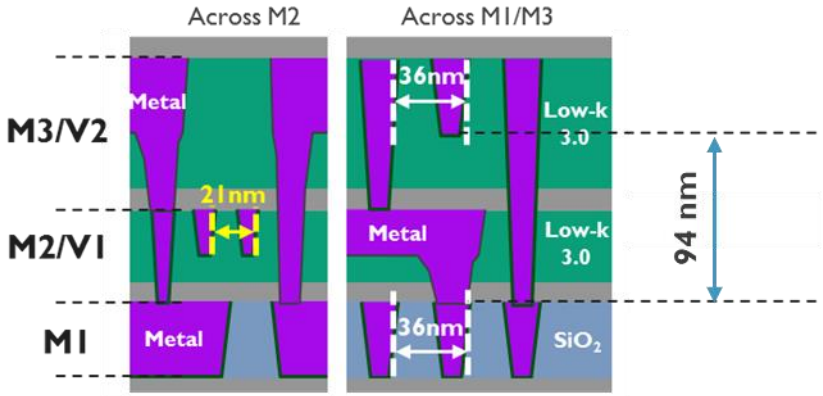
Extending the Supervia concept for 3nm node and beyond

Towards 3-level Supervias

2-level SV

AR ~ 4-5

M3 → M1



M1 & M3 → EUV lithography, P36

M2 → i193 lithography, SAQP P21

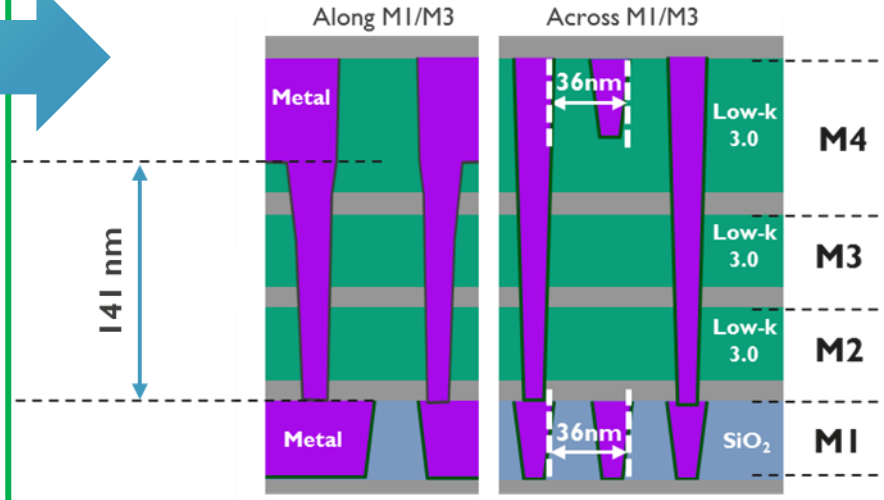
SV → i193 lithography

V2 & V1 → EUV lithography

3-level SV

AR ~ **8-10**

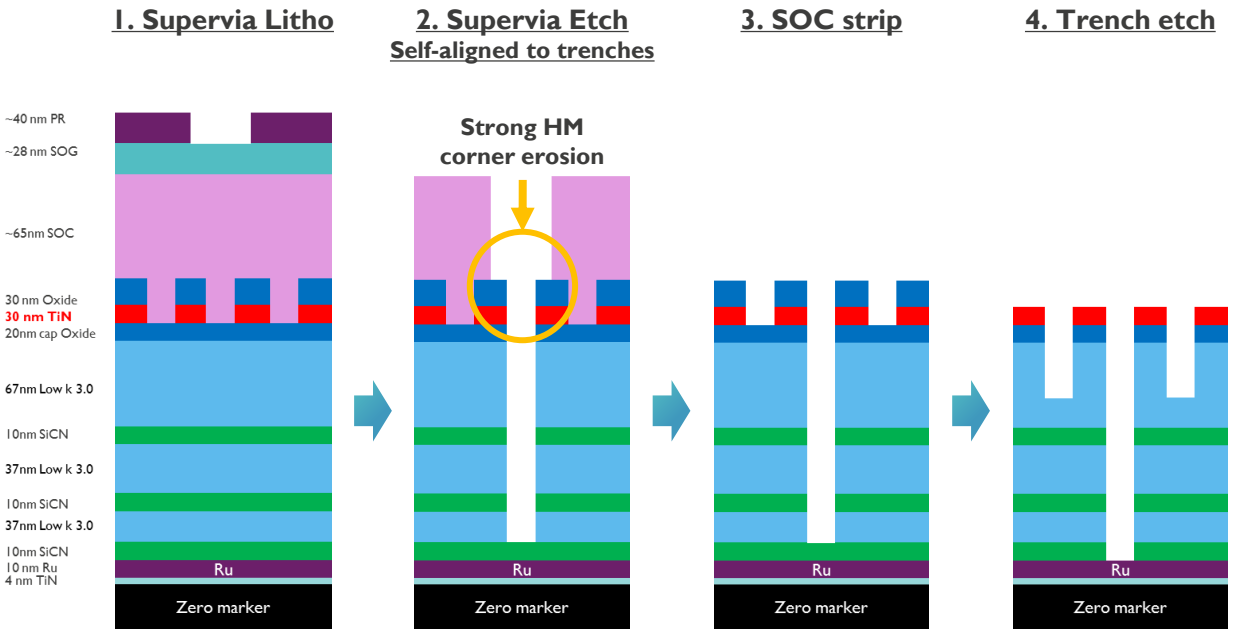
M4 → M1

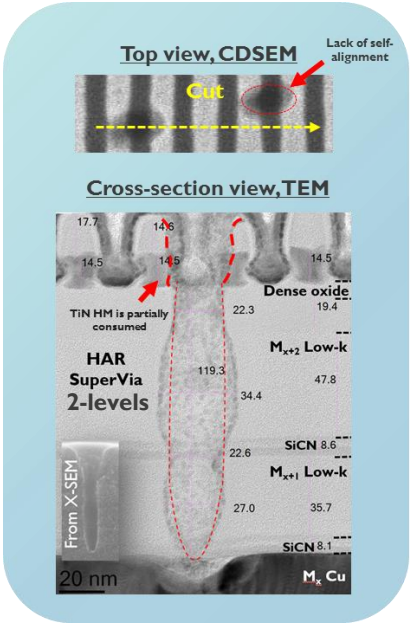


- M4 layer uses M3 EUV mask
- Dummy M2 and M3 layers (no patterning)

Integration flow & patterning challenges

Supervia first, Dual Damascene process





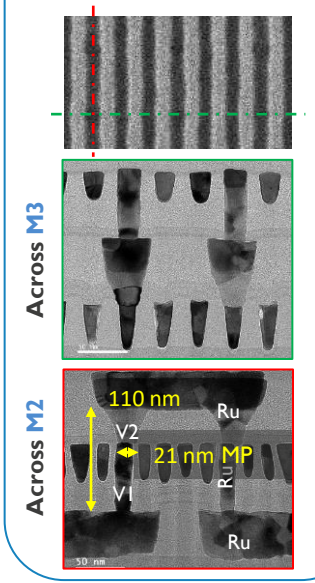
Patterning challenges

- **Selectivity to Hard Mask**
- SV straight profile
- CD control
- Uniformity
- Metal filling

2-level Supervias

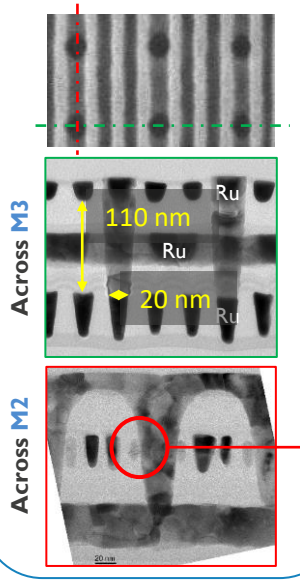
Evolution of 2-level Supervias

Stacked vias



Reference

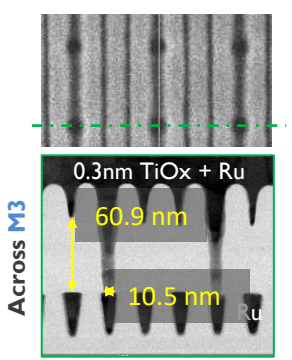
Standard SV[1]



CD_{bottom} = 20 nm
AR = 5.5

Need to control CD
Avoid short-circuit M2

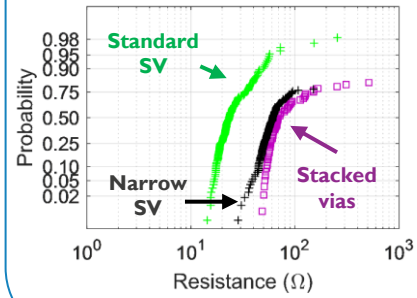
Narrow SV[2]



CD_{bottom} = 10.5 nm
AR = 5.8

Aggressive scaling possible

Resistance measurements



Resistance: 59 % decrease Standard SV vs stacked vias

[1] Supervia Process Integration and Reliability Compared to Stacked Vias Using Barrierless Ruthenium, V. Vega et al. IEDM 2020

[2] Process Integration of High Aspect Ratio Vias with a Comparison between Co and Ru Metallization, V. Vega et al. IITC 2020

3-level Supervias

Towards 3-level SV

Supervia patterning

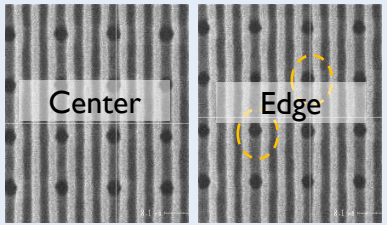
Two different etch chambers

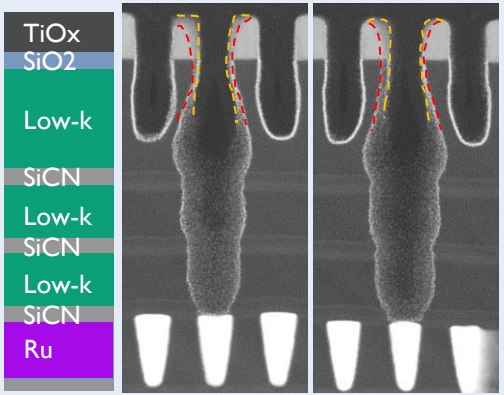
Challenges

- Higher aspect ratio etch
- Keep vertical etch → Control undercut
- Minimize TiN HM erosion

SV etch chamber A

(SV + trench etch)



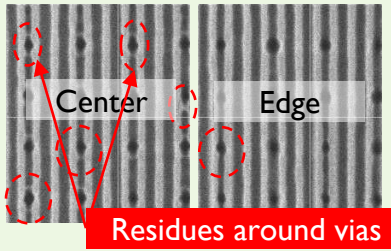


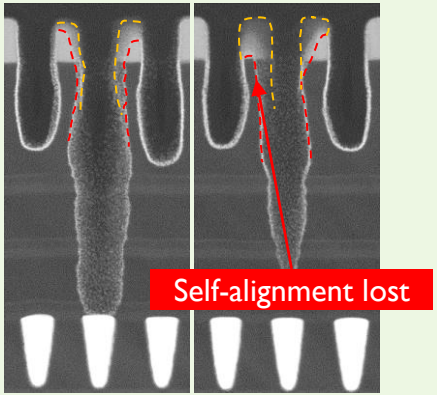
✓ **All vias are landing**

- **Partial Self-alignment loss**

SV etch chamber B

(trench etch in chamber A)





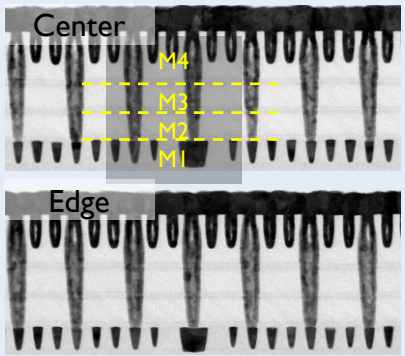
✓ **Controlled undercut**

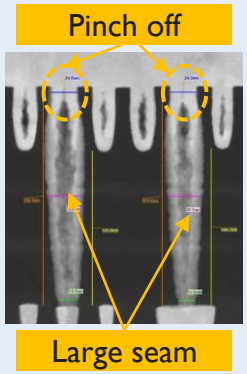
- **Not all vias are landing**
- **Self-alignment lost at wafer edge**
- **Residues around via**

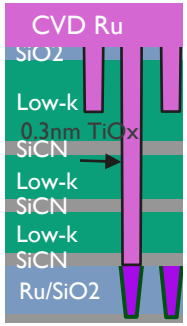
3-level SV: 1st iteration after metal fill

Inspection across M3 trenches

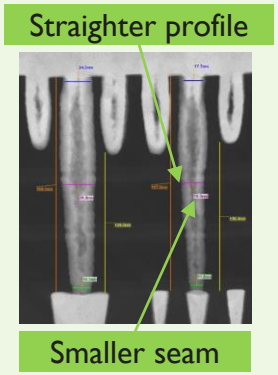
Chamber A

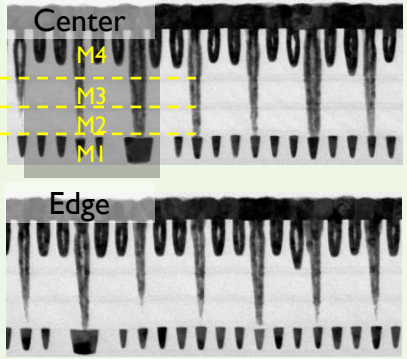




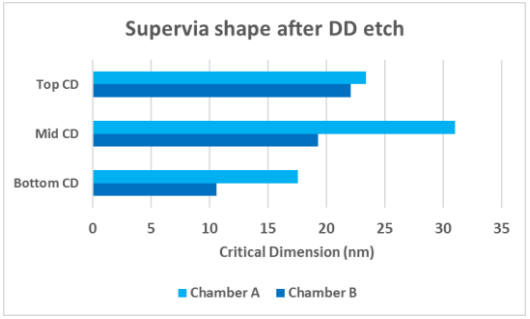


Chamber B





✓ **Good conformality with Ru fill**
- **Vias not fully filled → pinch off**
- **CD_{bottom} = 17.6nm, AR = 8.1**



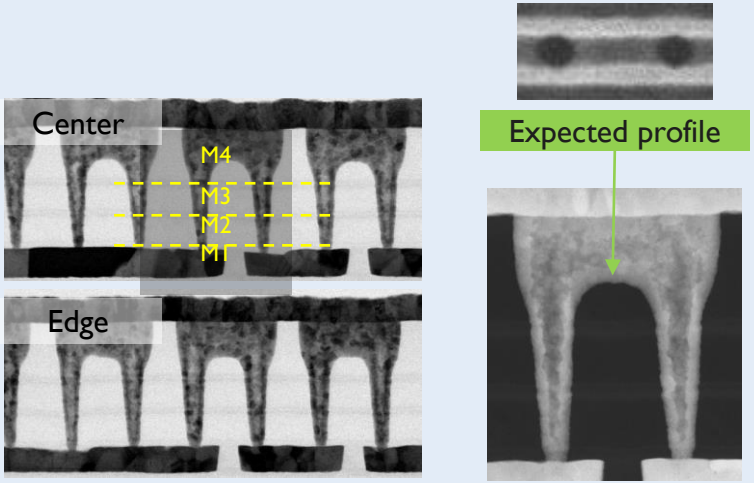
✓ **Straighter profile and higher AR**
✓ **Better Ru CVD fill**
✓ **CD_{bottom} = 10.6nm, AR = 12.3**
- **Not all SV landing**

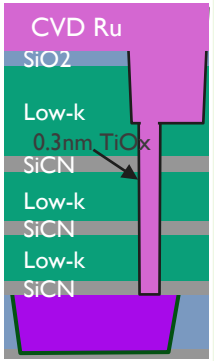
Results averaged over 60 SV per wafer

3-level Supervia: 1st iteration

Inspection along M3 trenches

Chamber A

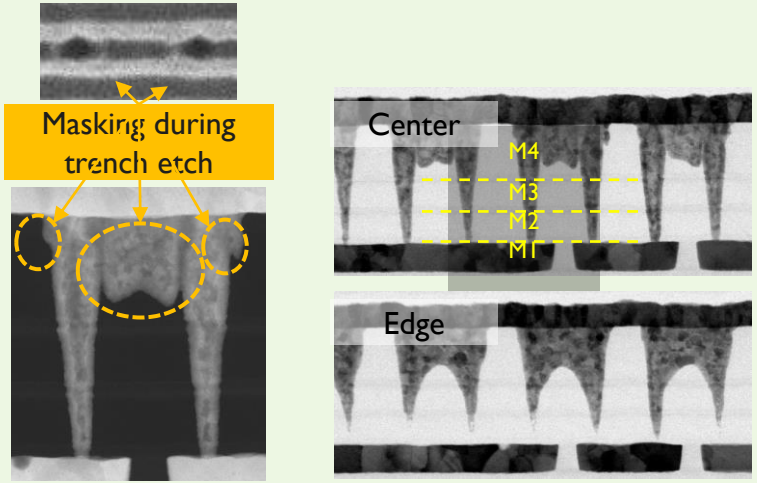




✓ **Expected profile**

- **Some chamfering**

Chamber B

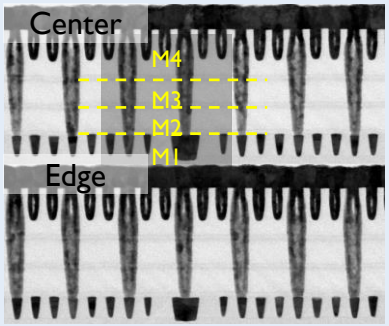


- **Unexpected profile**
- **Trench etch delayed around SVs**

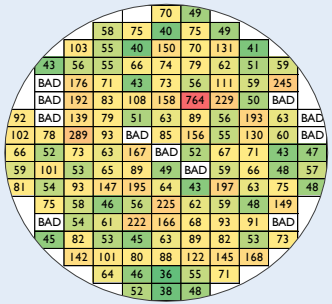
3-level Supervia: 1st iteration

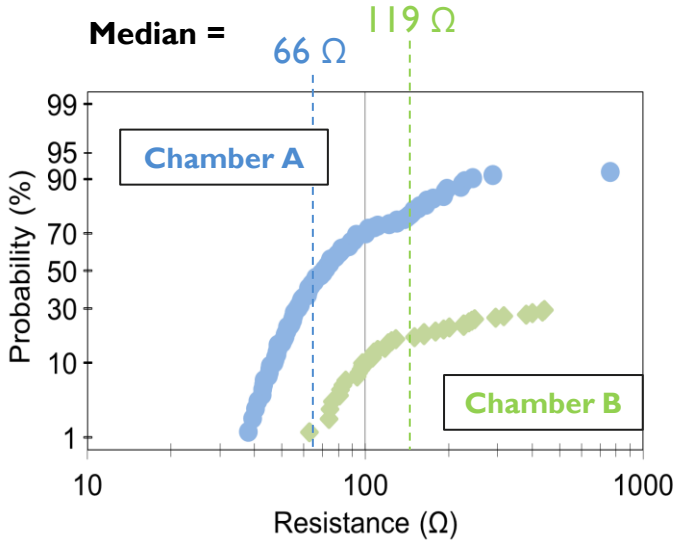
Resistance measurements (Kelvin vias)

Chamber A



Kelvin vias

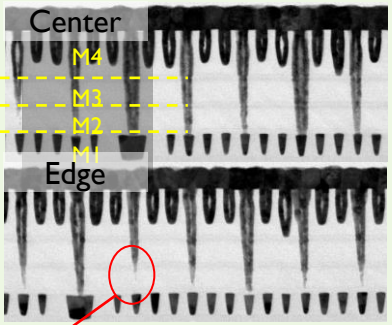




✓ **> 90 % yield chamber A**

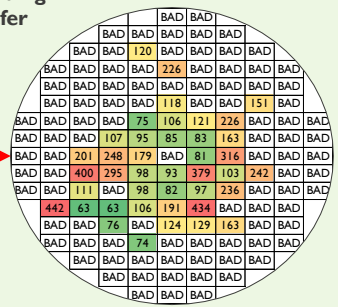
- **25 % yield chamber B**

Chamber B



SV not landing edge wafer

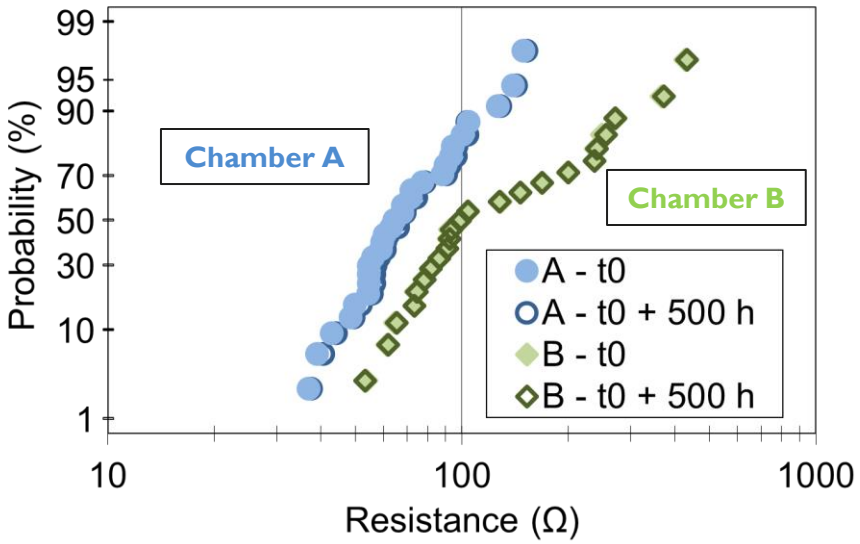
Kelvin vias



3-level Supervia: 1st iteration

Thermal shock tests

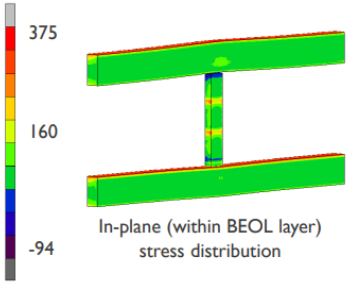
- *Stress conditions:*
  - *[-50°C, 125°C]*
  - *[15,15] min/cycle*
- *Total stress time = 2000cycles (500h)*



- ✓ **No impact on SV resistance after 500 h**
- ✓ **Good integration**

Stress simulations

**Courtesy of Houman Z.*

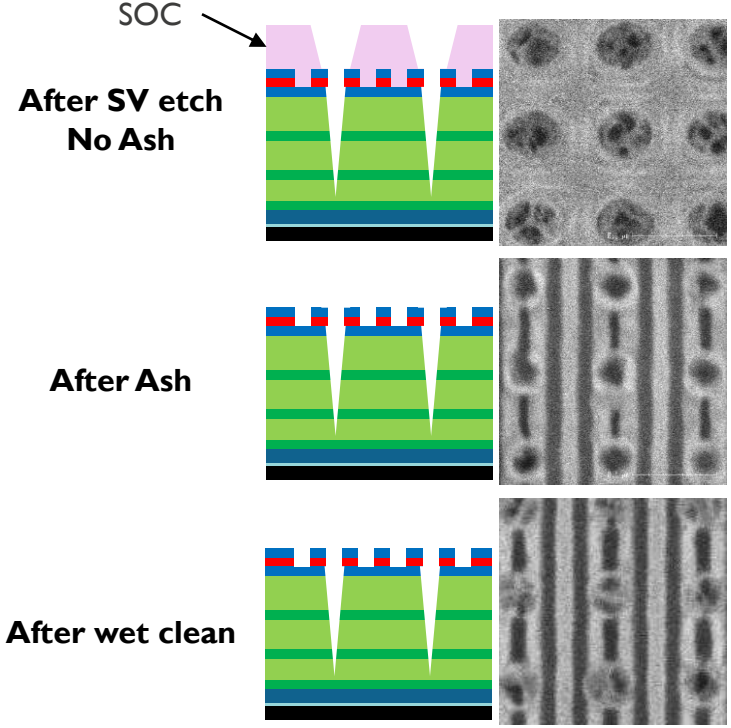


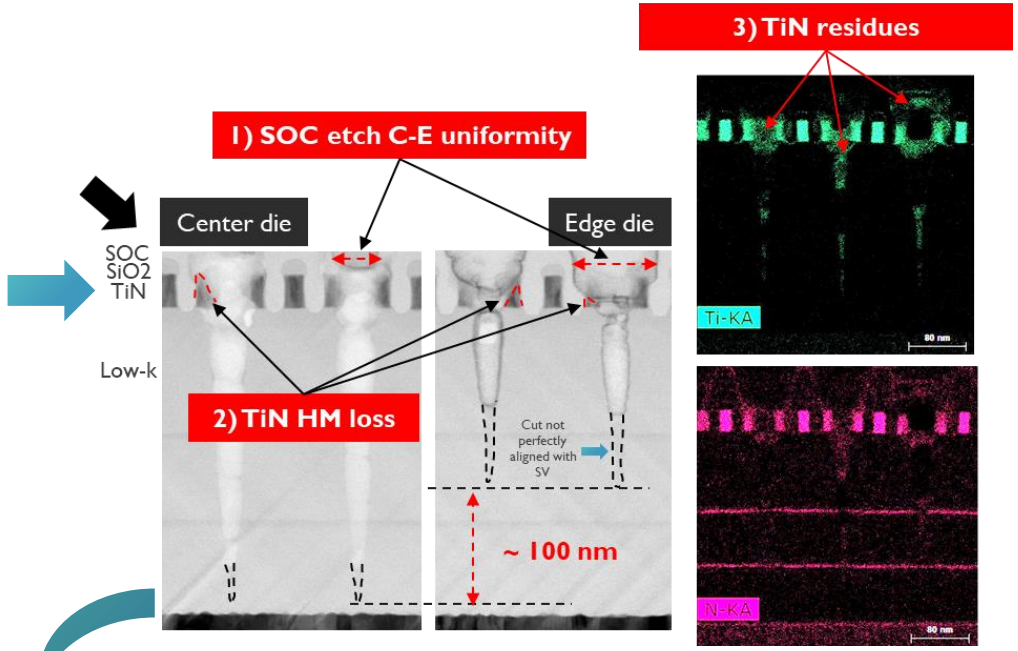
Higher stress on lines than on vias due to in-plane constrains

Improving results on chamber B

SV failure analysis: chamber B

Partition of supervia etch



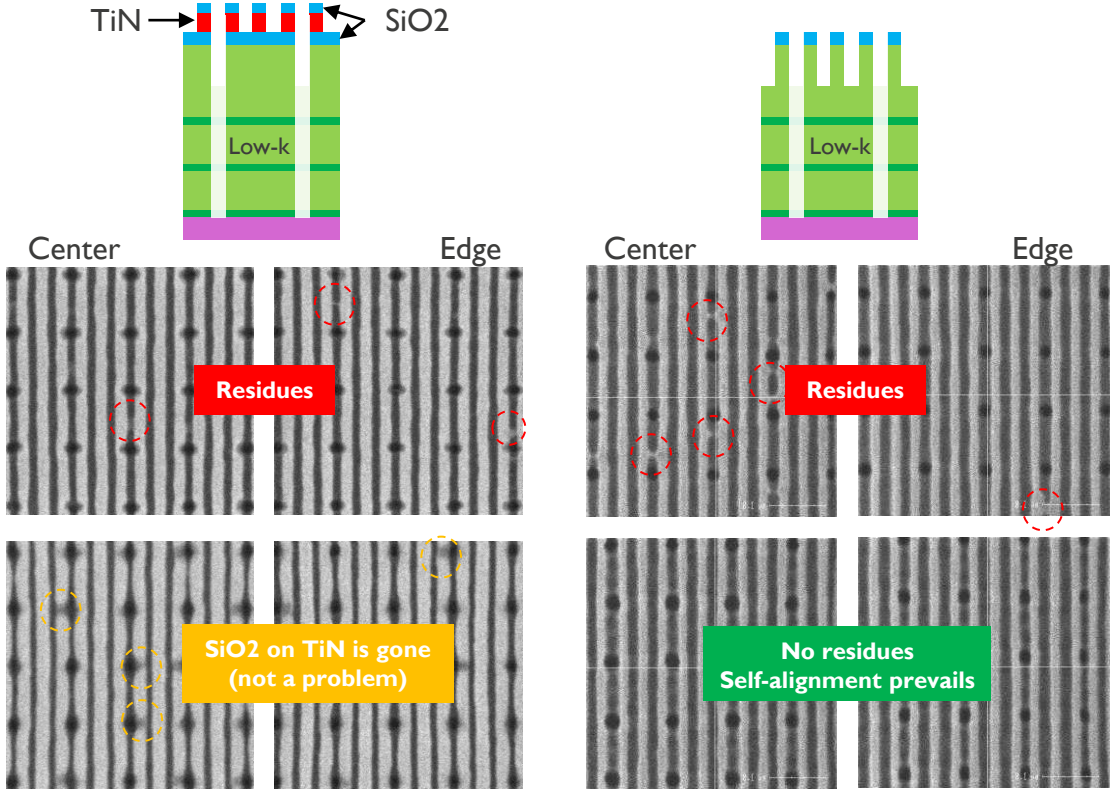


1. High CD @ SOC etch @ wafer edge
2. Too much TiN exposed
3. TiN is sputtered
4. TiN residues block SV etch

2nd iteration: etch improvements

SV etch in chamber B

+ trench etch in chamber A



New SOC
(better wafer uniformity and higher TiN selectivity)

New SOC + new ash
(more aggressive ash)

An aggressive SoC ash is required to remove residues

2nd iteration: morphological results

SV etch in chamber B + trench etch in chamber A

Previous iteration

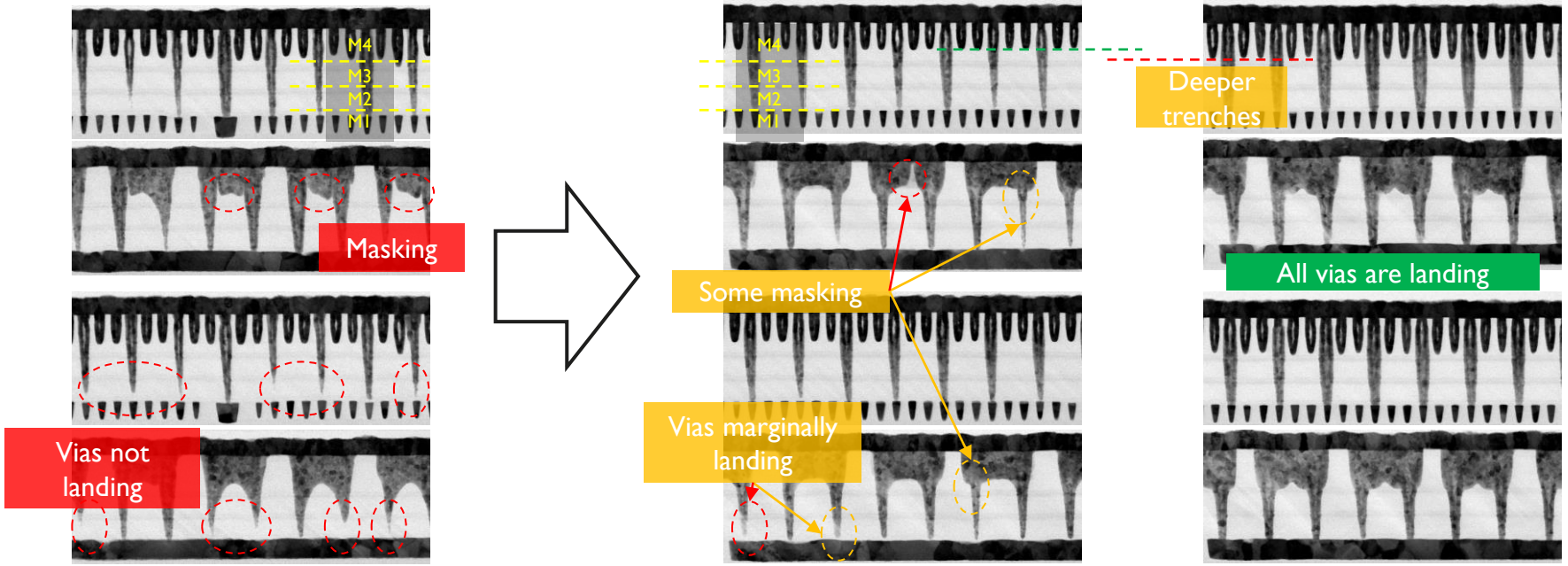
- CD $_{bottom}$= 10.6nm
- AR= 12.3

New SOC

- CD $_{bottom}$ = 11.1nm
- AR= 12.1

New SOC + new ash

- CD $_{bottom}$= 15.5nm
- AR= 7.6



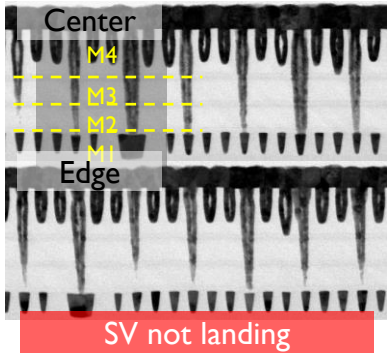
New SoC/ash etch improved uniformity, with less residues, but deeper trenches

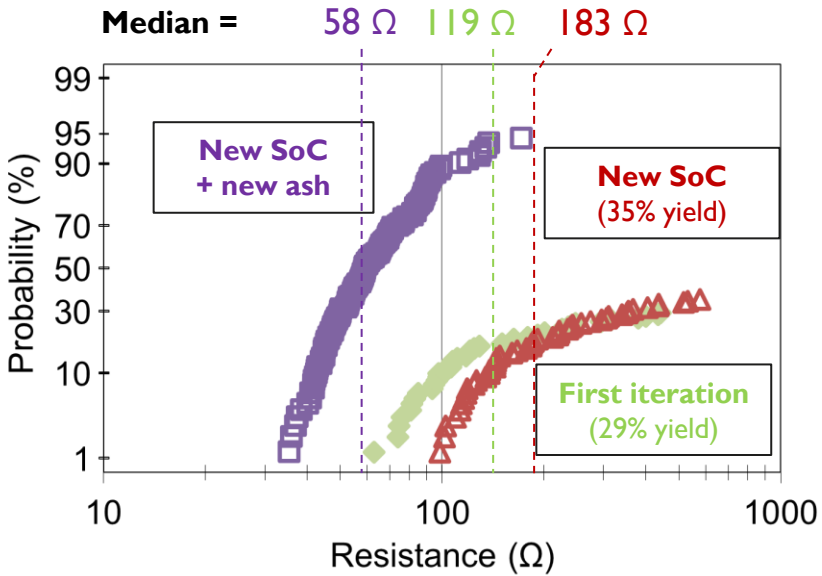
1st vs. 2st iteration: chamber B

Resistance measurements (kelvin vias)

First iteration

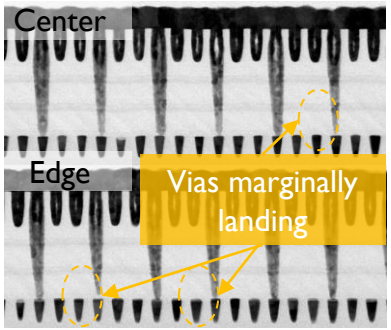
Old SOC etch & ash



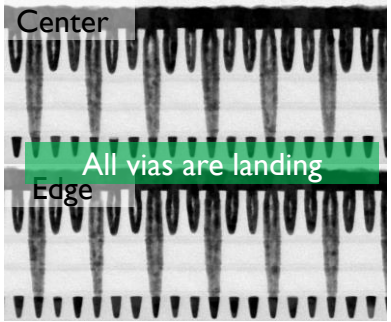


Second iteration

New SoC



New SoC + new ash

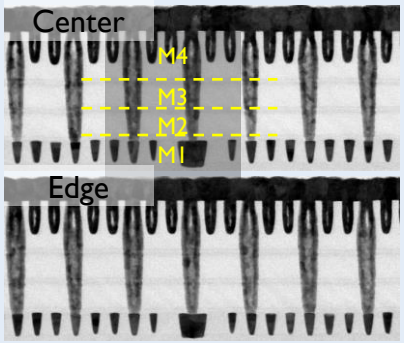


Higher yield obtained from second iteration

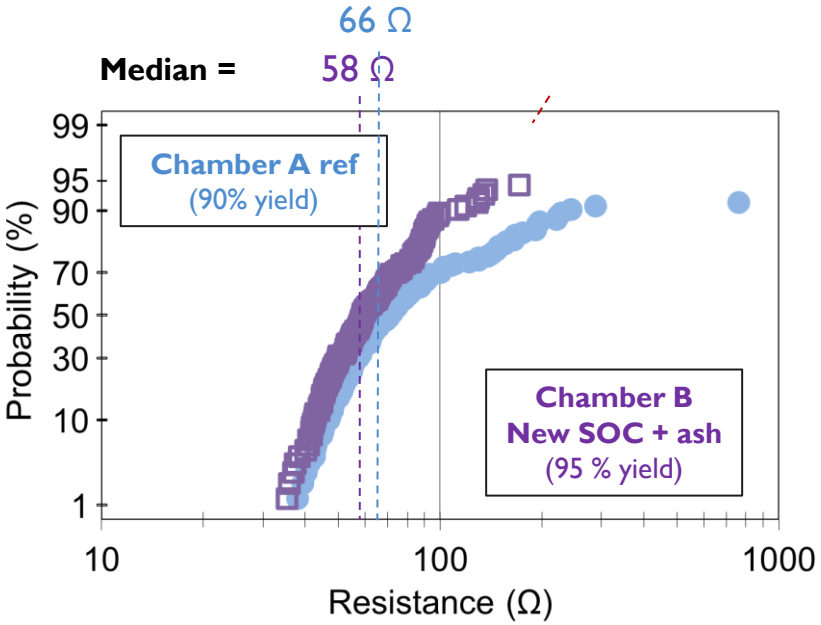
Final comparison: chamber A vs chamber B

Resistance measurements (kelvin vias)

Chamber A reference

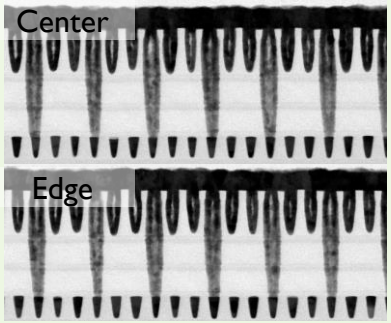


CD_{bottom} = 17.6nm
AR = 8.1



Chamber B

New SoC + new ash

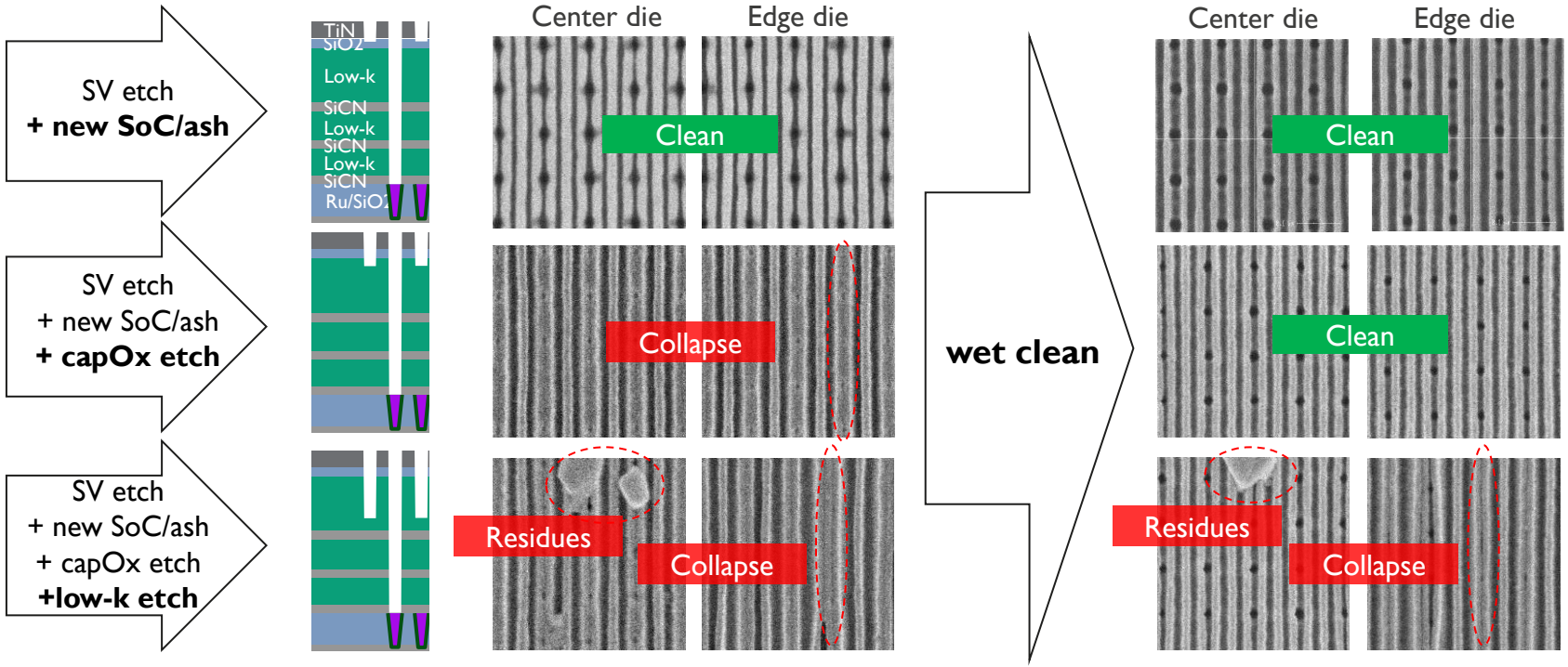


CD_{bottom} = 15.5nm
AR = 7.6

✓ **Chamber B: lower CD, higher yield and lower resistance**

Towards full integration in chamber B

SV + trench etch in Chamber B

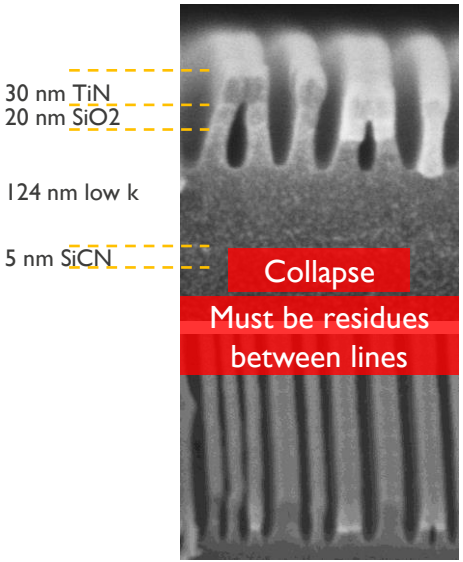


Ti-based residues after trench etch, wet clean can help

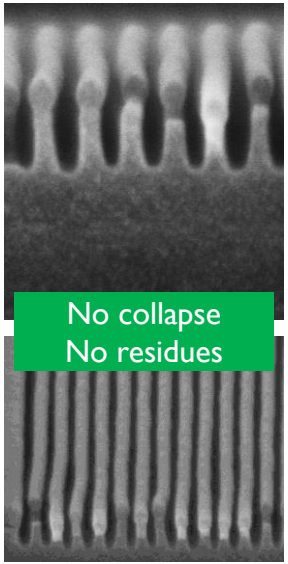
Improving line collapse on chamber B processing

Coupon tests, etch into low-k

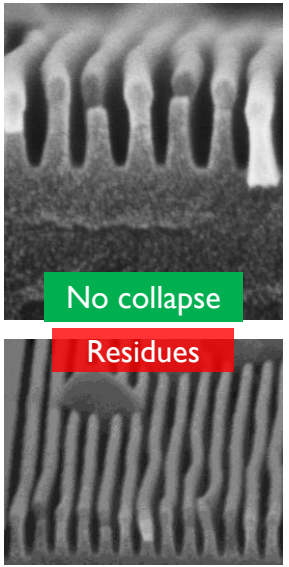
Low-k etch



Low-k etch
+ **post-etch treatment A**



Low-k etch
+ **post-etch treatment B**



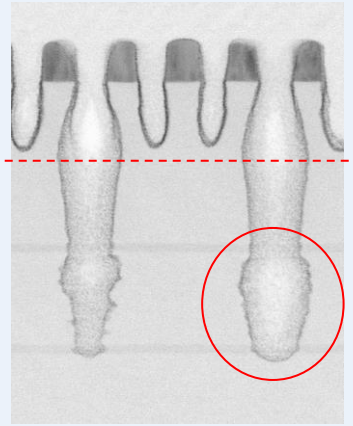
Post etch treatments are promising to remove residues and prevent line collapse

Improving line collapse full wafer

Interaction between trench etch and Supervia profile

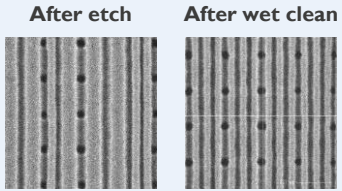
Low passivation

Trench etch



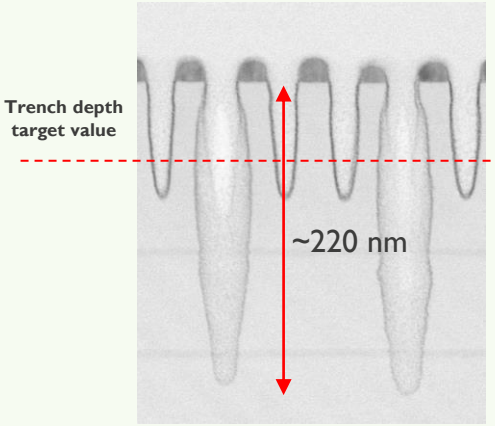
- After etch
  - Line collapse
- After wet clean
  - Line restored
- Good self-alignment
- SV damaged

Selectivity TiN ~ 8



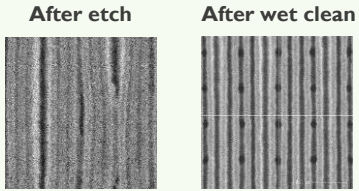
High passivation

Trench etch



- After etch
  - Line collapse
- After wet clean
  - Line restored
- Good self-alignment
- **Straigth SV profile**
- Less TiN selectivity

Selectivity TiN ~ 4.5



Good candidate for next iterations

Conclusions

3-level Supervias

- ✓ 3-level SV successfully patterned
- ✓ Chamber B shows better results (2nd iteration)
  - Advantages
    - High AR ~ 7.6
    - Self-alignment
    - Bottom CD ~ 15.5 nm
    - Electrical yield > 95 %
    - Low resistance 58 Ω
  - But...
    - More Ti-based residues → improve cleaning strategies
- ✓ Thermal shock tests are ok after 500 hours of stress
- Towards DD etch in chamber B
  - Trench etch challenging → residues
  - Combine PET + wet clean → best results

Outlook

3-level SV

- Improve selectivity to TiN Hard Mask
- Reduce residue formation
- Adjust trench depth to target
- Extend the concept to 4-level SV (uber-vias)

Outline

3-level Supervias

- Introduction: What is a Supervia?
- 2-level SV
- Extending the concept → 3-level SV
  - First iteration
  - Failure analysis
  - Second iteration
- Conclusions
- Challenges & future work

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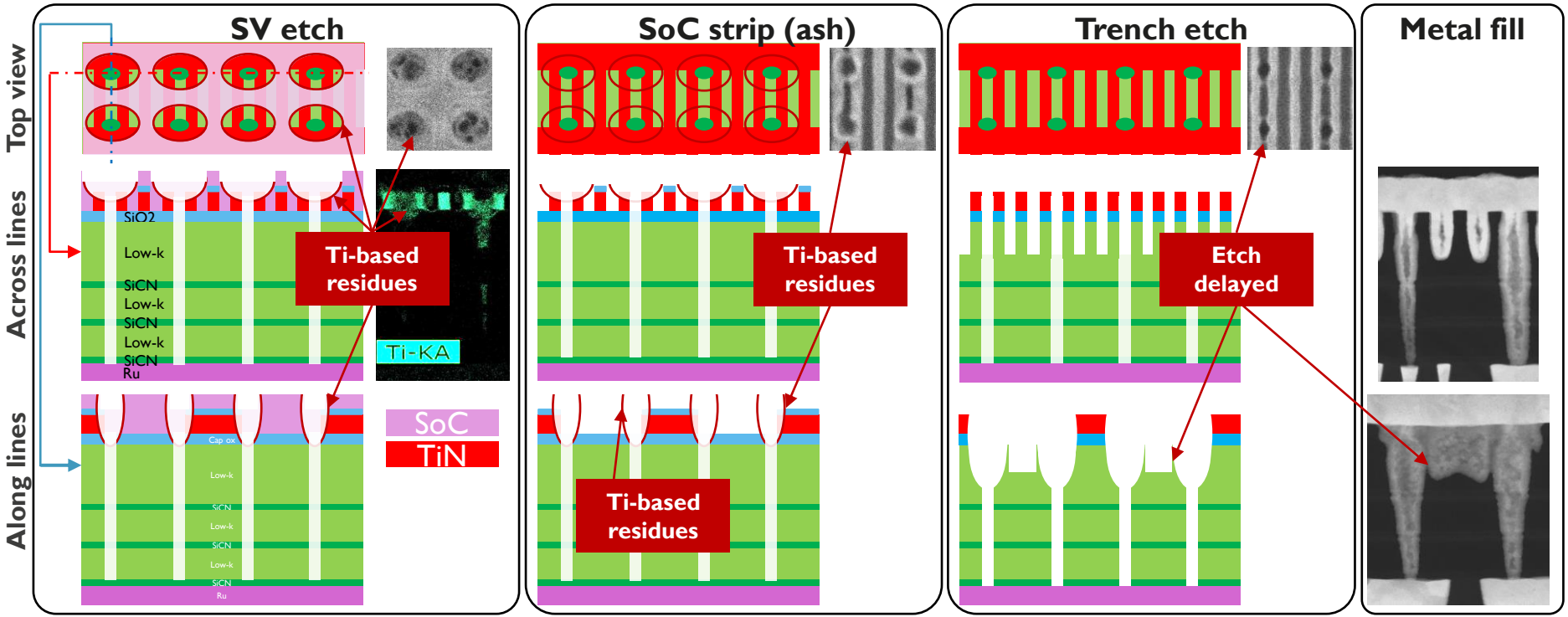
Partners/Suppliers

embracing a better life

Back-up slides

SV failure analysis: chamber B

Atypical profile along trenches explained



TiN residues on SV walls delay the trench etch