MFA-MTJ Model: Magnetic-Field-Aware Compact Model of pMTJ for Robust STT-MRAM Design

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***Abstract*—The popularity of perpendicular magnetic tunnel junction (pMTJ) based STT-MRAMs is growing very fast. The performance of such memories is very sensitive to magnetic fields including both internal and external ones. This article presents a magnetic-field-aware compact model of pMTJ, named as MFA-MTJ model, for magnetic/electrical co-simulation of MTJ/CMOS circuits. Magnetic measurement data of MTJ devices, with diameters ranging from 35 nm to 175 nm, is used to calibrate an in-house magnetic coupling model. This model is subsequently integrated into our developed compact pMTJ model, which is implemented in Verilog-A. The superiority of the proposed MFA-MTJ model for device/circuit co-design of STT-MRAM is demonstrated by simulating a single pMTJ as well as STT-MRAM full circuits. The design space is explored under PVT variations and various configurations of magnetic fields.**

***Index Terms*—STT-MRAM, MTJ model, circuit simulation**

I. Introduction

SPIN-TRANSFER torque magnetic random access memory (STT-MRAM) is a next-generation non-volatile memory technology for a variety of applications such as enterprise SSD, industrial-grade MCU, automotive, and AIoT [1]. In recent years, its commercialization progress towards both discrete and embedded memories has accelerated with heavy investments from major semiconductor companies worldwide. For example, Everspin first commercialized discrete STT-MRAM (64 Mb) chips in 2015 and started shipping 1 Gb parts in 2019 [2]. SK hynix [3], Samsung [4], Globalfoundries [1], and TSMC [5] all revealed their STT-MRAM solutions in recent years and claimed they are production ready. Similar to the development process of all semiconductor products, STT-MRAM design, design automation, and test using commercial computer-aided design tools play a critical role. The data-storing elements in STT-MRAMs are magnetic tunnel junction (MTJ) devices, which are inserted between two adjacent metal layers in the back-end-of-line process [6]. MTJ devices are typically selected, programmed, and read out using CMOS-based circuits. Therefore, it is crucial to develop a SPICE-compatible compact MTJ model which accurately captures both the *magnetic and electrical characteristics* of MTJ with reasonable simulation overhead for fast and robust STT-MRAM design.

Several MTJ models with different features and implementation methods have been introduced in the literature [7–14]. Generally, they can be classified into four categories: 1) micro-magnetic models, 2) commercialized-tool-based models, 3) macro models, 4) behavioral models [7]. Micro-magnetic MTJ models are implemented using micro-magnetic simulation tools such as OOMMF, which offers high simulation accuracy and is able for studying the switching dynamics of a single MTJ [8]. The commercialized-tools-based models such as Sentaurus Device provide decent simulation accuracy of a single MTJ as well as small MTJ/CMOS circuits [9]. Macro MTJ models are composed of SPICE built-in circuit elements such as resistors, capacitors, and voltage-/current-dependent voltage/current sources [10]; this type of MTJ model owns good compatibility with circuit simulators, but the number of circuit elements dramatically increase with the complexity of MTJ's dynamic characteristics. Behavioral MTJ models describe the analog behaviors of MTJ using a hardware description language such as Verilog-A; they gain popularity for circuit-level simulations due to several advantages including: 1) good compatibility with circuit simulators, 2) fast simulation, 3) flexible configuration with input parameters, and 4) easiness of designing, sharing, and upgrading. In view of this, many Verilog-A MTJ models have been presented and improved over the past decade [11–15]. Nevertheless, these MTJ models were not capable of simulating magnetic coupling effects and external field disturbance on MTJ's performance, which poses a critical constraint for STT-MRAM designs as reported with silicon characterization data in [1,16,17].

This article presents a versatile compact pMTJ model: MFA-MTJ model, which is Magnetic-Field-Aware for SPICE-based hybrid MTJ/CMOS circuit simulations. It is well recognized that MTJ retention and switching characteristics are very sensitive to all sources of magnetic fields including internal intra-cell and inter-cell stray fields and external disturbance fields in the operating environment. Therefore, we have developed a physics-based analytical model for stray fields in STT-MRAMs [17]. Building on top of this work, we propose the MFA-MTJ model, which to our knowledge is the first work which enables *magnetic/electrical co-simulation* of MTJ-based spintronic circuits under various sources of magnetic fields. The main contributions are listed as follows.

- Present magnetic characterization results of MTJ devices fabricated at IMEC with diameters from 35 nm to 175 nm.
- Integrate the above model into a Verilog-A compact MTJ

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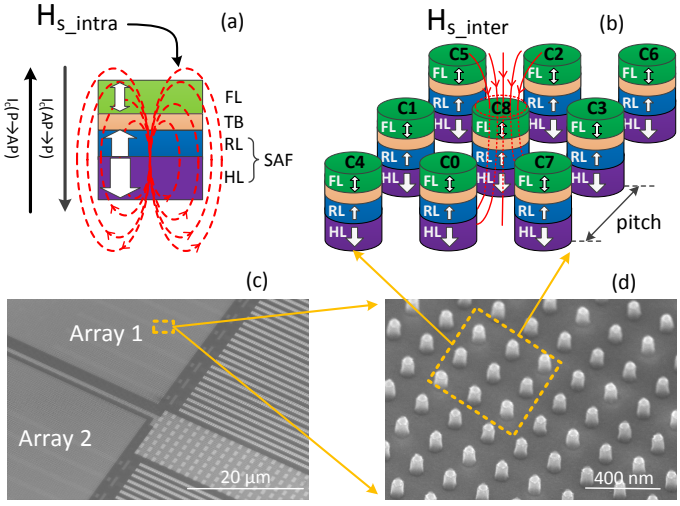


Fig. 1. (a) MTJ stack and the intra-cell stray fields from the RL and HL, (b) 3×3 MTJ array and the inter-cell stray fields from neighboring cells, (c) SEM image of the 0T1R wafer floorplan, and (d) SEM image of MTJ array.

model for SPICE-based circuit simulation which is aware of device size, array pitch, and magnetic fields.

- Use the proposed MFA-MTJ model to explore the design space of STT-MRAM with peripheral circuits under PVT variations and different magnetic configurations.

The rest of this paper is organized as follows. Section II provides a background on STT-MRAM technology. Section III presents magnetic characterization data. Section IV evaluates the impact of internal fields on MTJ's performance indicators such as the switching current and time. Section V integrates the proposed model into our MFA-MTJ model and details its implementation. Section VI elaborates MTJ electrical characteristics by performing DC and transient simulations of MFA-MTJ model. Section VII demonstrates electrical/magnetic co-simulation of STT-MRAM full circuits and explores its design space under various variation sources. Section IX concludes this paper.

II. Background

In this section, we first introduce the MTJ stack design and its working principles. Thereafter, we introduce three sources of magnetic fields including intra- and inter-cell stray fields internally from STT-MRAM arrays and external disturbance fields that may arise from the working environment.

A. MTJ Structure and Working Principles

Magnetic tunnel junction (MTJ) devices are the data-storing elements in STT-MRAMs. Each MTJ device stores one-bit data in the form of binary magnetic configurations. Fig. 1a shows the MTJ stack which essentially consists of four layers: FL/TB/RL/HL. The *hard layer* (HL) is composed of $[Co/Pt]_x$, which is used to pin the magnetization in the upper *reference layer* (RL). The RL is generally built up with a Co/spacer/CoFeB multilayer, which is anti-ferromagnetically coupled to the HL. These two layers form a *synthetic anti-ferromagnetic* (SAF) structure, providing a strong fixed reference magnetization in the RL. The *tunnel barrier* (TB) layer is made of dielectric MgO, typically ∼1 nm. The *resistance-area* (RA) product is commonly used to evaluate the TB resistivity, as it depends on the TB thickness but not the device size. The CoFeB-based *free layer* (FL) is the data-storing layer where the magnetization can be switched by a spin-polarized current. Note that the magnetization is perpendicular to the FL of MTJ (i.e., pMTJ); pMTJ offers better scalability towards smaller sizes and less write power, as opposed to the counterpart with in-plane magnetization [6]. Therefore, we limit our discussions to pMTJ which dominates today's STT-MRAM designs in industry.

To work properly as memory devices, MTJs need to provide read and write mechanisms, which are realized by the *tunneling magneto-resistance* (TMR) effect and the *spin-transfer-torque* (STT) effect [18]. Due to the TMR effect, the MTJ's resistance is low (R_{P}) when the magnetization in the FL is parallel to that in the RL, while the resistance is high (R_{AP}) when in anti-parallel state (see Fig. 2). For STT-MRAM, the low resistance state (LRS) represents logic '0', while the high resistance state (HRS) represents logic '1'. If the write current magnitude (with sufficiently long pulse width) is larger than the *critical switching current* I_{c}, the magnetization in the FL can switch to the opposite direction. It is a fundamental parameter to characterize the switching capability by current. The STT-induced switching behavior also depends on the current direction, as shown in Fig. 1a. I_{c}(AP→P) can be significantly different from I_{c}(P→AP) due to the bias dependence of STT efficiency and external field disturbance [18]. In addition, the *average switching time* t_{w} [19] is another critical parameter, which is inversely correlated with the write current. In other words, the higher the write current over I_{c}, the less the time required for the magnetization in FL to flip. In practice, t_{w}(AP→P) can also differ from t_{w}(P→AP) depending on the write current magnitude and duration.

In addition, enough retention time is required for STT-MRAMs depending on the target application. Storage applications require >10 years typically, while cache applications only necessitate ms-scale retention time [20]. an STT-MRAM retention fault occurs when the magnetization in the FL of the MTJ flips spontaneously due to thermal fluctuation. Thus, the STT-MRAM retention time is generally characterized by the *thermal stability factor* (Δ) [18]. The higher the Δ, the longer the retention time.

B. Three Sources of Magnetic Field Disturbance

STT-MRAM performance is vulnerable to magnetic fields, which may arise from the following three sources.

1) Intra-cell stray field $\boldsymbol{H}_{\mathbf{s\_intra}}$: To obtain high TMR and strong interfacial perpendicular magnetic anisotropy (iPMA), our MTJ devices were annealed at 375 °C for 30 min in a vacuum chamber under the perpendicular (out-of-plane) magnetic field of 20 kOe. Once the ferromagnetic layers (i.e., FL, RL, and HL) in the MTJ stack are magnetized, each of them inevitably generates a stray field in the space. Fig. 1a illustrates the intra-cell stray field $\boldsymbol{H}_{\mathbf{s\_intra}}$ perceived at the FL, generated by the RL and HL together; its in-plane component

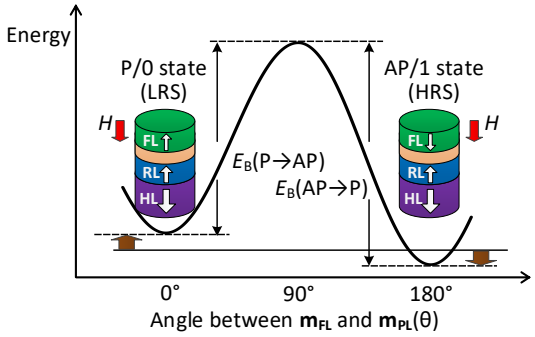


Fig. 2. Energy barrier E_B between AP and P states is bifurcated into E_B(P→AP) and E_B(AP→P) due to magnetic field H at the FL.

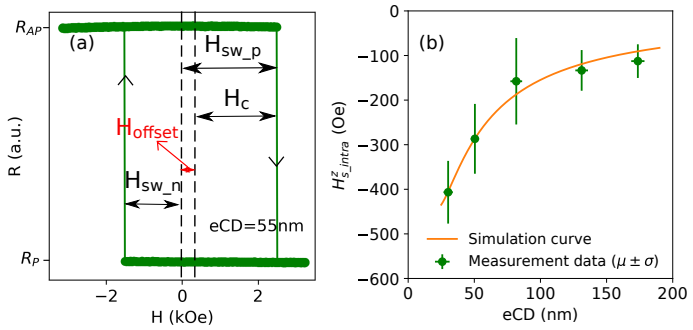


Fig. 3. (a) Measured R-H hysteresis loop, (b) device size dependence of $H^z_{\text{s\_intra}}$: measured vs. simulated.

$H^{x-y}_{\text{s\_intra}}$ is marginal [21], while its out-of-plane component $H^z_{\text{s\_intra}}$ at the FL has a significant influence on the energy barrier E_{B} between the P and AP states [22]. For example, if $H^z_{\text{s\_intra}}$ has the same direction as the magnetization in the FL in AP state, it leads to an increase in E_{b}(AP→P) and a decrease in E_{b}(P→AP), as illustrated in Fig. 2. The bifurcation of E_{B} along the two switching directions has a significant impact on the retention and the STT-switching characteristics of MTJ devices, as reported in [21,23]. In the extreme case where $H^z_{\text{s\_intra}}$ exceeds the FL *coercivity* H_{c}, defined as the reverse field needed to drive the magnetization of a ferromagnet to zero, the bistable states disappear [24].

2) Inter-cell stray field $\boldsymbol{H_{\text{s\_inter}}}$: As the density of STT-MRAMs increases, the spacing between neighboring MTJ devices becomes narrower (i.e., smaller pitch). This makes stray fields from neighboring cells not negligible any more [22,25]. Fig. 1b shows a 3×3 MTJ array, where the eight cells C0-C7 (aggressors) surrounding cell C8 (victim) in the center inevitably generate an inter-cell stray field $\boldsymbol{H_{\text{s\_inter}}}$ acting on the victim cell. Fig. 1c and Fig. 1d show the scanning electron microscope (SEM) images of our 0T1R wafer floorplan and MTJ array, respectively.

3) External disturbance field $\boldsymbol{H_{\text{ext}}}$: When being deployed in the field, STT-MRAM products may be subject to external magnetic fields unintentionally or maliciously in the operating environment. These unexpected disturbance fields further bifurcate E_{B} shown in Fig. 2, thus causing data retention and write errors when $\boldsymbol{H_{\text{ext}}}$ reaches a certain extent [16]. Lee *et al.* [26] observed with silicon measurements that the sensitivity of switching voltage V_{c} to $\boldsymbol{H_{\text{ext}}}$ was ∼8%/500Oe; with a 300 µm-thick shield at package level, the V_{c} sensitivity was reduced to ∼3%/500Oe. Naik *et al.* [1] demonstrated STT-MRAM with 500 Oe magnetic immunity by boosting write voltage and adding 2-bit ECC.

III. Characterization of Intra-cell Stray Field

$H^z_{\text{s\_intra}}$ can be extracted from R-H hysteresis loops. Fig. 3a shows a measured R-H hysteresis loop for a representative MTJ device with the HL/RL configuration shown in Fig. 1a. During the measurement, an external field was applied perpendicularly to the device under test. It was ramped up from 0 Oe to 3 kOe, then it went backwards to −3 kOe and finished at 0 Oe. In total, we measured 1000 field points, each of which was followed by a read operation to read out the device resistance with a voltage of 20 mV. The same measurement was repeated ten cycles and an example of a representative R-H loop averaged over the measured ten cycles is shown in Fig. 1a. It can be seen that the MTJ device switches from AP state (high resistance) to P state (low resistance) when the field reaches at $H_{\text{sw\_p}}$, and it switches back to AP state at a negative field $H_{\text{sw\_n}}$. The device coercivity can be obtained by $H_{\text{c}} = (H_{\text{sw\_p}} - H_{\text{sw\_n}})/2$. Due to the existence of stray fields at the FL, the loop is always offset to the positive side for the device configuration in Fig. 1a. The offset field H_{offset} is equal to $(H_{\text{sw\_p}} + H_{\text{sw\_n}})/2$, as shown in the figure. Since H_{offset} is essentially equivalent to the extra external field applied to cancel out $H_{\text{s\_intra}}$, the relation of these two parameters is $H_{\text{s\_intra}} = -H_{\text{offset}}$. Given the fact that the *resistance-area* (RA) product does not change with the device size, the *electrical Critical Diameter* (eCD) of each device can be derived by [27]: $eCD = \sqrt{\frac{4}{\pi} \cdot \frac{RA}{R_{\text{P}}}}$, where RA=4.5 Ω·µm^2 (measured at blanket stage) for this wafer, and R_{P} can be extracted from the R-H loop (i.e., the lower horizontal line in Fig.3a). The calculated eCD for the device in Fig.3a is 55 nm.

In this way, we can obtain $H^z_{\text{s\_intra}}$ and eCD for MTJ devices with different sizes on the same wafer. The measurement results are shown in Fig. 3b. The error bars indicate the device-to-device variation in the the measured values due to process variations and the intrinsic switching stochasticity. Note that the switching stochasticity inevitably introduced measurement errors in the stray fields, thus amplifying its standard deviation as seen in the figure. This is because the intra-cell stray fields were calculated from the measured switching fields $H_{\text{sw\_p}}$ and $H_{\text{sw\_n}}$ which have cycle-to-cycle variations due to the switching stochasticity. A key observation is that the smaller the device size (i.e., smaller eCD), the higher $H^z_{\text{s\_intra}}$; the trend even tends to grow exponentially for eCD<100 nm. This is because the stray fields generated by the ferromagnets below FL are approximately proportional to $\frac{1}{\text{eCD}^2}$ when maintaining the same H_{k} and M_{s} at blanket level before etching. Similar results were shown using micromagnetic simulations in [23,24]. The solid curve in the figure represents simulation results which will be explained in the next section.

IV. Impact of Internal Stray Fields on MTJ Performance

In this section, we first briefly discuss our stray field model proposed in [17]. Thereafter, we use the proposed model to

evaluate the impact of internal stray fields on the critical switching current I_c and the average switching time t_w. We also investigate the impact on the thermal stability factor Δ in a similar way. Simulation results for MTJ devices with eCD=35 nm are presented as an example.

A. Internal Stray Field Modeling

To analyze and quantify the effects of magnetic fields on the MTJ's performance, we need to first develop an accurate model to cover all the three sources of magnetic field disturbance as mentioned in Subsection II-B. $\boldsymbol{H_{ext}}$ originates from the external surroundings thus is independent on any STT-MRAM design; it can be directly fed into a Verilog-A MTJ model as an input parameter. In contrast, $\boldsymbol{H_{s\_intra}}$ and $\boldsymbol{H_{s\_inter}}$ both depend on STT-MRAM designs, thus requiring an accurate stray field model. To this end, we first modeled and calibrated $\boldsymbol{H_{s\_intra}}$ for isolated MTJ devices using bound current theory and Biot-Savart law. Thereafter, we extrapolated this model to derive $\boldsymbol{H_{s\_inter}}$ for an memory array with various pitches. The modeling details can be found in our prior work [17].

It is worth noting that our stray field model is able to take into account the initial angle θ_0 between the magnetization ($\boldsymbol{m_{FL}}$) of the FL and the z-axis. Due to the thermal fluctuation effect, the direction of $\boldsymbol{m_{FL}}$ may deviate from the z-axis with an initial angle θ_0, which we model using the following equation [28,29].

$$\theta_0 = \sqrt{\frac{k_B T}{\mu_0 M_s V H_k}}, \tag{1}$$

where μ_0 is the vacuum permeability, T the temperature, k_B is the Boltzmann constant, M_s is the saturation magnetization, V is the volume of the FL, and H_k is the magnetic anisotropy field. Since θ_0 is induced by the thermal fluctuation, its value is intrinsically random. Therefore, we assigned a Gaussian distribution to it. We then took it into account in our stray field simulations by tilting the bound current loop representing $\boldsymbol{m_{FL}}$ by an angle away from the z-axis.

B. Impact on the Critical Switching Current

Under the influence of stray field, I_c can be expressed as follows [18]:

$$I_c(H^z_{\text{stray}}) = \frac{1}{\eta}\frac{2\alpha e}{\hbar} M_s \cdot V \cdot H_k \cdot (1 \pm \frac{H^z_{\text{stray}}}{H_k}), \tag{2}$$

where η is the STT efficiency, α the magnetic damping constant, e the elementary charge, $\hbar$ the reduced Planck constant, M_s the saturation magnetization, V the volume of the FL, H_k the magnetic anisotropy field. The sign in the parentheses is '+' for I_c(P→AP) and '−' for I_c(AP→P), given the definition of coordinates in this paper. In Equation (2), $H^z_{\text{stray}} = H^z_{\text{s\_intra}} + H^z_{\text{s\_inter}}$ can be calculated with our proposed magnetic coupling model taking into account both intra-cell and inter-cell stray fields, while H_k needs to be extracted from measurement data. the other parameters in the equation are measured at blanket stage before etch. Since the switching points (i.e., H_{sw_p} and H_{sw_n} in Fig. 3a) are intrinsically stochastic, we measured the R-H loop of the same device for 1000 cycles to obtain a statistical result of the switching probability at varying fields. With the technique proposed in [30], we are able to extract H_k and Δ_0 by performing curve fitting. Δ_0 is the intrinsic thermal stability factor without any stray field at the FL; it will be used in the next subsection. By doing this for a large number of devices, we obtained $\Delta_0 = 45.5$ and $H_k = 4646.8$ Oe (both in median) for devices with eCD=35 nm.

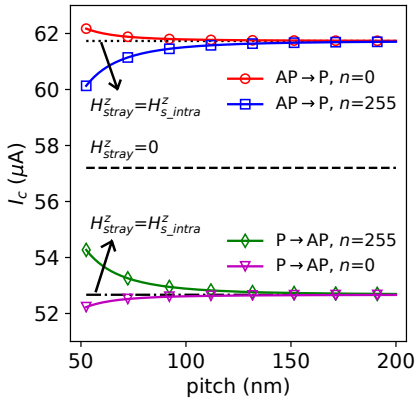


Fig. 4. I_c vs. pitch under the circumstance of different stray fields.

Fig. 4 shows the critical switching current I_c for C8 (for both P→AP switching and AP→P switching) at different pitches with respect to various stray fields. For isolated devices without any stray field (i.e., ideal case, $H^z_{\text{stray}} = 0$), the intrinsic I_c for the two switching directions is supposed to show no difference; $I_c = 57.2\,\mu$A. When taking into account the intra-cell stray field (i.e., $H^z_{\text{stray}} = H^z_{\text{s\_intra}}$), a static shift in I_c is introduced, making I_c(AP→P)=61.7 μA (i.e., 7% above the intrinsic I_c) and I_c(P→AP)=52.8 μA (i.e., 7% below). When considering both intra-cell and inter-cell stray fields (i.e., $H^z_{\text{stray}} = H^z_{\text{s\_intra}}$+$H^z_{\text{s\_inter}}$) for different neighborhood patterns NP_8, the impact on I_c shows a clear dependence on the array pitch. I_c(AP→P) becomes larger at smaller pitches when NP_8=0, while it shows an opposite trend when NP_8=255. This indicates that the variation in I_c(AP→P) between different neighborhood patterns increases as the pitch goes down. It can be seen that at pitch≈80 nm (corresponding to $\Psi = 2\%$), the variation is marginal. Similar observations can be seen on the P→AP switching direction.

C. Impact on the Average Switching Time

The average switching time t_w in the presence of H^z_{stray} in the precessional regime (namely, switched by the STT-effect) can be estimated using Sun's model [31] as follows:

$$t_w(H^z_{\text{stray}}) = \left(\frac{2}{C + \ln(\frac{\pi^2\Delta}{4})} \cdot \frac{\mu_B P}{em(1+P^2)} \cdot I_m\right)^{-1}, \tag{3}$$

$$I_m = I_{MTJ} - I_c(H^z_{\text{stray}}). \tag{4}$$

Here, C≈0.577 is Euler's constant, μ_B the Bohr magneton, P the spin polarization, e the elementary charge, and m the FL magnetization. I_{MTJ} is the current flowing through the MTJ device. Note that we assume the STT switching statistics obey a normal distribution, as shown with silicon data and simulation results in [32,33]; the variance increases with t_w.

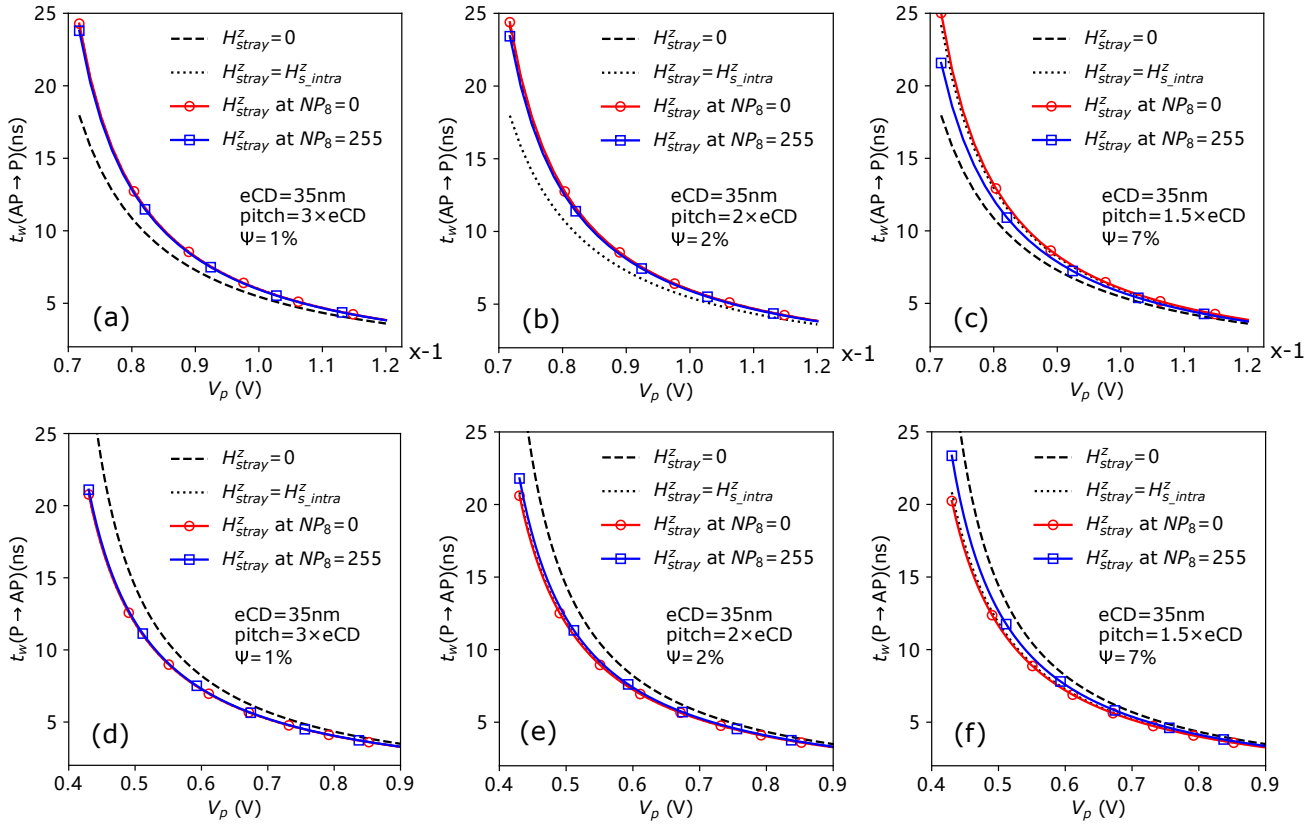


Fig. 5. Impact of internal stray fields on the voltage dependence of $t_{\rm w}$ with eCD=35 nm at various pitches: (a) 3×eCD, AP→P switching, (b) 2×eCD, AP→P switching, (c) 1.5×eCD, AP→P switching, (d) 3×eCD, P→AP switching, (e) 2×eCD, P→AP switching, and (f) 1.5×eCD, P→AP switching.

Therefore, we consider the impact of stray fields $H^z_{\rm stray}$ on the switching stochasticity by incorporating $H^z_{\rm stray}$ into $t_{\rm w}$ and keeping the same dependence of the variance on $t_{\rm w}$.

Fig. 5a-5c show the voltage dependence of the average switching time from AP state to P state ($t_{\rm w}$(AP→P)) for MTJs with eCD=35 nm at pitch=3×eCD, 2×eCD, and 1.5×eCD, respectively. It can be seen that $t_{\rm w}$(AP→P) becomes larger for MTJ devices in the presence of internal stray field $H^z_{\rm stray}$ (solid lines), comparing to devices without any internal stray field (dashed lines). It is worth noting that the larger the voltage, the smaller the impact of $H^z_{\rm stray}$ on $t_{\rm w}$(AP→P). However, an increase in the switching voltage $V_{\rm MTJ}$ also results in more power consumption and a higher vulnerability to breakdown. In addition, when the pitch goes from 3×eCD (Fig. 5a) to 2×eCD (Fig. 5b), the inter-cell magnetic coupling factor Ψ increases from 1% to 2% and the change in $t_{\rm w}$(AP→P) is negligible. However, when the pitch goes down to 1.5×eCD (Fig. 5c), Ψ increases to 7% and the variation in $t_{\rm w}$(AP→P) between different NPs (i.e., $H^z_{\rm s\_inter}$) becomes very visible. For example, at a voltage of 0.72 V, $t_{\rm w}$(AP→P) under NP_8=0 is ∼4 ns slower than NP_8=255, as shown in Fig. 5c. This indicates that a larger write margin (e.g., a longer pulse) is required to avoid write failure in the worst case (i.e., NP_8=0). Similarly, Fig. 5d-5f show the simulation results of the other switching direction: P→AP, under the same Python simulation setup. It is clear that $H^z_{\rm stray}$ exerts an inverse influence on $t_{\rm w}$(P→AP), in comparison to $t_{\rm w}$(AP→P). When pitch=1.5×eCD (see Fig. 5f), NP_8=0 facilitates P→AP switching to the highest extent, whereas the same data pattern impedes AP→P switching the most (see Fig. 5c).

D. Impact on the Thermal Stability Factor

The intrinsic thermal stability factor Δ_0 (without any stray field at the FL) of the MTJ device is given by [18]: $\Delta_0 = \frac{H_{\rm k} M_{\rm s} V}{2 k_B T}$, where $k_{\rm B}$ is the Boltzmann constant and T is the absolute temperature. However, in the presence of stray fields, the thermal stability factor in AP state deviates from that in P state, i.e., $\Delta_{\rm AP} \neq \Delta_{\rm P}$. The Δ value in the presence of $H^z_{\rm stray}$ is given by [18]:

$$\Delta(H^z_{\rm stray}) = \Delta_0 (1 \pm \frac{H^z_{\rm stray}}{H_{\rm k}})^2, \tag{5}$$

where the sign in the parentheses is '+' for $\Delta_{\rm P}$ and '−' for $\Delta_{\rm AP}$ for the devices considered in this paper. $H^z_{\rm stray}$ can be calculated with our proposed magnetic coupling model, while $H_{\rm k}$ and Δ_0 are extracted from measurement data, as explained previously.

Fig. 6a shows the thermal stability factor Δ at varying temperature for eCD=35 nm and pitch=2×eCD, corresponding to $\Psi = 2\%$. It can be seen that the intra-cell stray field $H^z_{\rm s\_intra}$ introduces a static shift in $\Delta_{\rm AP}$ and $\Delta_{\rm P}$; $\Delta_{\rm AP}$ is ∼30% smaller than $\Delta_{\rm P}$ comparing the dash-dotted line to the dotted one. The solid lines represent the thermal stability factors considering both intra-cell and inter-cell magnetic coupling. It can be seen that the MTJ device has the smallest Δ (highest vulnerability to a retention fault) when the victim cell is in P state and all

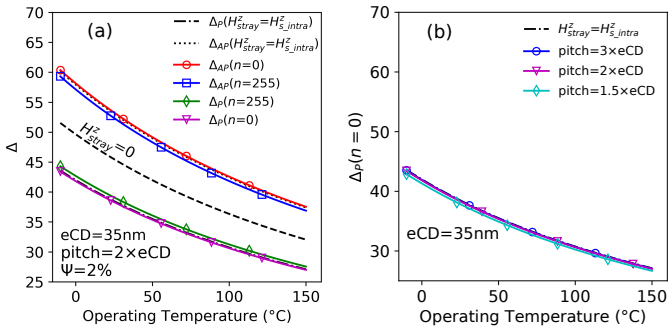


Fig. 6. Impact of magnetic coupling on Δ with eCD=35 nm at: (a) pitch= 2×eCD and (b) worst-case Δ for pitch=3×eCD, 2×eCD, and 1.5×eCD.

neighboring cells are also in P state (i.e., NP_8=0). Note that we think it is more important to identify the worst-case Δ instead of its maximum variation, under the influence of array pitch and data pattern in the neighborhood. As long as $\Delta_P(NP_8=0)$ (worst case here) meets the minimum requirement of retention time for a specific application, the other cases should also be acceptable. Fig. 6b compares the curve of $\Delta_P(NP_8=0)$ vs. temperature at pitch=3×eCD, 2×eCD, and 1.5×eCD. One can observe that $\Delta_P(NP_8=0)$ shows a marginal degradation when the array pitch goes down to 1.5×eCD, in comparison to pitch=2×eCD.

V. Implementation of MFA-MTJ Model

Robust and fast STT-MRAM design requires an accurate MTJ model for efficient circuit simulations. After verifying the proposed physics-based model of internal stray fields and its impact on MTJ performance in Python, we integrated this model into our Verilog-A pMTJ model; we name the resultant *magnetic-field-aware* pMTJ model as MFA-MTJ model. In this section, we first overview the block diagram of the MFA-MTJ model. Thereafter, we delve into each internal functional module and elaborate its functions and modeling principles.

A. Overview of MFA-MTJ Model

Fig. 7 illustrates the block diagram of our MFA-MTJ model. This model has two terminals and meets Ohm's law: i.e., $V(\mathrm{T1,T2})=I_{\mathrm{MTJ}}\cdot R_{\mathrm{MTJ}}$. The MTJ resistance R_{MTJ} depends on the magnetic state AP or P, the bias voltage $V(\mathrm{T1,T2})$, and the ambient temperature T; R_{MTJ} can also be switched between R_{P} and R_{AP}, depending on the current I_{MTJ} and its duration. In essence, the compact MTJ model describes the complex relationships between these three electrical variables. It abstracts an MTJ device from physical level to electrical level via compact behavioral modeling, described in an analog circuit description language: Verilog-A. In other words, the inputs of the MFA-MTJ model are physical and technology parameters (e.g., eCD and RA) and the outputs are MTJ's electrical parameters (e.g., R_{P} and I_{c}); the mapping relationships from the inputs to the outputs are analytically described by physical equations such as Equation (2).

The internal implementation of the MFA-MTJ model consists of different functional modules, as shown in Fig. 7. We divide them into three groups. First, the R_{P}, TMR, and R_{AP} modules are all concerned with the modeling of MTJ resistance. Second, the Δ, I_{c}, stochastic switching, and state machine modules are related to the modeling of MTJ switching behavior. Third, MTJ devices are never fabricated perfectly in practice. The MTJ resistance and switching behavior are significantly influenced by several factors such as magnetic fields, process variations, and manufacturing defects. These factors have a large impact on MTJ performance, thus requiring special attention. Next, we elaborate these three groups of functional modules in detail.

B. Modeling of MTJ Resistance

1) R_{P} module: The physical model of MTJ's tunneling magneto-resistance originates from [34], where it indicates that the resistance is mainly determined by the TB thickness and the interfacial effects between TB and adjacent CoFeB layers. The resistance in P state R_{P} decreases slightly with bias voltage V and it can be approximately considered independent on temperature [35]. We adopted the following two equations to model R_{P} at varying bias voltage and fitted the modeling results to our measurement data in [14]:

$$R_{\mathrm{P}}(V)=\frac{R_0}{1+s\cdot|V|}, \tag{6}$$

$$R_0=\frac{t_{\mathrm{ox}}}{F\cdot\sqrt{\bar{\varphi}}\cdot A}\exp(\mathrm{coef}\cdot t_{\mathrm{TB}}\cdot\sqrt{\bar{\varphi}}). \tag{7}$$

t_{TB} is the TB thickness, $\bar{\varphi}$ the potential barrier height of MgO, $A=\frac{1}{4}\cdot\mathrm{eCD}^2$ the horizontal cross-section of the MTJ device. F, coef and s are fitting coefficients depending on the RA product as well as the material composition of the MTJ layers.

2) TMR module: TMR ratio plays a critical role in determining the difficulty of distinguishing R_{P} and R_{AP} in read operations. Thus, a high TMR ratio, preferably above 180%, is expected in practice for commercially feasible STT-MRAM products. A recent study [36] reported that TMR=249% was achieved, which represents a key step towards the commercialization of STT-MRAM. Experimental results have showed that TMR ratio decreases with both temperature T and bias voltage V [37]. We model the dependence of TMR ratio on V and T as follows [14,35].

$$TMR(T)=\frac{TMR_0+1}{1+2Q\cdot\beta_{\mathrm{AP}}\cdot\ln(\frac{k_{\mathrm{B}}T}{E_{\mathrm{c}}})}-1, \tag{8}$$

$$TMR(T,V)=TMR(T)\cdot(1+\frac{V^2}{V_{\mathrm{h}}^2}+b\cdot V^{\frac{4}{3}})^{-1}. \tag{9}$$

In the above equations, TMR_0 is the TMR ratio at T=0 K and V=0 V. Q describes the probability of a magnon involved in the tunneling process. $\beta_{\mathrm{AP}}=Sk_{\mathrm{B}}T/E_{\mathrm{m}}$, where S is the spin parameter, k_{B} is the Boltzmann constant, and E_{m} is related to the Curie temperature T_{c} of the ferromagnetic materials: $E_{\mathrm{m}}=3k_{\mathrm{B}}T_{\mathrm{c}}/S+1$. E_{c} is the magnon cutoff energy. V_{h} and b are both fitting parameters.

3) R_{AP} module: Based on Equations (6-9), R_{AP} at certain T and V can be derived accordingly:

$$R_{\mathrm{AP}}(T,V)=R_{\mathrm{P}}(V)\cdot(1+TMR(T,V)). \tag{10}$$

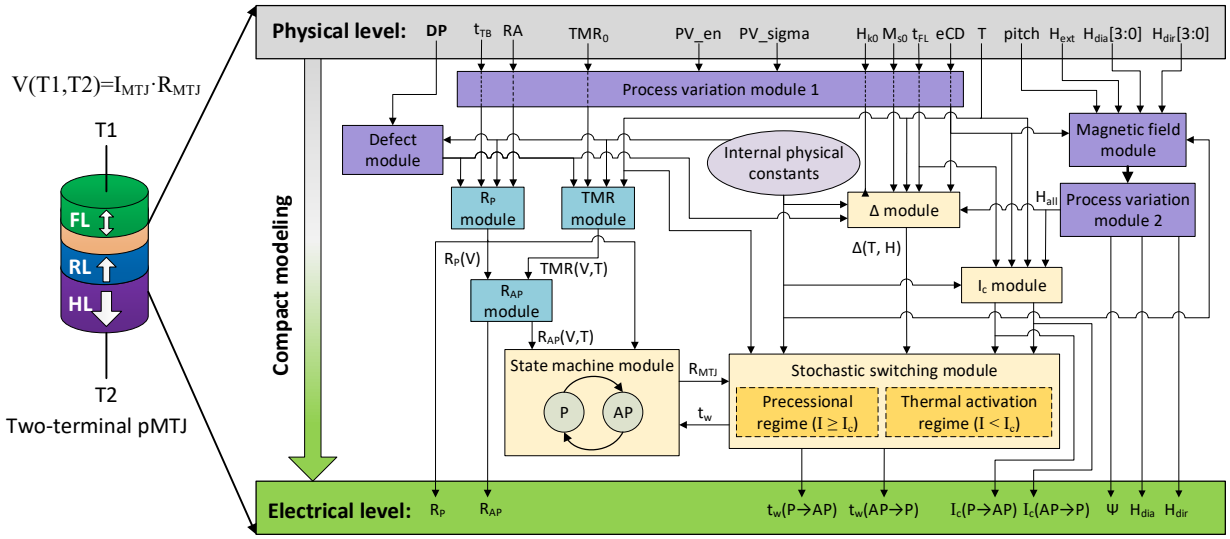


Fig. 7. Block diagram of the proposed MFA-MTJ model for simulations of hybrid MTJ/CMOS circuits.

C. Modeling of MTJ Switching Behavior

1) Δ module: The thermal stability factor Δ is a figure of merit for MTJs. Δ directly determines the retention time of data stored in an MTJ and it also has an impact on the switching behavior between AP and P states. Under the macrospin assumption (i.e., the magnetization in the FL switches uniformly as a whole), Δ can be expressed as [18,35]:

$$\Delta = \frac{E_{\mathrm{B}}}{k_{\mathrm{B}}T} = \frac{\mu_0 \cdot t_{\mathrm{FL}} \cdot M_{\mathrm{s}}(T) \cdot A \cdot H_{\mathrm{k}}(T)}{2k_{\mathrm{B}}T}, \tag{11}$$

$$M_{\mathrm{s}}(T) = M_{\mathrm{s0}} \cdot (1 - \frac{T}{T^*})^{\frac{3}{2}}, \tag{12}$$

$$H_{\mathrm{k}}(T) = f_1 \cdot T + f_2. \tag{13}$$

In Equation (11), μ_0 is the vacuum permeability and the other physical parameters have been introduced previously. Note that M_{s} and H_{k} are both dependent on T, as suggested by the experimental and modeling results in [38]. From the same paper, we extracted Equations (12-13) for modeling the temperature dependence of M_{s} and H_{k} in our MFA-MTJ model. M_{s0} is the saturation magnetization of the FL at 0 K; T^*, f_1, and f_2 are all fitting parameters.

2) I_{c} module: The magnetization dynamics in the STT switching process is typically described by the Landau-Lifshitz-Gilbert (LLG) equation with the addition of STT-related terms, under the assumption of macrospin approximation [14,18]. Solving the LLG equation results in Equation (2) for the critical switching current I_{c}.

3) Stochastic switching module: The switching behavior between AP and P states is a complex process, which is intrinsically stochastic and dependent on the applied pulse width t_{p}. Depending on the mechanism which dominates the switching behavior, the entire switching spectrum can be divided into two regimes: 1) *precessional regime* and 2) *thermal activation regime*. In the precessional regime where $t_{\mathrm{p}} <\sim 40$ ns, the STT effect is the main driving force which flips the magnetization of FL. In this regime, the average switching time t_{w} can be estimated using Sun's model, namely Equations (3-4). The actual switching time varies from one pulse to another (i.e., switching stochasticity). The root cause can be attributed to the variation of incubation time after the pulse onset, due to thermal fluctuation. We model the switching stochasticity by assigning a normal distribution to t_{w}, which has a fair agreement with measurement data [33,35]. In the thermal activation regime where the pulse width increases above 40 ns, observed in our devices, a small current less than I_{c} is able to flip the magnetization due to the increased thermal fluctuation. The thermal fluctuation plays a main role in determining the switching behavior. In this regime, the Neel-Brown model can be used to describe the average switching time t_{w} [14]:

$$t_{\mathrm{w}} = \tau_0 \exp(\Delta(1 - \frac{I_{\mathrm{MTJ}}}{I_{\mathrm{c}}})), \tag{14}$$

where τ_0 is the attempt period ($\sim$1 ns). The actual switching time in this regime is modeled as an exponential distribution with its mean value at the calculated t_{w} in Equation (14) [13,39]. As a result, the switching probability $Pr(t_{\mathrm{p}})$ under a long pulse with current I_{MTJ} and width t_{p} is [40]:

$$Pr(t_{\mathrm{p}}) = 1 - \exp(-\frac{t_{\mathrm{p}}}{t_{\mathrm{w}}}). \tag{15}$$

Equations (14-15) are commonly used to estimate the read disturb rate, as the read current shares the same path and direction with the write current in w0 operations [19].

4) State machine module: The state machine controls the transition between P and AP states at run time. It outputs the MTJ resistance $R_{\mathrm{MTJ}} \in \{R_{\mathrm{P}}, R_{\mathrm{AP}}\}$ to the stochastic switching module for calculating I_{MTJ} under the voltage bias V(T1,T2) applied across the MTJ device. Meanwhile, the stochastic switching module sends t_{w} to the state machine to activate a transition between P and AP states when meeting all switching conditions.

D. Modeling of Other Key Characteristics

1) Magnetic field module: Analog circuit simulators such as Cadence Spectre and HSPICE are intended for simulations

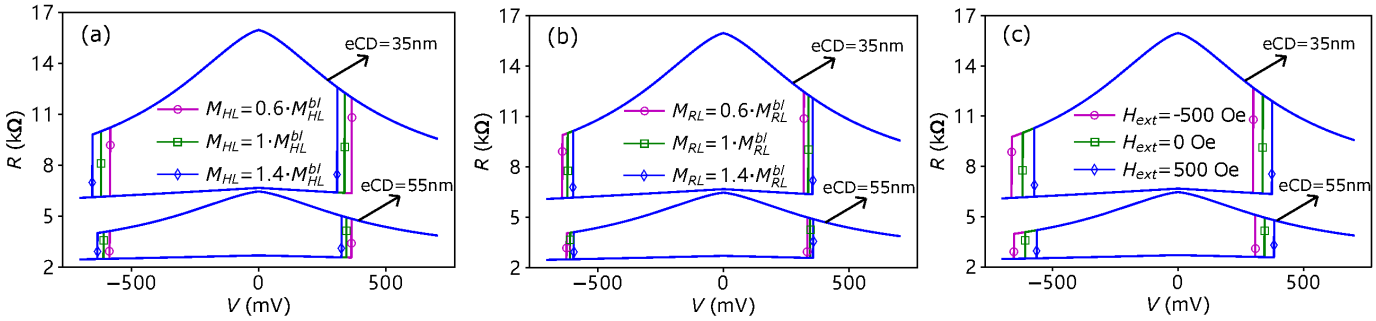


Fig. 8. DC simulation results of R-V loops for MTJs with eCD=35 nm and 55 nm, with respect to different configurations of magnetic fields at the FL.

of electrical circuits. With the emergence and fast development of spintronics, there is a need of simulating hybrid MTJ/CMOS circuits such as STT-MRAM, magnetic flip-flop, and magnetic full adder. Unlike MOSFETs where only electrical properties matter, MTJ devices own both electrical and magnetic properties. These two types of properties are typically interacted exploiting the spin and charge properties of electron, and they are very sensitive to magnetic fields, as mentioned in the previous sections. Therefore, it is paramount to consider and evaluate the effects of magnetic fields when simulating and designing MTJ-based circuits. As a solution, we implemented our magnetic field module presented in the previous sections using Verilog-A and then integrated it into our MFA-MTJ model. The magnetic field module takes into account three sources of magnetic fields:

$$H_{\rm all} = H^z_{\rm s\_intra} + H^z_{\rm s\_inter} + H^z_{\rm ext}. \quad (16)$$

In the above equation, $H^z_{\rm s\_intra}$, $H^z_{\rm s\_inter}$, and $H^z_{\rm ext}$ are the out-of-plane components of intra-cell stray field, inter-cell stray field, and external stray field, respectively. $H^z_{\rm s\_intra}$ is calculated internally in the MFA-MTJ model, depending on eCD and pitch. $H^z_{\rm s\_inter}$ consists of $H_{\rm dir}$[3:0] and $H_{\rm dia}$[3:0], standing for the inter-cell stray fields from four direct and four diagonal neighbors. Note that $H_{\rm dir}$[3:0], $H_{\rm dia}$[3:0], and $H^z_{\rm ext}$ are all defined as electrical input ports, which connect to other MTJ devices or circuit elements. Together, these three magnetic fields result in a net overall field $H_{\rm all}$ acting on a specific MTJ device in an STT-MRAM array. The magnetic field module is connected to a process variation module which can introduce a Gaussian distribution to the calculated stray fields. $H_{\rm all}$ is then fed into the Δ, $I_{\rm c}$, and stochastic switching modules, as described by Equations (2-5). The process variation module for the magnetic field module also outputs Ψ, $H_{\rm dir}$, and $H_{\rm dia}$ at run time (depending eCD, pitch, and MTJ state) via three electrical ports of the MFA-MTJ model in the form of voltage.

2) Defect module: MTJ devices are typically fabricated and integrated between two adjacent metal layers (e.g., M4 and M5) in the BEOL of CMOS process; this process is unique to STT-MRAM and is susceptible to manufacturing defects [19]. We have successfully designed and integrated models for MTJ-internal defects such as pinhole [6], synthetic anti-ferromagnetic layer flip [33], and intermediate state [41] into our MFA-MTJ model. The effects of these defects are first incorporated into the physical parameters of MTJ and thereafter into the electrical parameters; these defect models were also corroborated and calibrated by silicon data of defective MTJ devices fabricated at IMEC.

3) Process variation module: Process variation (PV) is inevitable when fabricating integrated circuits. The impact of PV on the performance and reliability of integrated circuits becomes increasingly pronounced as the CMOS technology node scales down. To design robust STT-MRAM circuits, PV related to MTJ devices should also be taken into account. The PV module is implemented by assigning normal distributions to key MTJ dimension parameters such as eCD, $t_{\rm FL}$, and $t_{\rm TB}$, as well as key physical parameters such as RA and TMR_0. "PV_en" and "PV_sigma" are two input parameters of the compact MTJ model, controlling the internal PV module.

VI. MTJ Electrical Characteristics Under Various Magnetic Configurations

After obtaining the MFA-MTJ model, we verified it with Cadence Spectre, a commercial analog circuit simulator. In this section, we first present DC simulation results of the model. Thereafter, we present transient simulation results in the form of write error rate (WER) statistics.

A. DC Simulations: R-V Loops

Measuring R-V loops is a common practice to characterize the voltage dependence of MTJ resistance at P and AP states. We have calibrated the DC simulation results of R-V loops of our compact model with silicon data, as can be found in [14]. Fig. 8a shows the DC simulation results of R-V loops for MTJs with eCD=35 nm and 55 nm. For each size, we simulated three configurations of HL by modifying its saturation magnetization $M_{\rm HL}$; the change of $M_{\rm HL}$ resulted in different stray fields at the FL. $M^{\rm bl}_{\rm HL}$ means the baseline $M_{\rm HL}$ from experimental results. It can be seen in Fig. 8a that both $R_{\rm P}$ and $R_{\rm AP}$ increase significantly as eCD decreases. A change in $M_{\rm HL}$ has no impact on MTJ resistance, but it affects the switching voltage $V_{\rm c}$. Reducing $M_{\rm HL}$ by 40% of $M^{\rm bl}_{\rm HL}$ leads to an increase in $V_{\rm c}$ for P→AP switching and a decrease in $V_{\rm c}$ for AP→P switching. In contrast, increasing $M_{\rm HL}$ by 40% of $M^{\rm bl}_{\rm HL}$ results in an opposite effect on $V_{\rm c}$, as shown in the figure. Similarly, we also simulated three values of saturation magnetization of RL ($M_{\rm RL}$) and three values of the external magnetic field at FL ($H_{\rm ext}$). The simulation results are shown in Fig. 8b and Fig. 8c, respectively.

In addition to changing $M_{\rm HL}$ and $M_{\rm RL}$, another common method in the community to tune the stray field at the FL is

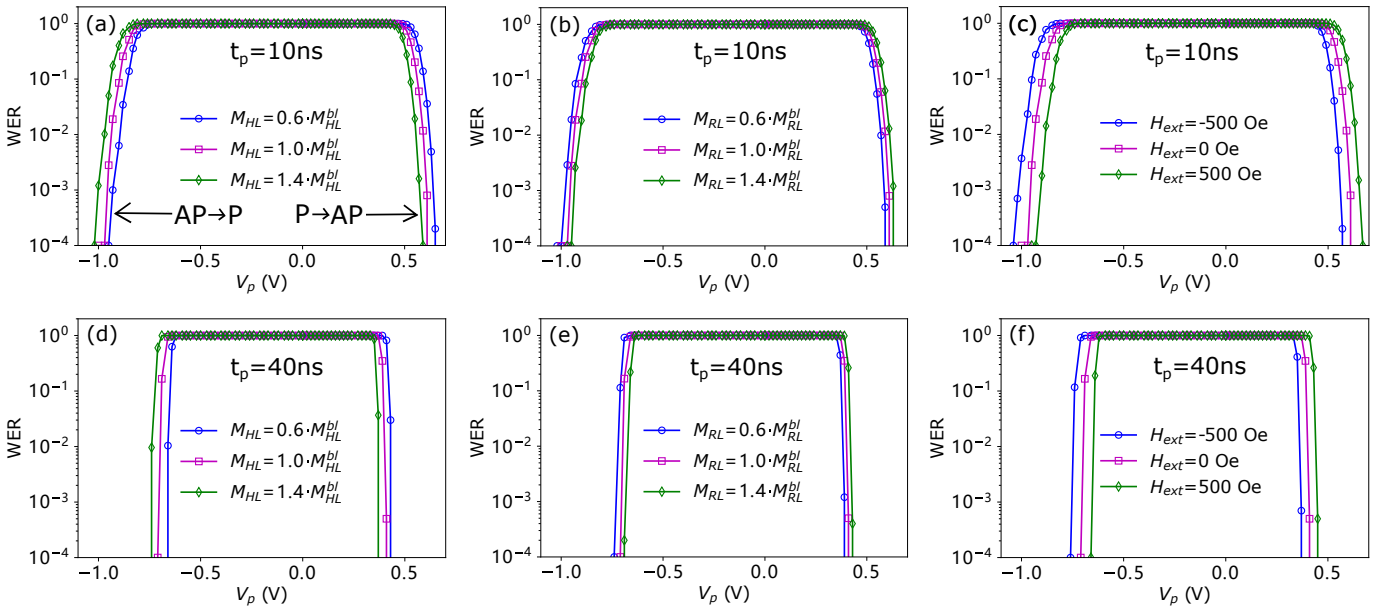


Fig. 9. Transient simulation results of write error rate (WER) vs. bias voltage $V_{\rm p}$ for MTJs with eCD=35 nm at pulse width $t_{\rm p}$=10 ns and 40 ns.

to change the cycle numbers of CoPt multilayers in the RL and HL [24,42]. This represents the change of layer thickness of the RL and HL. In our stray field model [17], the magnetic moment of a ferromagnet is expressed as $\boldsymbol{m} = \boldsymbol{M_s} \cdot A \cdot t$, where A is the cross-sectional area of the ferromagnet and t is its thickness. Considering the bound current I_b, $\boldsymbol{m}$ can also be written as $I_b \cdot A \cdot \hat{\boldsymbol{n}}$, where $\hat{\boldsymbol{n}}$ is the unit vector along the direction of M_s. Therefore, one can easily derive $I_b = M_s \cdot t$. This suggests that changing the layer thickness t has a similar effect as M_s on the bound current and thus on the stray field it generates in the near space.

B. Transient Simulations: WER Statistics

The MTJ switching behavior is intrinsically stochastic and is significantly dependent on the applied pulse width $t_{\rm p}$ and amplitude $V_{\rm p}$. This characteristic directly affects STT-MRAM circuit designs such as cell selector and write driver. Therefore, it is very important to experimentally characterize WER vs. $V_{\rm p}$ at varying $t_{\rm p}$, meanwhile providing a capability of simulating this characteristic to facilitate and verify circuit designs. Fig. 9a-9c present the simulation results of WER vs. $V_{\rm p}$ at $t_{\rm p}$=10 ns with respect to different magnetic configurations, using our MFA-MTJ model with eCD=35 nm. It is clear that increasing the $V_{\rm p}$ magnitude is very effective in reducing WER for both switching directions; note that here a negative $V_{\rm p}$ results in AP→P switching whereas a positive $V_{\rm p}$ results in P→AP switching. For the original MTJ design where $M_{\rm HL}$=$M_{\rm HL}^{\rm bl}$, $M_{\rm RL}$=$M_{\rm RL}^{\rm bl}$, and $H_{\rm ext}$=0 Oe, the WER curve is asymmetric; $|V_{\rm p}({\rm AP}\rightarrow{\rm P})|$ is much larger than $|V_{\rm p}({\rm P}\rightarrow{\rm AP})|$ for a given WER value. By reducing $M_{\rm HL}^{\rm bl}$ by 40%, the WER curve in Fig. 9a shifts to the right side, indicating approximately one order of magnitude decrease in WER at a fixed $V_{\rm p}$ for AP→P switching and an opposite effect on P→AP switching. Fig. 9b-9c depict how the WER curve is affected when modifying $M_{\rm RL}$ and $H_{\rm ext}$, respectively. Fig. 9d-9f present similar simulation results, but at $t_{\rm p}$=40 ns. It is worth noting that the slope of WER curve when $t_{\rm p}$=40 ns is much larger than that when $t_{\rm p}$=10 ns. This is because the switching variation is smaller at longer pulses, which is consistent with the measurement data of our devices [33] and others' devices [43,44].

In summary, the above DC and transient simulation results suggest that our MFA-MTJ model is qualified for emulating MTJ devices for SPICE-based circuit simulations. By manipulating stray fields at the FL, which is achieved by adjusting the SAF design of the MTJ device, we can adjust the WER curve to the position that we desire when designing STT-MRAM cell and peripheral circuits. Hence, our MFA-MTJ model can be used for device/circuit co-design for STT-MRAM.

VII. Robustness Analysis of STT-MRAM Designs

Apart from a single MTJ device, we also simulated a 3×3 STT-MRAM array with peripheral circuits such as write driver and sense amplifier, as shown in Fig. 10a. Each STT-MRAM cell consists of an MTJ device and an NMOS as a selector; Fig. 10b shows the memory cell and three basic operations [19]. The details of simulation circuits can be found in [6]; all transistors in the netlist were built with the 45 nm predictive technology model (PTM). In this section, we first present transient simulation results of the STT-MRAM full circuit under different eCDs and pitches. Thereafter, we explore the design space under PVT variations and different magnetic configurations.

A. Transient Simulations Under Different eCDs and Pitches

To demonstrate the capability of our MFA-MTJ model for electrical/magnetic co-simulation under SPICE-based circuit

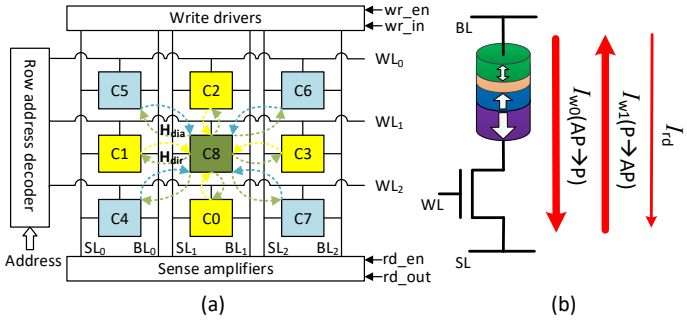


Fig. 10. (a) 3×3 STT-MRAM array with peripheral circuits, and (b) 1T-1MTJ memory cell and the associated cell operations.

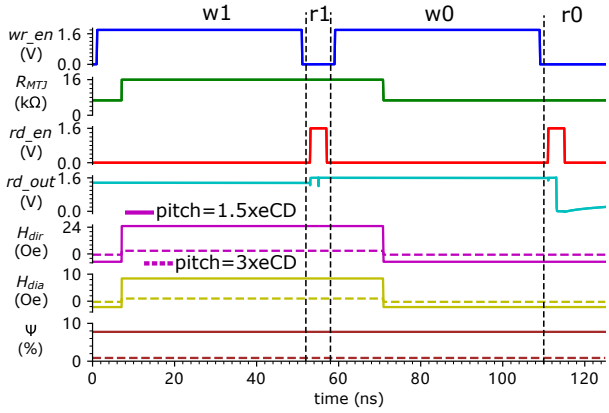
simulation environment, we simulated the STT-MRAM full circuit in Fig. 10 with two eCDs (35 nm and 55 nm) and two pitches (3×eCD and 1.5×eCD). During the simulations, we set the data background in C0-C7 at 255 (i.e., NP_8=255) and applied the operation sequence: 0w1r1w0r0 to the central cell C8 as a case-study.

Fig. 11a shows the simulation waveforms of seven key signals related to C8 when eCD=35 nm. It can be seen that C8 is initialized to 0; it outputs $H_{\rm dir}$=−7.06 Oe to its direct neighbors C0-C3 and $H_{\rm dia}$=−2.17 Oe to its diagonal neighbors C4-C7 at pitch=1.5×eCD. Ψ is 7.8% at this pitch value. In contrast, $H_{\rm dir}$, $H_{\rm dia}$, and Ψ are all close to 0 at pitch=3×eCD. During the w1 operation, the state of C8 transitions to 1 (see $R_{\rm MTJ}$); $H_{\rm dir}$ and $H_{\rm dia}$ are changed to 24.27 Oe and 8.16 Oe, respectively, when at pitch=1.5×eCD. Following the w1 operation, a r1 is applied, which outputs 1 on the signal rd_out. Similar observations can be seen for the following w0 and r0 operations.

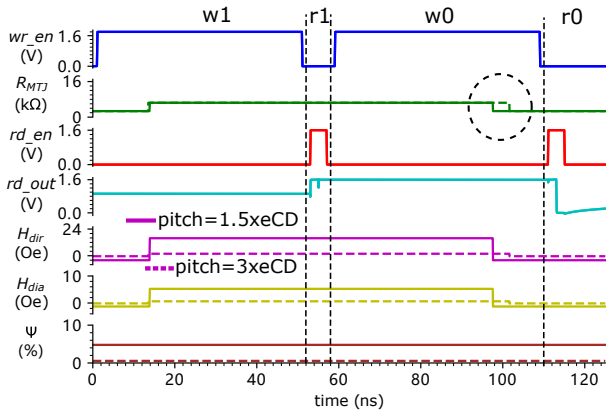
Fig. 11b shows the simulation waveforms when eCD= 55 nm. The following three differences from Fig.11a are worth noting: 1) the switching time in both w1 and w0 operations become longer, as larger MTJ devices require larger switching current; 2) $H_{\rm dir}$, $H_{\rm dia}$, and Ψ are different due to the change of eCD; 3) when the pitch changes from 3×eCD to 1.5×eCD, the switching time during the w1 operation larger while it becomes smaller in the w0 operation (see the circled part), due to the inter-cell magnetic coupling effect.

B. Design Space With Various Variation Sources

It is well known that STT-MRAM designs are significantly influenced by the following sources of variations: 1) process variation (device-to-device variation), 2) supply voltage variation, 3) operating temperature variation, 4) MTJ switching stochasticity (cycle-to-cycle variation), and 5) magnetic field variation. We explored the design space considering the aforementioned five variation sources in our circuit simulations. The process variation was modeled by assigning normal distributions to key parameters of both transistors and MTJs. For transistors, it was lumped into the variation in the threshold voltage $V_{\rm th}$ with 10% away from its nominal value at 3σ corners. For MTJs, we assigned the same normal distribution to key input parameters shown in Fig. 7. In terms of supply voltage $V_{\rm DD}$ variation, we assigned a uniform distribution to $V_{\rm DD}$ with its minimum at 1.5 V and maximum at 1.7 V. The



(a) eCD=35 nm.



(b) eCD=55 nm.

Fig. 11. Waveforms of key signals during the transient simulation of operation sequence: 0w1r1w0r0, under four different combinations of eCD and pitch.

typical industrial standard of operating temperature $T \in$ [-40, 125]°C [1]. The MTJ switching stochasticity was implemented in our MFA-MTJ model and it can be enabled or disabled as required. The magnetic field variation includes $\boldsymbol{H}_{\rm s\_intra}$, $\boldsymbol{H}_{\rm s\_inter}$, and $\boldsymbol{H}_{\rm ext}$ as mentioned in the previous sections.

We performed 10k-cycle Monte Carlo simulations of 0w1 and 1w0 operations while sweeping two variables: pulse width $t_{\rm p}$ and voltage on the WL $V_{\rm WL}$. This is based on the fact that boosting $V_{\rm WL}$ is required to deliver sufficient switching current going through MTJ devices due to the source degeneration issue [19]; this has been a common practice in industry. Fig. 12a shows a contour plot of WER of 1w0 operation with respect to $t_{\rm p}$ and $V_{\rm WL}$, when eCD=35 nm, pitch=1.5×eCD, NP_8=255, and $H_{\rm ext}$=0 Oe at room temperature T=27 °C. It can be seen that WER(1w0) gradually decreases from the lower-left corner to the upper-right corner. When the 1w0 operations were all successful among the 10k Monte Carlo simulations, we marked the WER value at 10^{-6} (i.e., the deep blue area). We define the *area of design space* $A_{\rm ds}$ as the normalized area where WER=10^{-6} with respect to the entire area of the contour plot. In Fig. 12a, $A_{\rm ds}$=0.254. This is 12.4% larger than the baseline $A_{\rm ds}$ value in Fig. 12c where pitch=3×eCD and NP_8 has no influence. Fig. 12b shows the simulation results when pitch=1.5×eCD, NP_8=0, and $H_{\rm ext}$=0 Oe; $A_{\rm ds}$ decreases by 3.5% in comparison to the baseline setup, due to the inter-cell magnetic coupling effect. In addition, we also studied the

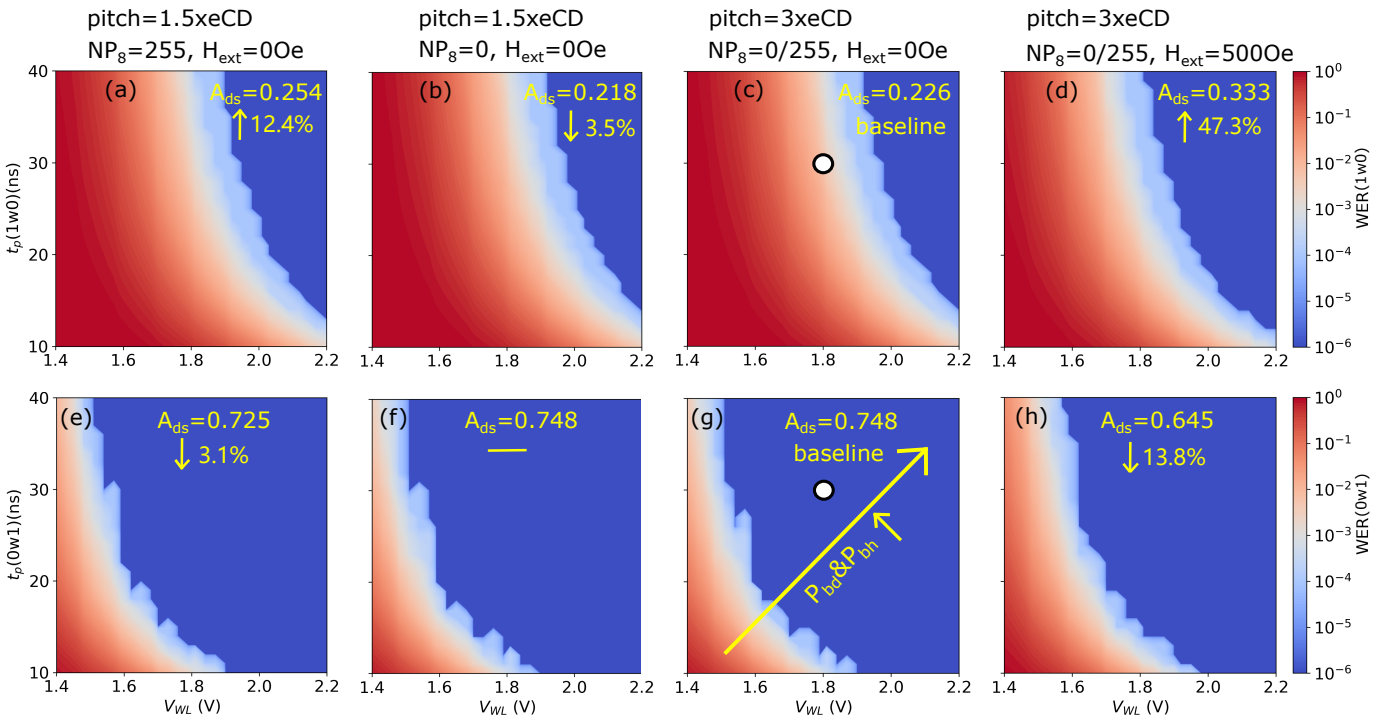


Fig. 12. WER at different combinations of t_{p} and V_{WL} for 1w0 and 0w1 operations under different simulation set-ups about pitch, NP_8, and H_{ext}.

impact of H_{ext} on A_{ds}; the result is shown in Fig. 12d. When the STT-MRAM design is subject to an external magnetic field of 500 Oe, A_{ds}(1w0) increases by 47.3%.

Similarly, the simulation results for 0w1 operations are shown in Fig. 12e-12h. It is clear that A_{ds}(0w1) is much larger than A_{ds}(1w0) under the same simulation conditions, which suggests a critical design challenge facing STT-MRAM: write asymmetry. For example, when fixing t_{p}=30 ns and V_{WL}=1.8 V, the resultant WER(0w1) has already reached the center of the deep blue area in Fig. 12g (see the white circle). In contrast, WER(0w1) has not entered into the deep blue area (see the white circle in Fig. 12c). Worse still, the deeper the white circle enters into the deep blue area, the probability of breakdown (P_{bd}) or back-hopping (P_{bh}) becomes larger, as illustrated with the yellow arrow in Fig. 12g. Moreover, the effects of NP_8 and H_{ext} are always opposite for 0w1 operations, compared to 1w0 operations. This implies that the write asymmetry can be adjusted by manipulating magnetic fields. For example, applying H_{ext}=500 Oe increases A_{ds}(1w0) by 47.3% (see Fig. 12d), whereas it reduces A_{ds}(0w1) by 13.8% (see Fig. 12h).

Fig. 13a shows the dependence of A_{ds} on H_{ext}. It can be observed that A_{ds}(0w1) significantly decreases with H_{ext} whereas A_{ds}(1w0) shows an opposite trend. When H_{ext}=∼1.1 kOe, a symmetric design space for 0w1 and 1w0 operations is achieved. On one hand, this suggests that we can design the SAF layer to generate the desired stray field at the FL (same effect as H_{ext}), meeting the requirements of circuit-level designs. On the other hand, we need to pay attention to external magnetic disturbance, requiring package-level magnetic shield or other measures to enhance magnetic immunity [5].

Fig. 13a shows the dependence of A_{ds} on the operating temperature T. It can be observed that A_{ds} for both 1w0 and

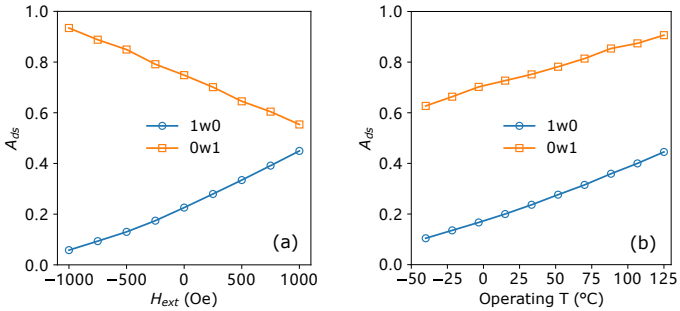


Fig. 13. STT-MRAM write design space A_{ds} vs. (a) external magnetic field H_{ext} and (b) operating temperature T.

1w0 significantly increases with T. Although high temperature is in favor of STT-MRAM write operations, it also brings side effects: 1) retention time reduction, 2) degraded read reliability due to TMR drop, and 3) increased vulnerability to breakdown and back-hopping. For an industrial standard $T\in[-40, 125]$°C, A_{ds} variation can reach up to 0.25. This implies the importance of having a field-programmable/self-adaptive write scheme for STT-MRAM, in order to select the optimal operating point for various working environments.

VIII. Discussion and Future Work

In this section, we briefly compare our proposed MTJ model with other models in the literature. Thereafter, we discuss the magnetic fields from current-carrying metal lines, how to use our model, and its limitations.

A. Comparison with Other MTJ Model

We compared the proposed MFA-MTJ model in this work with other MTJ models in the literature using eight metrics, as shown in Table I.

TABLE I
COMPARISON BETWEEN DIFFERENT MTJ MODELS.

Model Type	MTJ Model	Sim. Accuracy	Sim. Overhead	Circuit Sim. Compatibility	Flexibility	Scalability	Magnetic/Electrical Co-Simulation	Defect Injection &Fault Analysis	Silicon Data Validation
Micromagnetic model	OOMMF [8]	High	High	No	Low	No	No	No	Yes (First-hand)
	mumax^3 [45]	High	High	No	Low	No	No	No	No
Commercialized-tool based model	Synopsis Sentaurus Device [9]	Medium	Medium	Yes	Low	Low	No	No	No
Macro model	SPICE-inbuit circuit element model [10]	Medium	Medium	Yes	Medium	Medium	No	No	Yes (Second-hand)
Behavioral model	Verilog-A model [13]	Medium	Low	Yes	High	High	No	No	Yes (Second-hand)
	This work	Medium	Low	Yes	High	High	Yes	Yes	Yes (First-hand)

Micromagnetic MTJ models based on OOMMF and mumax^3 obviously provide high simulation accuracy with high simulation overhead; they are suitable for studying switching dynamics and interactions of physical phenomena for a single MTJ. Commercialized-tool-based MTJ models offer medium simulation accuracy and overhead, and they are compatible with circuit simulations. But they are flawed with low flexibility and scalability, which limit their use in simulating a large STT-MRAM array with different device configurations. Macro MTJ models have a good balance and provide medium performance at many aspects; but the inbuit circuit elements increase dramatically and simulation overheads are very high when simulating a large STT-MRAM array. Behavioral MTJ models are considered as new circuit elements and provide better flexibility and scalability than Macro models.

MFA-MTJ model owns the advantages of traditional behavioral models. In addition, it has the following new features:

- Magnetic/electrical co-simulation of MTJ/CMOS circuits. Since the performance of MTJ devices is very sensitive to magnetic fields, this feature is crucial for spintronic circuit design; This work is the first introducing this feature in the EDA community.
- Device defect injection and fault analysis. MTJ devices require unique manufacturing steps and are subject to new defects and failure mechanisms [19]. Thus, this new feature enables device-aware test [46] to analyze realistic fault models and to develop high-quality yet cost-efficient tests for STT-MRAMs.
- Comprehensive silicon data validation. We have validated our MTJ model including the magnetic field module in this work, resistance modules [14], switching modules [6], and defect modules [33], using first-hand silicon data collected at IMEC.

B. Magnetic Fields From Current-Carrying Metal Lines

As we emphasize many times in this paper, the performance of STT-MRAM is very sensitive to any sources of magnetic fields. Thus, we have taken into account internal stray fields and external disturbance fields and studied their impact on STT-MRAM performance in this work. For the future work on this topic, it is crucial to analyze, model, and evaluate the magnetic fields generated by current-carrying metal lines such as the BL, SL, and WL. The impact of the fields from these metal lines are strongly dependent on specific STT-MRAM cell designs (e.g., physical cell structure and cell layout). In [47], TSMC presents the vertical STT-MRAM cell structure with logic compatible metal layers; it shows that the BL is located at M5 and M6, right on top of MTJ devices which sit above M4. In contrast, WL and SL are located at different metal layers which are slightly farther from MTJ devices; this indicates that the magnetic fields from WL and SL lines probably have no or marginal impact on STT-MRAM devices. Similarly, Intel revealed their STT-MRAM cell layout in [48], which also suggests that BLs are very close to STT-MRAM cells; thus, the magnetic fields from BLs might need to be considered. In summary, magnetic fields from current-carrying metal lines and their impact on STT-MRAM performance can be very interesting to study in the future work; the design constraints in terms of magnetic coupling also need to be determined when design STT-MRAMs.

C. Model Usage and Limitations

The proposed MFA-MTJ model can be used for spintronic circuit design and validation, especially for STT-MRAMs. Although we demonstrated the usage of this model for circuit simulations and analysis of a single STT-MRAM device and 3×3 STT-MRAM full circuits in this article, we can also instantiate more cells to scale up to a large memory array. The simulation of a single cell takes $415\,\text{ms}$, and a 3×3 array takes $823\,\text{ms}$, a 16×16 array takes $1.7\,\text{s}$. Note that the simulation time varies with the simulation configurations such as the time step of transient simulation, switching stochasticity options, and defect injection. To facilitate circuit simulations and analyses, we have wrapped the circuit netlist with a high-level controller written in Python3; configuration parameters are passed from the end users to the Python controller which creates the desired netlist, controls the simulation process, and analyzes the measured data. Therefore, the simulation platform is quite user-friendly; the end users only need to learn what simulation parameters and what simulation analyses the Python controller provides. The simulation parameters are all independent and can be easily configured.

We also provide Python code to run the simulations in a Cluster to speed up the simulation process by exploiting task-level parallelism. We observed that Monte Carlo (MC) simulations are very time consuming. For example, a 10-cycle MC simulation of the 3×3 array takes $5.7\,\text{s}$, 100 cycles

take 55.6 s, 1k cycles take 537 s, 10k cycles take ∼23 mins. The simulation time becomes prohibitive if we would like to sweep several key parameters (e.g., t_{p} and V_{WL} in Fig. 12). Therefore, we provide another Python controller version which distributes parallel simulation tasks onto different compute nodes in a cluster. Our experiments show that running our Spectre circuit simulations (MC + parameter sweep) on the cluster in our department with eight compute nodes provides ∼100x speedup. Still, the excessive amount of computation resources and time is a big barrier for the study of design space considering different variation sources. To further speed up such circuit simulations, the worst-case corner method [35] can be a good alternative to the MC simulation method.

IX. Conclusion

In this article, we have proposed a magnetic-field-aware compact model of pMTJ, named as MFA-MTJ model. This model has been implemented in Verilog-A and calibrated with silicon data. It features high configurability and awareness of internal intra- and inter-cell stray fields and external disturbance fields. Based on the MFA-MTJ model, magnetic/electrical co-simulations of STT-MRAM designs have been demonstrated. This model also enables us to explore STT-MRAM design space under PVT variations and various configurations of magnetic fields.

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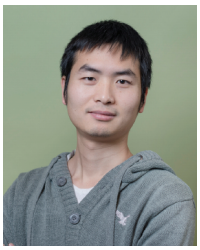

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