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## Device modeling of two-steps oxygen anneal-based submicron InGaZnO back-end-of-line field-effect transistor enabling short-channel effects suppression

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Amorphous oxide semiconductor (AOS) field-effect transistors (FETs) have been integrated with complementary metal-oxide-semiconductor (CMOS) circuitry in the back end of line (BEOL) CMOS process; they are promising devices creating new and various functionalities. Therefore, it is urgent to understand the physics determining their scalability and establish a physics-based model for a robust device design of AOS BEOL FETs. However, the advantage emphasized to date has been mainly an ultralow leakage current of these devices. A device modeling that comprehensively optimizes the threshold voltage ( $V_T$ ), the short-channel effect (SCE), the subthreshold swing (SS), and the field-effect mobility ( $\mu_{FE}$ ) of short-channel AOS FETs has been rarely reported. In this study, the device modeling of two-steps oxygen anneal-based submicron indium-gallium-zinc-oxide (IGZO) BEOL FET enabling short-channel effects suppression is proposed and experimentally demonstrated. Both the process parameters determining the SCE and the device physics related to the SCE are elucidated through our modeling and a technology computer-aided design (TCAD) simulation. In addition, the procedure of extracting the model parameters is concretely supplied. Noticeably, the proposed device model and simulation framework reproduce all of the measured current–voltage ( $I$ – $V$ ),  $V_T$  roll-off, and drain-induced barrier lowering (DIBL) characteristics according to the changes in the oxygen (O) partial pressure during the deposition of IGZO film, device structure, and channel length. Moreover, the results of an analysis based on the proposed model and the extracted parameters indicate that the SCE of submicron AOS FETs is effectively suppressed when the locally high oxygen-concentration region is used. Applying the two-step oxygen annealing to the double-gate (DG) FET can form this region, the beneficial effect of which is also proven through experimental results; the immunity to SCE is improved as the O-content controlled according to the partial O pressure during oxygen annealing increases. Furthermore, it is found that the essential factors in the device optimization are the subgap density of states (DOS), the oxygen content-dependent diffusion length of either the oxygen vacancy ( $V_O$ ) or O, and the separation between the top-gate edge and the source-drain contact hole. Our modeling and simulation results make it feasible to comprehensively optimize the device characteristic parameters, such as  $V_T$ , SCE, SS, and  $\mu_{FE}$ , of the submicron AOS BEOL FETs by independently controlling the lateral profile of the concentrations of  $V_O$  and O in two-step oxygen anneal process.

Amorphous oxide semiconductor (AOS) field-effect transistors (FETs) are successfully utilized in the back-plane panels of commercial display products, such as organic light-emitting diode displays and liquid-crystal

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displays<sup>1,2</sup>. Their advantages include higher mobility than amorphous Si, good large-area uniformity, and a low process temperature. Furthermore, AOS FETs are promising candidates for the back end of line (BEOL) FETs; their advantages include a low-temperature process, ultralow leakage current<sup>3</sup>, scalability, stability, endurance, low mask count, compatibility with complementary metal-oxide-semiconductor (CMOS) technology<sup>4</sup>, high thermal tolerance<sup>5</sup>, and threshold voltage ( $V_T$ ) controllability<sup>6</sup>.

Various new and promising applications have recently been demonstrated based on AOS BEOL FETs (e.g., 2T1C gain-cell memory<sup>4</sup>, monolithic three-dimensional (3D) 2T-dynamic random access memory<sup>7,8</sup>, W doping-based high-performance memory<sup>9</sup>, high-density and low-power memory using the incorporation into ferroelectric FET structures<sup>10</sup>, and the low standby power normally-off microcontroller<sup>11</sup>). In these applications, electrical properties of AOS FETs are mostly controlled via modulating the concentration of carrier donors, i.e., oxygen vacancy ( $V_O$ ) or hydrogen species, which are employed during the deposition of AOS active thin films or by combining the depositions of active film and gate insulator (GI) (especially in the case of the self-aligned top-gate coplanar structure<sup>12–18</sup>). However, these methods are not actually suitable for the BEOL process owing to their complexity and high cost. More BEOL-compatible AOS FET technology is required.

On the other hand, in these applications, whether the degree of integration density of AOS FETs is comparable to CMOSFETs determines the performance, power consumption, and cost. In particular, from the viewpoint of power consumption, AOS FET's advantage of very low leakage current may be diluted unless the integration density is significantly improved. Therefore, an AOS FET technology, which is compatible with the BEOL process and facilitates FET scaling-down, should be developed.

Meanwhile, as the AOS FETs are integrated with the CMOSFETs in the BEOL process and attract more attention as promising devices that create new and various functionalities, the understanding of the effect of process/structure condition on the short-channel effect (SCE) is urgent. Up to now, the device modeling and simulation have rarely demonstrated a comprehensive optimization of  $V_T$ , SCE, subthreshold swing (SS), and field-effect mobility ( $\mu_{FE}$ ) of short-channel AOS FETs, particularly in terms of the effect of process/structure condition on SCE.

This study demonstrates the device modeling of submicron amorphous InGaZnO (a-IGZO) FETs, based on experimentally extracted parameters. Both the subgap density of states (DOS), which is extracted through the photo-response of the current–voltage ( $I$ – $V$ ) characteristics, and the lateral profile of donor doping concentration are considered in the proposed model. In addition, the model parameters are incorporated into the technology computer-aided design (TCAD) simulation framework. Through the device simulation, the effects of oxygen (O) partial pressure and device structure on the device parameters are quantitatively investigated, and the feasibility of comprehensive optimization of the device performance parameters, such as  $V_T$ , SCE, SS, and  $\mu_{FE}$ , is proved in the bottom-gate (BG) and double-gate (DG) IGZO FETs fabricated with a two-step O annealing. The range of the channel length ( $L$ ) of used device is  $L = 0.245$ – $20.2$   $\mu\text{m}$ . In particular, which role the lateral profile of  $V_O$  and O concentrations can play in suppressing either the  $L$ -dependency of  $V_T$  or the drain-induced barrier lowering (DIBL) is explained and validated based on the proposed model-based simulation.

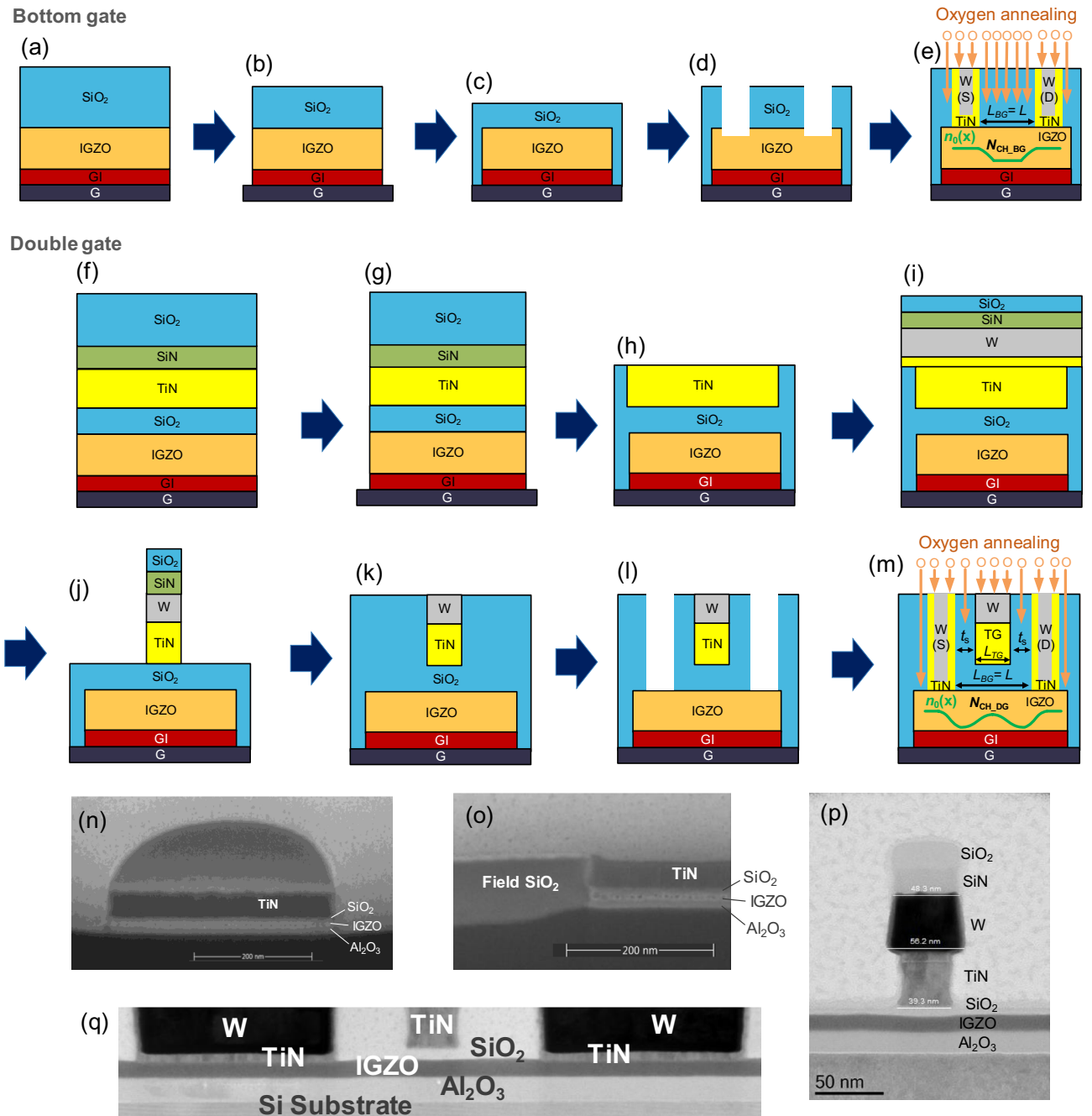
## Experimental results

**Two-step oxygen anneal-based fabrication of AOS FETs.** Figure 1a–e show the process of a bottom-gate (BG) IGZO FET fabrication<sup>19</sup>. First, 5-nm SiCN and 15-nm  $\text{Al}_2\text{O}_3$  films are deposited on a  $p^+$ -Si wafer, serving as back gate dielectrics (for BG). Then, a 12-nm-thick a-IGZO film is deposited by using physical vapor deposition (PVD). After that, a 180-nm  $\text{SiO}_2$  hard mask is deposited on top of the IGZO layer. Thus, the full stack is formed (Fig. 1a) and then patterned (Fig. 1b).  $\text{SiO}_2$  is then deposited and planarized (Fig. 1c). Next, the source/drain (S/D) contact trenches are patterned, landing selectively on IGZO (Fig. 1d). Finally, the metallization is implemented by depositing a 6-nm atomic layer deposition (ALD) TiN barrier and ALD/chemical vapor deposition (CVD) W metal contacts followed by a chemical mechanical polishing (CMP). The first oxygen anneal is then performed at 350 °C in an  $\text{O}_2$  atmosphere for 1 h in order to passivate defects generated during the process fabrication (Fig. 1e). The channel length of BG FET ( $L_{BG}$ ) is determined by the distance between the source and the drain contact holes. The IGZO active thickness ( $t_{act}$ ) and the equivalent oxide thickness of BG dielectric ( $t_{BGi}$ ) are 10 nm and 6.5 nm.

On the other hand, Fig. 1f–m show the process of the DG IGZO FET fabrication<sup>20</sup>. First, 15-nm  $\text{Al}_2\text{O}_3$  film is deposited on a  $p^+$ -Si wafer, serving as back gate dielectrics (for BG). After a 10-nm-thick a-IGZO film is then PVD deposited, the first oxygen anneal is performed. A top gate dielectric ( $\text{SiO}_2$ , 7 nm) and a TiN gate metal are then deposited (for top-gate (TG)) and followed by the deposition of SiCN/ $\text{SiO}_2$  hard mask (Fig. 1f). After the active patterning (Fig. 1g),  $\text{SiO}_2$  gap fill, planarization stopping on TiN, and etch-back are done (Fig. 1h). Then, the rest of the gate stack is deposited (TiN/W/SiCN/ $\text{SiO}_2$ ) (Fig. 1i), patterned (Fig. 1j),  $\text{SiO}_2$  gap fill, and planarized (Fig. 1k). Next, the S/D contact trenches are opened down to the IGZO layer (Fig. 1l). The contact metals are deposited (TiN-contact barrier/W-metal fill) and planarized. The first oxygen anneal is the same as the BG devices (Fig. 1m). Additional interconnections made of vias and metal lines are then implemented to access small devices. The TG channel length ( $L_{TG}$ ) in the DG structure (unlike the  $L_{BG}$  in the BG FET) is determined by the length of the TG electrode.

The scanning electron microscope (SEM) images after active patterning (Fig. 1g) and after planarization (Fig. 1h) of DG FETs are shown in Fig. 1n,o. In addition, the transmission electron microscopy (TEM) images after gate patterning (Fig. 1j) and after metallization (Fig. 1m) of DG FETs are given in Fig. 1p,q. As seen in Figs. S1–S3 (supplementary information), the wafer map for the critical dimension suggests that the entire fabrication process is reproducible, and a high-yield process is used in this work.

To adjust the donor doping concentration of the channel in IGZO ( $N_{CH}$ ), the second oxygen anneal is performed in both DG and BG FETs (Fig. 1e,m). According to the condition of the second oxygen anneal, two types

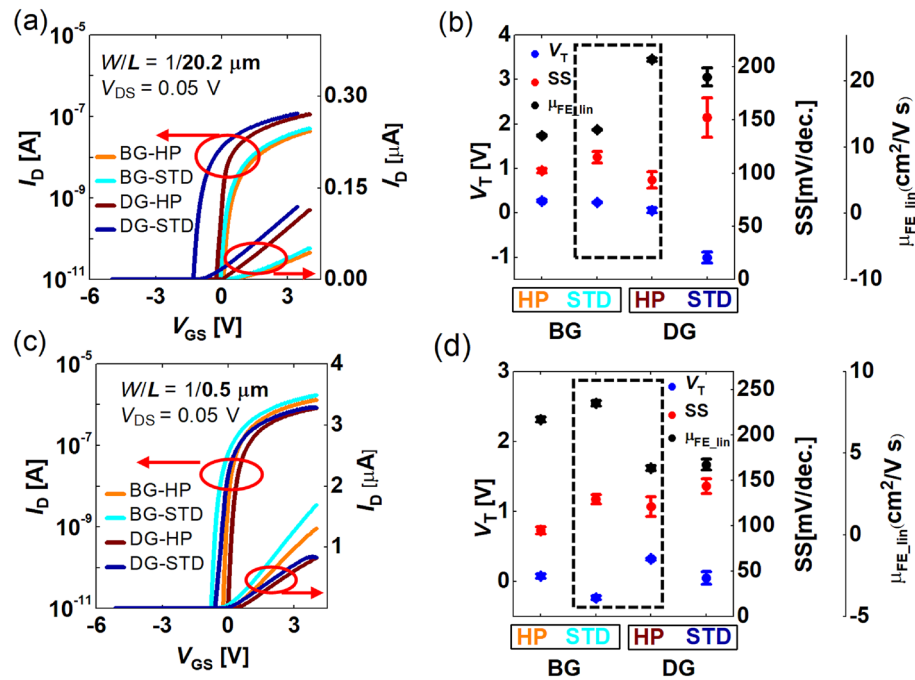


**Figure 1.** The integration process of the IGZO FET fabrication. Process sequence for (a–e) BG and (f–m) DG FET fabrication. SEM images of DG FET (n) after active patterning (g) and (o) after planarization (h). TEM images of DG FET (p) after gate patterning (j) and (q) after metallization (m).

of samples are prepared; (1) 350 °C in an O<sub>2</sub> atmosphere 1 atm for 2 h (called by the standard (STD) sample) and (2) 350 °C in an O<sub>2</sub> atmosphere 1 atm for 2 h + 350 °C in an O<sub>2</sub> atmosphere 20 atm for 2 h (called by the high pressure (HP) sample).

In the BG structure, the S/D metal acts as a diffusion barrier for oxygen during the oxygen annealing process (Fig. 1e). Meanwhile, in the DG structure, both TG metal and the S/D metal act as oxygen diffusion barriers during the second oxygen annealing (Fig. 1m). Therefore, oxygen infiltrates locally through the separation ( $t_s$ ) between the TG edge and the S/D contact trenches.

As the BG FET goes through the second oxygen annealing process without TG, the IGZO under the S/D metal has a low O concentration (that is, it has a high  $V_O$  concentration). Owing to this concentration difference,  $V_O$  diffusion occurs from the IGZO under the S/D metal toward the center of the channel, and the resulting donor doping concentration [ $n_0(x)$ ] has a laterally non-uniform profile (shown as a green line in Fig. 1e). The lateral profile of  $n_0(x)$  is a crucial factor in determining the electrical characteristics and the SCE of IGZO FETs, which



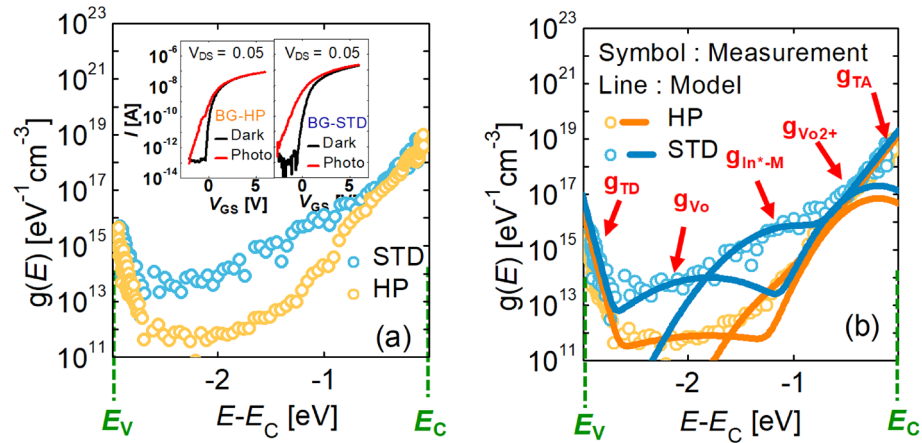
**Figure 2.** The (a) transfer characteristics and (b) device parameters (i.e.,  $V_T$ , SS, and  $\mu_{FE}$ ) of long-channel IGZO FETs ( $L = L_{BG} = 20.2 \mu\text{m}$  and  $L_{TG} = 20 \mu\text{m}$ ). The (c) transfer characteristics and (d) device parameters of short-channel IGZO FETs ( $L = L_{BG} = 0.5 \mu\text{m}$  and  $L_{TG} = 0.3 \mu\text{m}$ ). Error bar was taken from five device samples.

will be modeled in detail later. Compared to BG FET, the O concentration of the channel is relatively low, and the  $N_{CH}$  is higher in DG FET ( $N_{CH,DG} > N_{CH,BG}$ ) because the second oxygen annealing step proceeds in the DG structure while the TG electrode exists. Furthermore, due to O penetrating the  $t_s$ , a local high-concentration O region (that is, a locally low  $n_0$  region) is formed on both edges of the  $L_{TG}$  (shown as the green line in Fig. 1m). This region has a vital role in suppressing the SCE of the submicron IGZO BEOL FET, as will be discussed later.

**IGZO FET DC characterization.** The device sample types are divided into BG and DG according to their structure. They are also divided into STD and HP according to the partial pressure of oxygen during the second O annealing step. The four types of samples are named BG-STD, BG-HP, DG-STD, and DG-HP, respectively. The basic characteristics of the devices were analyzed. Figure 2a,b are the transfer characteristics and device parameters (i.e.,  $V_T$ , SS, and  $\mu_{FE}$ ) for the long-channel devices [channel width ( $W$ )/channel length ( $L$ ) = 1/20.2  $\mu\text{m}$ ] while Fig. 2c,d show the transfer characteristics and device parameters for the short-channel devices ( $W/L = 1/0.5 \mu\text{m}$ ). Here  $\mu_{FE,lin}$  means the  $\mu_{FE}$  extracted in the linear region ( $V_{GS} = 1 \text{ V}$  and  $V_{DS} = 0.05 \text{ V}$ ). Error bars in Fig. 2b,d were taken from five devices. This supports the reproducibility of device parameters. When measuring the transfer characteristics of the DG FET, the BG voltage ( $V_{BG}$ ) was swept, and the TG was floated.  $L_{TG}$  is 20  $\mu\text{m}$  when  $L = L_{BG} = 20.2 \mu\text{m}$ , and is 0.3  $\mu\text{m}$  when  $L = L_{BG} = 0.5 \mu\text{m}$ , which is due to  $t_s = 0.1 \mu\text{m}$ .

As is demonstrated in Fig. 2b,d, the HP sample has a higher  $V_T$ , a smaller SS, and a lower  $\mu_{FE}$  than the STD sample with the same structure and the same  $L$ , regardless of device structure or channel length. For the HP sample, because the amount of O inside the IGZO film is larger than that of the STD sample, the  $V_O$  concentration ( $n_{V_O}$ ) is lower than the STD sample, and so is the  $N_{CH}$ . Since the  $V_O$  plays the role of electron donor inside the IGZO, the  $V_T$  of the HP sample is relatively high. In addition, since the electron transport in IGZO follows a percolation transport<sup>21</sup>, the mobility increases along with electron concentration. The lower  $\mu_{FE}$  in the HP sample is due to the lower electron concentration (relatively lower than in the STD sample). The change in the SS due to the amount of O is related to the trap density at the IGZO/GI interface and in the IGZO thin-film bulk; therefore, it can be explained by analyzing the DOS.

**Subgap DOS extraction.** The DOS was extracted using the photo-response of the  $I-V$  characteristics of the IGZO FET (inset of Fig. 3a). The detailed procedure for the DOS extraction is described in the supplementary information (including Fig. S4 and S5). Figure 3a demonstrates how the DOS of IGZO, extracted from the long-channel BG FET, depends on the amount of O. The bandgap energy ( $E_g$ ) of IGZO is 3 eV, and the extracted DOS consists of the following terms, in the order of increasing energy level from the valence band (VB) maximum level ( $E_V$ ) to the conduction band (CB) minimum level ( $E_C$ ):  $g_{TD}$  (valence band tail states),  $g_{V_O}$  (neutral  $V_O$  states),  $g_{In^{n-M}}$  (undercoordinated In states),  $g_{V_{O2+}}$  (ionized  $V_O$  states), and  $g_{TA}$  (conduction band tail states). Additionally, Fig. 3b shows that the extracted DOS fits well with the proposed DOS model. The DOS  $g(E)$  model formula is calculated in the following equations, and the extracted DOS model parameters are tabulated in Table S1 in the supplementary information.



**Figure 3.** (a) The DOS depending on the O content, extracted from the BG IGZO FETs with  $W/L = 1/20.2 \mu\text{m}$ . The inset shows the measured photo-response of the  $I$ - $V$  curve. (b) The extracted DOS (symbol) fitted with the proposed DOS model (line).

$$g(E) = g_A(E) + g_D(E) \tag{1}$$

$$g_A(E) = g_{TA}(E) + g_{In^{*-}M}(E) = N_{TA} \exp\left(-\frac{E_C - E}{kT_{TA}}\right) + N_{In^{*-}M} \exp\left(-\left(\frac{E_C - E_{In^{*-}M} - E}{kT_{In^{*-}M}}\right)^2\right) \tag{2}$$

$$\begin{aligned} g_D(E) &= g_{TD}(E) + g_{V_o}(E) + g_{V_{O2+}}(E) \\ &= N_{TD} \exp\left(-\frac{E - E_V}{kT_{TD}}\right) + N_{V_o} \exp\left(-\left(\frac{E_V + E_{V_o} - E}{kT_{V_o}}\right)^2\right) \\ &\quad + N_{V_{O2+}} \exp\left(-\left(\frac{E_C - E_{V_{O2+}} - E}{kT_{V_{O2+}}}\right)^2\right) \end{aligned} \tag{3}$$

When the IGZO DOS change by the O annealing conditions was evaluated, the  $g_{V_o}$  of the HP sample with high O concentration was confirmed as small compared with the STD sample. The decrease in  $V_o$  explains this well. In addition,  $g_{In^{*-}M}$ , which indicates the density of the states by the combination of the undercoordinated In and metal cation ( $In^{*-}M$ ), was also relatively lower in the HP sample case. Consistently with<sup>22</sup>, this indicates that the  $In^{*-}M$  probability of bond formation increases as the carrier concentration increases. In addition,  $g_{TA}$  and  $g_{V_{O2+}}$  just below the  $E_C$ <sup>23-25</sup> are relatively low in the HP sample case, which is consistent with that the SS of the HP sample is lower than that of the STD sample (Fig. 2b). Noticeably, the O content-dependent DOS in long-channel BG FETs and the device characteristics are well matched; therefore, the extracted DOS is reasonable.

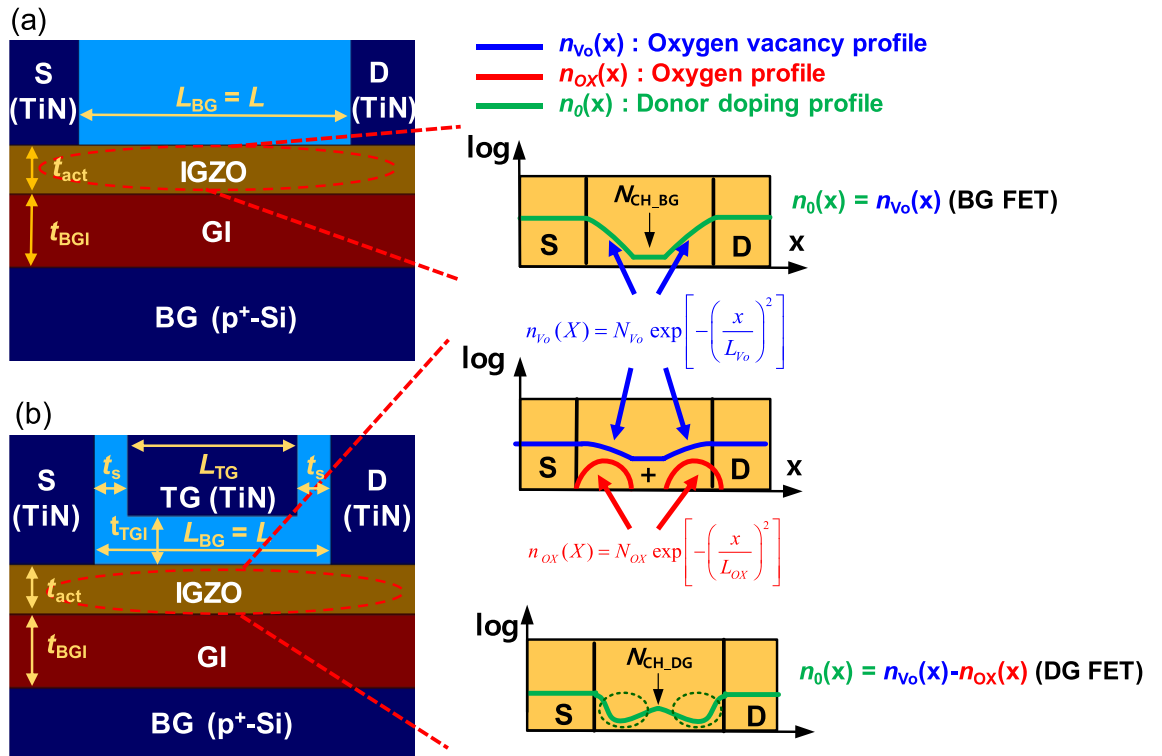
Based on the consistency between DOS and device parameters, it is well understood that under the same O partial pressure condition in a long-channel device, the  $V_T$  of the BG FET is higher than that of the DG FET, and the SS and the  $\mu_{FE}$  are smaller (Fig. 2a,b). This is because the DG device prevents O from infiltrating (compared with the BG device) into the IGZO during the O annealing process.

On the other hand, the changes by the O content and device structure of  $V_T$ , SS, and  $\mu_{FE}$  become complicated in a short-channel device (Fig. 2c,d). While the O-dependent change tendencies of  $V_T$ , SS, and  $\mu_{FE}$  in the same device structure is the same as the long-channel device, the tendency of their changes between the BG-STD and the DG-HP samples is reversed in the short-channel devices (shown as dotted rectangles in Fig. 2b,d). Undoubtedly, this is because the  $V_T$  of the sample, which experienced the same O annealing condition, varied with  $L$ .

The understanding of the  $L$ -dependence of  $V_T$  is eventually central to a robust design of submicron AOS FETs. To understand either the SCE of IGZO FETs or the effect of O content and structure on the SCE, appropriate device modeling and simulation are necessary and should be supported for a robust design of a submicron IGZO FET immune to the SCE.

### Modeling and simulation

**Device model and parameter extraction.** To obtain the robust framework for material-process-device co-design of submicron IGZO FETs, we performed device modeling and incorporated it into a TCAD simulation. First, as is shown in Fig. 4, the BG FET and DG FET device structures were implemented with the TCAD, and the  $n_{V_o}(x)$  and  $n_{Ox}(x)$  profiles were generated along with the O annealing process conditions and modeled



**Figure 4.** Models for  $n_{vo}(x)$  and  $n_0(x)$  considering the device structure and process conditions, which are implemented by the TCAD device simulator for the (a) BG FET and the (b) DG FET structure.

by the equations in Fig. 4. Here  $n_{ox}$  is the concentration of oxygen which is additionally employed during the second oxygen anneal in DG FETs.

In our modeling, the  $n_{vo}(x)$  and  $n_{ox}(x)$  were assumed to be Gaussian profiles through the previous consideration of the two-step O annealing process and the STD/HP conditions. The  $L_{vo}$  and  $L_{ox}$  mean characteristic lengths, which are associated with the respective diffusivity of  $V_o$  and O during the oxygen annealing, describing the  $n_{vo}(x)$  and  $n_{ox}(x)$ . Final donor doping profile [ $n_0(x)$ ] of the BG FET is determined by the combination of the  $n_{vo}(x)$  near the S/D extension and the  $N_{CH\_BG}$  in the center of a channel. In contrast, the final  $n_0(x)$  of the DG FET is determined as  $n_{vo}(x) - n_{ox}(x)$  near the S/D extension and the  $N_{CH\_DG}$  in the channel part. Then, the  $N_{ox}$  was determined as  $N_{ox} = N_{CH\_BG} - N_{CH\_DG}$  because the additional oxygen would compensate the donor concentration.

The detailed procedure for extracting the model parameters is described in Fig. S6 in the supplementary information. The process is outlined as follows. First, after inputting the material parameters and the device structural parameters into the TCAD, we designated the experimentally extracted DOS model into the IGZO active layer. Based on the DOS parameter, the electron effective mass ( $m_n^*$ ) and the CB effective DOS ( $N_C$ ) were determined through the formulas below<sup>26</sup>.

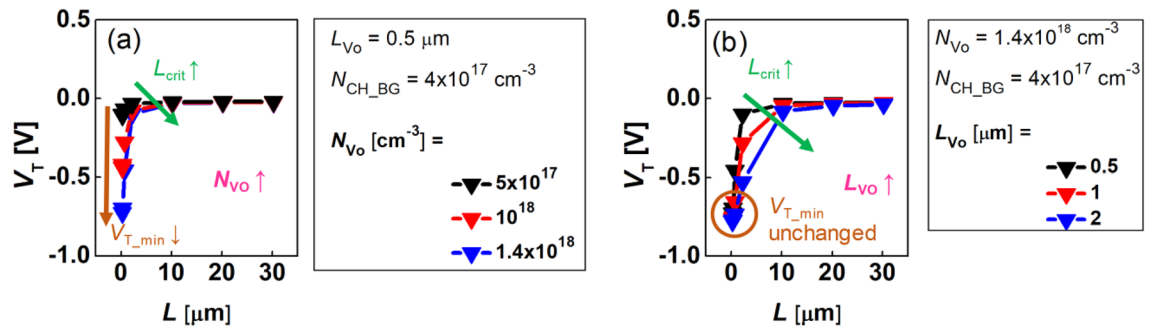
$$m_n^* = \left( \frac{N_{TA}}{4.9 \times 10^{21} \sqrt{kT_{TA}}} \right)^{\frac{2}{3}} \times m_0 \tag{4}$$

$$N_C = 4.9 \times 10^{21} \left( \frac{m_n^*}{0.34m_0} \right)^{\frac{3}{2}} \tag{5}$$

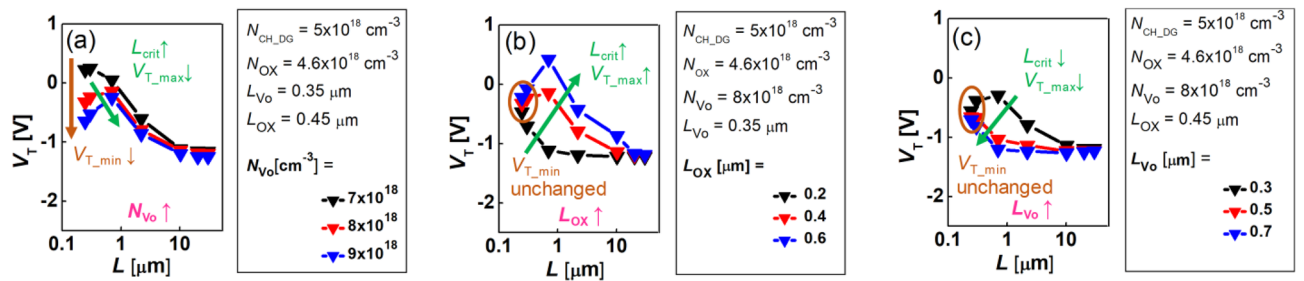
Then, the  $N_{CH}$  and the charge density in GI ( $Q_{ox}$ ) were fitted by comparing the simulated  $V_T$  and flat band voltage ( $V_{FB}$ ) and the measured ones. After that, the CB mobility ( $\mu_{band}$ ) was adjusted by the numerical iteration until the simulated  $\partial I_D / \partial V_{GS}$  and measured  $\partial I_D / \partial V_{GS}$  were in good agreement at various  $V_{DS}$ 's. In these fitting processes, the numerical iteration was allowed until the average error between the simulated and measured values fell within a specific error rate (ER). The ER can be selected considering the trade-off between the precision of the model parameter and the computing burden of simulation. An ER = 10% was used in this study.

Next, the parameters that defined the lateral profile of the carrier doping concentration (e.g.,  $N_{vo}$ ,  $L_{vo}$ ,  $N_{ox}$ , and  $L_{ox}$ ) were decided. These parameters were extracted using the point that they affected the  $V_T$  roll-off characteristic, i.e., the  $L$ -dependency of  $V_T$ , of the short-channel FET. Since the  $n_0(x)$  of the BG FET was determined by the  $n_{vo}(x)$ , we performed the simulation study (Fig. 5) to understand the effect of  $N_{vo}$  and  $L_{vo}$  changes on the  $V_T$  roll-off characteristic.

As is shown in Fig. 5, the  $V_T$  roll-off occurs as  $L$  becomes shorter in the BG FET. Here, the channel length at which the  $V_T$  roll-off begins is defined as  $L = L_{crit}$ , and the  $V_T$  at the minimum  $L$  ( $L = 0.245 \mu m$ ) is defined as



**Figure 5.** The TCAD simulation results for the  $L$ -dependent  $V_T$  in BG FETs with the variations of (a)  $N_{VO}$  and (b)  $L_{VO}$ .



**Figure 6.** The TCAD simulation results for the  $L$ -dependent  $V_T$  in DG FETs by splitting the (a)  $N_{VO}$ , (b)  $L_{OX}$ , and (c)  $L_{VO}$ .

$V_{T\_min}$ . As demonstrated in Fig. 5a, as the  $N_{VO}$  becomes higher, the  $L_{crit}$  becomes longer, and the  $V_{T\_min}$  becomes lower simultaneously. It is also shown in Fig. 5b that as the  $L_{VO}$  becomes longer, the  $L_{crit}$  becomes more extended, but  $V_{T\_min}$  is independent of the  $L_{VO}$ . Therefore, in the BG FET, the  $N_{VO}$  can be extracted through a fitting with the measured  $V_{T\_min}$  under a fixed  $N_{CH\_BG}$  condition, and then the  $L_{VO}$  can be extracted through the second fitting with the measured  $L_{crit}$  at a fixed  $N_{VO}$ .

In the DG FET, the changes either in  $N_{VO}$  and  $L_{VO}$  or in  $N_{OX}$  and  $L_{OX}$  affect the  $V_T$  roll-off characteristic since the  $n_0(x)$  is determined by the combination of the  $n_{VO}(x)$  and the  $n_{OX}(x)$ . Therefore, in the DG FET, a more complex  $L$ -dependency of the  $V_T$  appears compared with the BG FET as seen in Fig. 6. More interestingly, the reverse SCE appears in the medium  $L$  range where the  $V_T$  increases as the  $L$  decreases. Here, when the maximum value of the  $L$ -dependent  $V_T$  is defined by  $V_{T\_max}$ ,  $L_{crit}$  can be re-defined particularly in DG FET as the  $L$  where the  $L$ -dependency of  $V_T$  interchanges between the increase and decrease in  $V_T(L)$ . Then, as the  $N_{VO}$  increases,  $V_{T\_min}$  decreases,  $L_{crit}$  increases, and  $V_{T\_max}$  decreases (Fig. 6a). In addition, as  $L_{OX}$  becomes longer, both  $L_{crit}$  and  $V_{T\_max}$  increase, but the  $V_{T\_min}$  is independent of the  $L_{OX}$  (Fig. 6b). Moreover, as  $L_{VO}$  lengthens, both  $L_{crit}$  and  $V_{T\_max}$  decrease, but the  $V_{T\_min}$  is immune to the variation of  $L_{VO}$  (Fig. 6c).

Therefore, in the DG FET, the parameters, such as  $N_{VO}$ ,  $L_{VO}$ ,  $N_{OX}$ ,  $L_{OX}$ , and  $N_{CH\_DG}$ , can be extracted through the relationship of  $N_{OX} = N_{CH\_BG} - N_{CH\_DG}$  and a fitting between the measured  $V_{T\_min}$ ,  $L_{crit}$ , and  $V_{T\_max}$  and simulated values under the given  $N_{CH\_BG}$  condition.

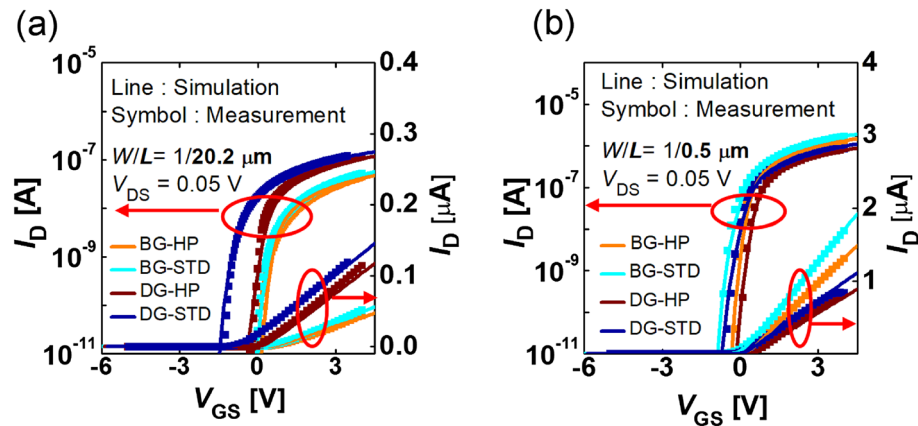
The extracted model parameters are summarized in Table S1 (supplementary information).

**TCAD simulation.** The TCAD framework was setup for each process condition (HP/STD) and structure (BG/DG) by using the parameter set summarized in Table S1. The simulated and measured  $I$ - $V$  characteristics are compared with each other (Fig. 7a,b). In the four types of samples (BG-STD, BG-HP, DG-STD, and DG-HP), all the TCAD simulation results reproduce well the measured  $I$ - $V$  curves and parameters, i.e.,  $V_T$ , SS, and  $\mu_{FE}$ , for both the long-channel (Fig. 7a) and short-channel FETs (Fig. 7b).

Considering the discrepancies between the measured and simulated results, the ER range is 1.16–13.1%. The main cause of this difference is expected to be due to the bias-dependent mobility of the AOS FETs, suggesting that further studies are needed. In Fig. 7a ( $L = 20.2 \mu\text{m}$ ), the ER for BG-HP, BG-STD, DG-HP, and DG-STD is 7.35, 5.57, 13.1, and 3.82%, respectively. Meanwhile, in Fig. 7b ( $L = 0.5 \mu\text{m}$ ), each ER for BG-HP, BG-STD, DG-HP, and DG-STD is 1.16, 3.67, 8.65, and 9.48%.

These values are consistent with the critical ER ( $< 10\%$ ) used in extracting model parameters. Therefore, the proposed model and model parameter extraction are reasonable and accurate enough to expect the electrical characteristics of AOS FETs.

Noticeably, using the  $L$  vs.  $V_T$  relationship in Figs. 5 and 6, we can extract the Gaussian doping parameters for each structure and process condition (Fig. 4) as a unique set. This means that the O and  $V_O$  diffusion effects are reflected well along with every  $L$ , process condition, and structure (including the minimum  $L$  of 245 nm). As seen in Table S1, in the long  $L$ , the  $N_{CH}$  was higher in the order of DG-STD, DG-HP, BG-STD, and BG-HP.



**Figure 7.** The TCAD simulation (line) vs. the measurement data (symbol). (a)  $I$ - $V$  curve at  $W/L=1/20.2 \mu\text{m}$ , and (b)  $I$ - $V$  curve at  $W/L=1/0.5 \mu\text{m}$ .

In the second O annealing step of the BG structure, since there is no O diffusion barrier,  $N_{\text{CH,DG}}$  is higher than  $N_{\text{CH,BG}}$ . In the same structure, the  $N_{\text{CH}}$  of the STD device is higher than that of the HP device.

## Discussion

**Short-channel effects.** Understanding why the  $L$ -dependency of  $V_T$  in the BG FET changes along the variations of  $L_{\text{Vo}}$  and  $N_{\text{Vo}}$  (Fig. 5) is central to the design of the doping profile of the submicron AOS FET. Similarly, understanding why the  $L$ -dependency of  $V_T$  of the DG FET changes along with the variations of  $L_{\text{Vo}}$ ,  $N_{\text{Vo}}$ , and  $L_{\text{OX}}$  (Fig. 6) is central to the design of the immunity to SCE in the submicron AOS FET.

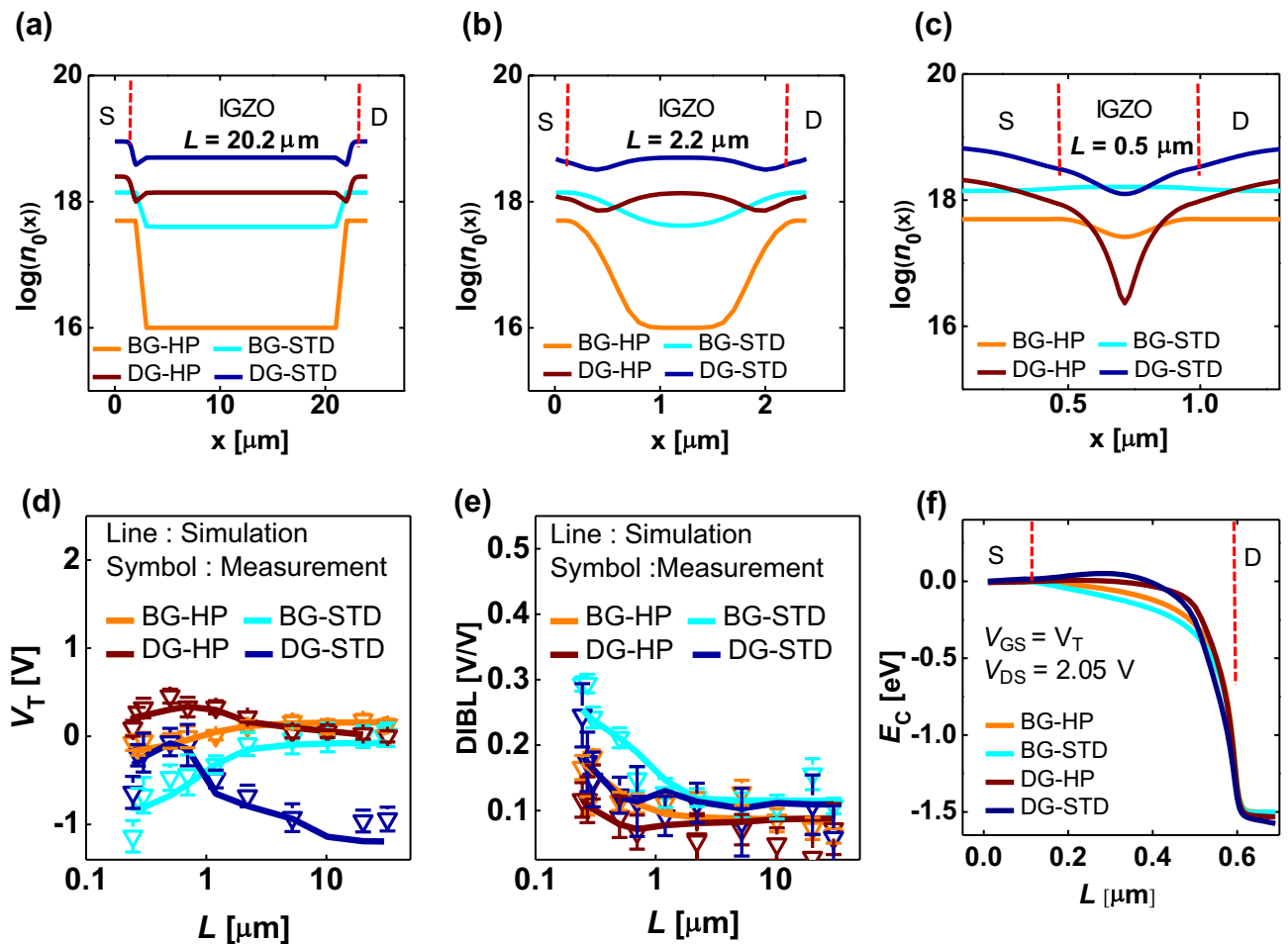
First, for the BG FET, the  $n_0(x)$  is composed of  $N_{\text{Vo}}$  (S/D region),  $n_{\text{Vo}}(x) = N_{\text{Vo}} \times e^{-\left(\frac{x}{L_{\text{Vo}}}\right)^2}$  (S/D extension area), and  $N_{\text{CH,BG}}$  (the center of the channel), as illustrated in Fig. 4a. At this time, the  $N_{\text{Vo}}$  is determined by the amount of the  $V_{\text{O}}$  employed in the IGZO film, which is controlled by the amount of the O inflow and the temperature during the IGZO deposition. The diffusion length of  $V_{\text{O}}$  ( $L_{\text{Vo}}$ ) is also determined by either the lateral diffusivity of  $V_{\text{O}}$  or the thermal budget during the process. In the same process conditions, when the  $L$  becomes shorter and comparable to the scale of the  $L_{\text{Vo}}$ , then the  $n_{\text{Vo}}(x)$  profiles of both the source and drain merge in the center of the channel to effectively increase the  $N_{\text{CH}}$ ; therefore, the  $V_T$  starts to decrease. That is, when the  $L = L_{\text{crit}}$ , the  $N_{\text{CH,BG}}$  increases compared with the long-length device, and the  $V_T$  roll-off phenomenon begins to occur. Accordingly, as the  $L_{\text{Vo}}$  lengthens and the  $N_{\text{Vo}}$  becomes higher, the longer  $L_{\text{crit}}$  becomes (the SCE becomes severe) because the  $n_{\text{Vo}}(x)$  starts to intersect at the channel center at the longer  $L$  (Fig. 5a). At the minimum  $L$  ( $L = 0.245 \mu\text{m}$ ), the channel length is too short, and the donor doping concentration in the center of the channel approaches  $N_{\text{Vo}}$ , i.e., the peak value of the Gaussian donor doping  $n_{\text{Vo}}(x)$ , independently of the  $L_{\text{Vo}}$ . Therefore, the  $V_{T,\text{min}}$  is only affected by  $N_{\text{Vo}}$  (Fig. 5b).

On the other hand, in the DG FET (Fig. 6), if the locally high O concentration area (formed during the second O annealing step) is described as the Gaussian acceptor profile  $n_{\text{OX}}(x) = N_{\text{OX}} \times e^{-\left(\frac{x}{L_{\text{OX}}}\right)^2}$ , then the  $n_0(x)$  consists of the  $N_{\text{Vo}}$  in the S/D area, the  $n_{\text{Vo}}(x) - n_{\text{OX}}(x)$  in the S/D extension area, and the  $N_{\text{CH,DG}}$  in the center of the channel. At this time, the O diffusion length  $L_{\text{OX}}$  is determined by either the lateral diffusivity of O or the thermal budget during the process. Since the  $n_{\text{OX}}(x)$  region is relatively closer to the channel center than the  $n_{\text{Vo}}(x)$  region, when  $L$  is shortened, the locally higher  $n_{\text{OX}}(x)$  [locally lower  $n_0(x)$ ] regions are merged first, and then  $V_T$  increases. That is, as shown in Fig. 6, a  $V_T$  roll-up (the reverse SCE) is observed ( $V_{T,\text{max}}$  is observed).

Furthermore, as  $L$  becomes further shorter, the merge in the  $n_{\text{Vo}}(x)$  section is overlapped. Then, a  $V_T$  roll-off section, where  $V_T$  decreases again, is observed. Meanwhile, as  $L_{\text{Vo}}$  increases, the  $N_{\text{CH,DG}}$  also increases and  $V_{T,\text{max}}$  decreases. In this case, as  $L_{\text{Vo}}$  increases,  $L_{\text{crit}}$  shortens since the influence of the  $n_{\text{OX}}(x)$  also decreases (Fig. 6a). In addition, as  $L_{\text{OX}}$  lengthens,  $V_{T,\text{max}}$  increases because the  $N_{\text{CH,DG}}$  decreases. However,  $L_{\text{crit}}$  lengthens because the  $N_{\text{CH,DG}}$ , which has already been lowered, makes the  $n_{\text{Vo}}(x)$  overlap followed by the decrease in  $V_T$  occur at a longer  $L$  (Fig. 6b). Finally, at the minimum  $L$  ( $L = 0.245 \mu\text{m}$ ), the  $N_{\text{CH,DG}}$  (also  $V_{T,\text{min}}$ ) is determined by the combination of the  $N_{\text{Vo}}$  and  $N_{\text{OX}}$  regardless of the  $L_{\text{OX}}$  and  $L_{\text{Vo}}$  because the channel length is too short (Fig. 6b,c). Thus, when the  $N_{\text{OX}}$  is fixed,  $L_{\text{crit}}$  shortens and  $V_{T,\text{max}}$  decreases as the  $L_{\text{Vo}}$  lengthens (Fig. 6c).

Hence it needs to be explained why, in a short-channel case, the  $V_T$  of the DG FET increases overall and the  $\mu_{\text{FE}}$  decreases overall compared with the BG FET (the dotted boxes in Fig. 2b,d). As explained above, the  $N_{\text{CH,DG}}$  is higher than  $N_{\text{CH,BG}}$  in the long  $L$ . Therefore, the DG device has a lower  $V_T$  and a higher  $\mu_{\text{FE}}$  when compared with the BG device. However, in a short-channel case, the  $N_{\text{CH,DG}}$  is lower than that of the  $N_{\text{CH,BG}}$  due to the merging phenomenon of the  $n_{\text{OX}}(x)$ , so that the DG device has a higher  $V_T$  and a lower  $\mu_{\text{FE}}$  than the BG device (Fig. 8a–c). Furthermore, at the same process condition, the SS of the DG device is higher in the short channel ( $L = 0.5 \mu\text{m}$ ) than that of the BG device, whereas the SS in the long channel is immune to the device structure and process. This is because in the DG device with a short  $L$ , there is a big difference between the resistance of the channel and that of the S/D extension (Fig. 8a–c), so the lateral electric field by the drain voltage becomes more focused on the channel center, and the vertical electric field by the gate voltage acts relatively weakly; therefore, this weakens the gate controllability.





**Figure 8.** The TCAD-simulated  $n_0(x)$  profiles in the four types of samples along the structures and processes with varying channel length. (a)  $L = 20.2 \mu\text{m}$ , (b)  $L = 2.2 \mu\text{m}$ , and (c)  $L = 0.5 \mu\text{m}$ . The TCAD simulated (line) vs. the measured (symbol)  $L$ -dependent (d)  $V_T$  and (e) DIBL. Error bar was taken from six device samples. (f) The energy band obtained through the TCAD simulation for the BG-HP, BG-STD, DG-HP, and DG-STD devices at  $W/L = 0.5/1 \mu\text{m}$ .

The symbols in Fig. 8d,e show the  $L$ -dependent  $V_T$  and DIBL characteristics measured in the IGZO FET. Error bars were taken from six devices. These two characteristics are the performance index representing the SCE. In addition, the lines in Fig. 8d,e show the TCAD simulation results (using the model parameters in Table S1) reproduce well the  $L$ -dependent  $V_T$  and DIBL characteristics over a wide range of the  $L$ . Based on these results, the model parameter extraction process and the parameter values confirm that the O and  $V_O$  diffusion effects are reflected well over a wide range of the  $L$ . This is also reasonable for the variations of process condition and device structure, both qualitatively and quantitatively.

In Fig. 8d, when the  $V_T$  roll-off occurs in the BG FET, the HP device is more immune to the SCE than in the STD device (that is, the  $L_{crit}$  is longer). This is because the HP device has a relatively lower  $N_{CH}$  and  $N_{V_0}$  than the STD device. Here, it is worthwhile to note that the  $L_{V_0}$  of HP device is  $\times 1/5$  to  $\times 1/3$  shorter than that of STD device (Table S1). It indicates that the more O-poor the IGZO active layer is, the more active the lateral diffusion of the  $V_O$  and the longer the diffusion length of the  $V_O$  will be. Our finding is consistent with the results of studies that indicate that the diffusion length of the  $V_O$  increases when the  $N_{V_0}$  is high<sup>27</sup>.

Meanwhile, in the DG FET (as was already shown in Fig. 6), the  $V_T$  roll-up (the reverse SCE) is observed along with a decreasing  $L$ , and the DG-HP device suppresses the SCE more effectively than the DG-STD device. As shown in  $N_{OX}$  and  $L_{OX}$  in Table S1, the  $n_{OX}(x)$  spreads more broadly in the DG-HP device, which lowers  $N_{OX}$  and lengthens  $L_{OX}$ , when compared with the DG-STD device. This broadening further reduces the  $N_{CH,DG}$  (Fig. 8c), and both the  $V_T$  roll-off and roll-up are consequently suppressed by weakening the lateral-merge effect of the  $n_{V_0}$  and the  $n_{OX}$ . Therefore, if the DG-HP device is optimized further, it is expected to effectively suppress the SCE while satisfying a positive  $V_T$ , which is an essential requirement from the circuit aspect.

**Device design perspective.** The following points should be noted: the spread of the  $n_{V_0}$  in the first O annealing step increases as it becomes more O-poor (the  $n_{V_0}$  spread in the STD device is larger than that in the HP device), and the spread of the  $n_{OX}$  in the second O annealing step increases as it becomes more O-rich (broader  $n_{OX}$  in the DG-HP device rather than in the DG-STD device). Therefore, if the O pressure during the

Index Ref.	Device structure	A [ $\mu\text{A}/\text{V}^2$ ]	B [ $\text{cm}^2/\text{V}\cdot\text{s}$ ]	$V_T$ [V]	$\mu$ [ $\text{cm}^2/\text{V}\cdot\text{s}$ ]	SS [mV/dec]	$L_{\min}$ [nm]	DIBL ( $L_{\min}$ ) [V/V]	$V_T(L_{\max}) - V_T(L_{\min})$ [V]
This work	DG/BG	2.56	7.84	0.3	8	94	245	0.1	-0.1 (DG) 0.19 (BG)
<sup>3</sup>	FinFET	4.31	7.5	0.9	10.3	100	72	-	-
<sup>5</sup>	FinFET	2.33	4.05	1.44	10.2	79	25	-	-
<sup>6</sup>	FinFET	2.05	3.57	0.9	10.5	87	21	0.1	-
<sup>7</sup>	TG	0.11	0.23	-0.8	-	-	45	-	0.1
<sup>10</sup>	GAA	1.4	1.18	-1.1	10	100	20,000	-	-
<sup>12</sup>	TG	0.27	8.04	0.55	12.1	100	6500	-	-
<sup>13</sup>	TG	-	-	0.9	8.4	110	6000	-	-
<sup>15</sup>	TG	0.15	4.34	0.9	10.5	180	6000	-	-
<sup>17</sup>	TG	-	-	0.9	6	160	15,000	-	-
<sup>18</sup>	TG	0.45	13.03	0.1	7.5	-	6000	-	-
<sup>19</sup>	BG	-	-	-0.4	-	175	245	-	-
<sup>23</sup>	BG	-	-	0.5	5.1	105	15,000	-	-
<sup>24</sup>	BG	-	-	0.2	9	274	10,000	-	-

**Table 1.** Summary of the performance indices compared with previous studies.

second annealing step and the  $t_s$  are further optimized in the two-step O annealing process, we can expect that the  $V_T$  will become more immune to the scale-down of  $L$ .

The TCAD-simulated energy band is shown in Fig. 8f. The DIBL is small in the following device order: DG-HP, BG-HP, DG-STD, and BG-STD, which is consistent with Fig. 8e. The overall tendency shows that the HP device has a smaller DIBL than the STD device, and the DG structure has a smaller DIBL than the BG structure. The HP structure is more robust to DIBL than the STD structure for the following two reasons; first, since the HP structure has a low  $N_{\text{CH}}$  and the Fermi energy level ( $E_F$ ) is lower than that of the STD structure, a high energy barrier is formed between the S/D and the channel. Second, the  $L_{\text{vo}}$  of the HP device is shorter than that of the STD device. If the  $L_{\text{vo}}$  is long, the channel area where the  $E_F$  rises gets longer, and the potential barrier lowers between the source and the channel, which makes it more vulnerable to the DIBL.

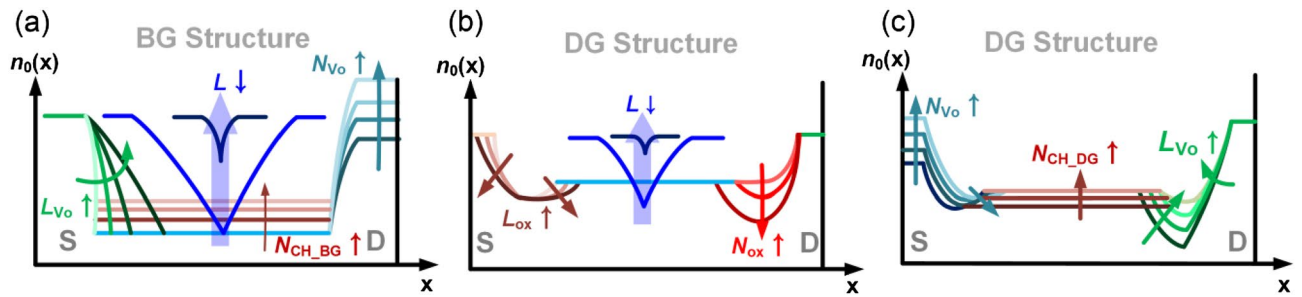
In the DG devices, the voltage drop by the  $V_{\text{DS}}$  is large because of the existence of a  $n_{\text{OX}}$  region with large resistance. Thus, the DIBL is suppressed in DG FET. This effect is further enhanced in the HP process (the resistance of the  $n_{\text{OX}}$  region becomes larger). The role of this  $n_{\text{OX}}$  region is very reminiscent of the role of halo (or pocket) implantation to block SCE in submicron CMOSFETs. The DG-HP device is the most advantageous from the DIBL point of view (similar to the  $V_T$  roll-off), and the DIBL is expected to be suppressed more effectively through further optimization.

To compare the performance of devices utilized in this study with previous studies, we compared the main device parameters with those of references, as summarized in Table 1. It should be noted that, since the operating voltage, device structure, and size are different for each device, it is necessary to define another new index for a fair comparison. In the case of mobility, for example, since either the voltage condition from which the mobility is extracted or the channel length is different, it is difficult to evaluate as the performance indicator of AOS. Therefore, we defined  $\alpha$  and  $\beta$  as new indices.  $\alpha$  is defined by  $\alpha = \frac{I_D \times L_{\min}}{W \times (V_{\text{GS}} - V_T) \times V_{\text{DS}}}$  and means the operating current normalized by the device size, gate overdrive voltage, and drain voltage.  $\beta$  is also defined by  $\beta = \frac{\alpha}{C_{\text{ox}}}$ , means the current further normalized by  $C_{\text{ox}}$ , and has the same unit as the mobility. That is, if  $\beta$  is used, fair comparison is possible even if the operating voltage, gate capacitive coupling, and device size are different. In the case of our device, assessed by  $\beta$ , it is confirmed that the performance is excellent compared to the devices of the previous studies. Furthermore, in the viewpoint of  $L_{\min}$ , it is found that our device shows good scalability except for the 3D device structure such as FinFET. From the SCE point of view, it can be seen that the previous studies rarely reported on  $V_T$  roll-off or DIBL. Noticeably, our study is a rare case that reports both DIBL and  $V_T$  roll-off, and it is confirmed that our device shows very good SCE properties despite not having a 3D structure.

A method that can optimize  $V_T$ , SS,  $\mu_{\text{FE}}$  and SCE in of the submicron AOS FET is vital, and the key is to control the  $n_0(x)$  with a combination of  $V_{\text{O}}$  and O. Figure 9 illustrates the change of  $n_0(x)$  by the variations of  $L_{\text{vo}}$ ,  $N_{\text{vo}}$ ,  $N_{\text{CH,BG}}$ , and  $L$ . If we perform the co-optimization of  $t_s$ ,  $N_{\text{vo}}$ ,  $L_{\text{vo}}$ ,  $N_{\text{OX}}$ , and  $L_{\text{OX}}$  by using both a two-step O annealing and DG structure after we make the IGZO active film sufficiently O-poor and fully raise the CB mobility at the beginning of the process, we will be able to implement AOS BEOL FETs that comprehensively satisfy the  $V_T$ , SS,  $\mu_{\text{FE}}$ , and SCE parameters that match the performance and specification of the application-dependent circuits.

## Conclusion

The DOS-based device model and TCAD simulation framework were proposed with emphasis on the control of  $n_0(x)$ , and were demonstrated in the BG/DG IGZO FETs with  $L = 0.245\text{--}20.2 \mu\text{m}$ . The validity of the device model and its parameters were proved through a TCAD simulation reflecting the extracted model parameters and the IGZO DOS. Based on a two-step O annealing, the effect of O partial pressure on not only the device performance parameters, such as  $V_T$ , SCE, SS, and  $\mu_{\text{FE}}$ , but also DOS was elucidated. The simulation results



**Figure 9.** (a) Change of  $n_0(x)$  by the variations of  $L_{VO}$ ,  $N_{VO}$ ,  $N_{CH\_BG}$ , and  $L$  in the BG structure. (b) Change of  $n_0(x)$  by the variations of  $L$ ,  $L_{OX}$ , and  $N_{OX}$  in the DG structure. (c) Change of  $n_0(x)$  by the variations of  $N_{VO}$ ,  $N_{CH\_DG}$ , and  $L_{VO}$  in the DG structure.

explained successfully the measured  $V_T$  roll-off and DIBL characteristics. The results of an analysis based on the proposed model and the extracted parameters indicate that the SCE of submicron AOS FETs is effectively suppressed when the local high O-concentration region (formed by applying the two-step O annealing to the DG FET) is used. We also found that  $L_{VO}$  becomes longer as the device becomes O-poor, and  $L_{OX}$  becomes longer as the device becomes O-rich.

Our results show that the co-optimization of  $t_s$ ,  $N_{VO}$ ,  $L_{VO}$ ,  $N_{OX}$ , and  $L_{OX}$  is vital to the immunity to SCE in AOS FETs. Proposed model and simulation framework are potentially useful to a comprehensive optimization of the device performance parameters, i.e.,  $V_T$ , SCE, SS, and  $\mu_{FE}$ , for the submicron AOS BEOL FET technology.

## Methods

**IGZO FET characterization.** In this study, to analyze the  $I_D$ - $V_{GS}$  characteristics of the IGZO FET, HP4156C (Keithley, Santa Rosa, CA, USA) was used, and the measurements were taken in a dark state at room temperature. The measurement conditions were as follows; the gate-to-source voltage ( $V_{GS}$ ) was swept from 4 to  $-6$  V in  $-0.05$  V steps, and the drain-to-source voltage ( $V_{DS}$ ) was fixed at 0.05 V. The  $V_T$  was extracted by the  $V_{GS}$  at  $I_D/(W/L) = 10^{-8}$  A, and the SS was extracted by  $I_D/(W/L) = 10^{-10}$ - $10^{-9}$  A. In addition, the  $\mu_{FE\_lin}$  was calculated at  $V_{GS} - V_T = 3$  V by using the following equation.

$$\mu_{FE\_lin} = \frac{dI_D}{dV_{GS}} \times \frac{L}{W \times V_{DS} \times C_{ox}}$$

The DIBL was calculated from the difference between the  $V_T$  at  $V_{DS} = 0.05$  V and the  $V_T$  at  $V_{DS} = 1.05$  V.

**Error evaluation.** In the case of measured data, the mean value and error bar were calculated by using the root mean square (RMS) value as follows ( $x$  = measurement value,  $m$  = mean,  $n$  = number of data):

$$\text{Error bar} = \sqrt{\frac{\sum^n (x - m)^2}{n}} \quad \text{and} \quad m = \frac{\sum^n |x|}{n}.$$

These mean and error bar were used in Fig. 2b,d, and in Fig. 8d,e.

In addition, for comparing the measured and simulated data, the error rate (ER) was calculated as follows ( $y$  = simulation data,  $m_{abs}$  = average of absolute values of measured data).

$$\text{RMS} = \sqrt{\frac{\sum^n (y - x)^2}{n}}, \quad m_{abs} = \frac{\sum^n |x|}{n}, \quad \text{and} \quad \text{ER} = \frac{\text{RMS}}{m_{abs}} \times 100 (\%)$$

This ER was used in Fig. 7.

## Data availability

The datasets used or analyzed during the current study are available from the corresponding author on reasonable request.

Received: 18 August 2022; Accepted: 8 November 2022

Published online: 12 November 2022

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## Acknowledgements

This work was supported in part by Samsung Electronics Co., Ltd under Grant IO200424-07306-01, in part by the National Research Foundation of Korea (NRF) funded by the Ministry of Science and ICT (MSIT) of Korea Government under Grant 2016R1A5A1012966 and 2020R1A2B5B01001979, and in part by the Institute of Information and Communications Technology Planning and Evaluation (IITP) funded by the Korea government (MSIT) under grant 2021-0-01764. Submicron IGZO FET samples was fabricated by imec. TCAD simulation was supported by SILVACO. The EDA tool was supported by the IC Design Education Center (IDEC), south Korea.

## Author contributions

D.K. and D.H.K. designed this work and wrote the main part of manuscript. D.K., J.-H.K., W.S.C., T.J.Y., and J.T.J. performed the device characterization, modeling and TCAD simulation. A.B., N.R., S.S., R.D., and G.S.K. contributed to the design and fabrication of the submicron IGZO FETs. D.K., A.B., S.S., R.D., W.L., M.H.C., D.H., and D.H.K. discussed the results. The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

## Competing interests

The authors declare no competing interests.

## Additional information

**Supplementary Information** The online version contains supplementary material available at <https://doi.org/10.1038/s41598-022-23951-x>.

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