A Snapshot Review on Metal-Semiconductor Contact Exploration for 7 nm CMOS Technology and Beyond

Hao Yu[1], Marc Schaekers[1], Jean-Luc Everaert[1],
Naoto Horiguchi[1], Kristin De Meyer[1,2], Nadine Collaert[1]
[1]*imec, Kapeldreef 75, Leven, Belgium*
[2]*Katholieke Universiteit Leuven, Dept. ESAT, Leuven, Belgium*
[*]hao.yu@imec.be

Abstract: Contact resistances take a significant portion of on-state resistances of advanced Si CMOS transistors. As a result, a metal-semiconductor contact resistivity (ρ_c) of sub-10^{-8} $\Omega\cdot cm^2$ or even sub-10^{-9} $\Omega\cdot cm^2$ is required to achieve high performance for a very downscaled transistor. In this snapshot review on our ρ_c investigation efforts, we first introduce a test structure—a multiring circular transmission line model (MR-CTLM)—with high accuracy to measure ultralow ρ_c, and then we evaluate different contact solutions. Our contact solution exploration includes metal/insulator/semiconductor (MIS) contacts for n^+-Si and advanced (gemano-)silicides for n^+-Si and p^+-SiGe. We discuss limitations of MIS contacts. And we demonstrate encouraging ρ_c of 10^{-9} $\Omega\cdot cm^2$ that meet the requirement of 7 nm or 5 nm CMOS technology nodes. We also briefly discuss the current ρ_c investigation status of n^+-Ge and n^+-InGaAs—two potential NMOS channel candidates.

1. Introduction

The long journey of CMOS downscaling has approached physical limits in multiple ends. In the past several technology nodes, the traditionally constant dimensional downscaling factor [1] applies no longer to every component of CMOS transistors; rather, the transistor downscaling mission has been reallocated among different components. For example (see the schematic in Fig. 1b), along transistor length, downscaling of the gate length (L_g) has much slowed down in the past several technology nodes to suppress short channel effects, while source/drain (S/D) contact length (L_c) and spacer thickness (t_{sp}) have got thus harder compressed [2], [3]. It is expected that in 14 nm and 7 nm CMOS technology nodes, L_c are as small as ~20 nm and ~14 nm, respectively [20]. Because the L_c is extremely confined and the metal gate scheme has been used, the conventional self-aligned silicidation (Salicide) process [4] (see the schematic in Fig. 1a) is no longer practical and beneficial. Instead, from 14 nm technology node onwards [5], S/D contact metals are deposited at the bottom of the via—these contacts are thus referred to as liner contacts [6]. Because of extreme L_c shrinkage in recent technology nodes, the contact resistance (R_c) of liner contacts becomes a performance killer of modern CMOS front-end transistors [7]. To reduce R_c, expansion of contact area and reduction of contact resistivity (ρ_c) are desired.

Making use of the 3D features of advanced transistors, novel schemes like raised S/D (Fig. 1d) [9] and wrap-around S/D (Fig. 1e and Fig. 1f) [10], [11] are effective to increase contact area. Besides S/D shape engineering, conformal metal deposition techniques [10], [11] help to further maximize contact area.

With contact area being optimized, one would rely on ρ_c reduction to further minimize R_c. Assuming that R_c composes 25% percent of the on-state resistance of transistors, the 7 nm/5 nm CMOS technology nodes require ρ_c to be lower than 2×10^{-9} $\Omega\cdot cm^2$ [12]. These ultralow ρ_c challenge not only S/D contact formation techniques but

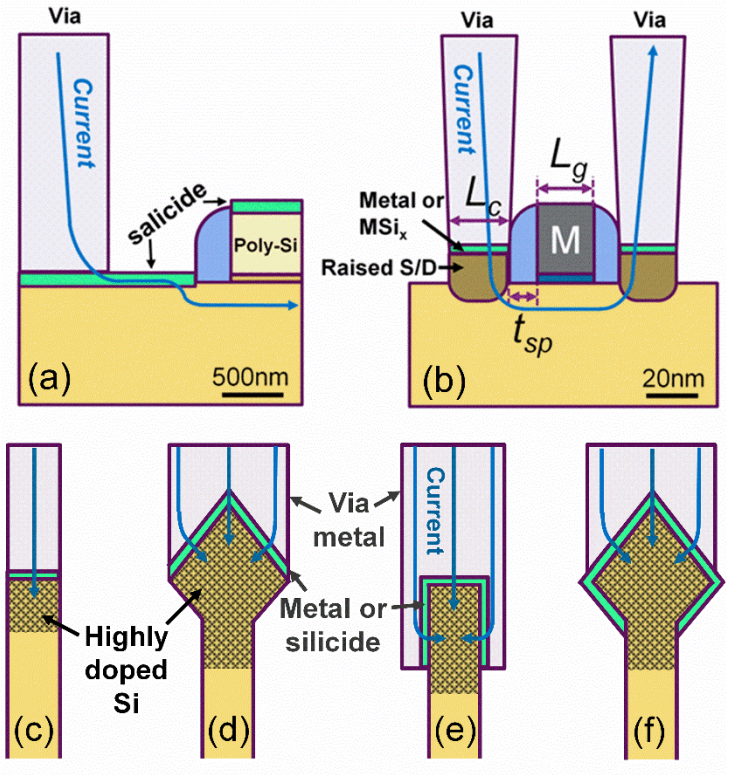

Fig. 1 Schematics of (a) Salicide contacts in traditional transistors [1] and (b) liner contacts in advanced transistors (e.g. 14 nm CMOS technology nodes [8]). Schematics of S/D contact schemes for FinFET: (c) Metal landing on fin, (d) metal landing on raised S/D, (e) metal wrapping around S/D, and (f) metal wrapping around raised S/D.

also challenge measurement accuracy of test structures. We could use the following simple calculation to illustrate quantitatively the importance of an ultralow ρ_c in the R_c control. The relationship between R_c and ρ_c at a simple S/D (like Fig. 1c) is expressed by [13]

$$R_c = \frac{\rho_c}{W_c L_t} \coth\left(\frac{L_c}{L_t}\right) \tag{1}$$

where the W_c is the contact width, the R_s is the sheet resistance of the highly doped semiconductor (namely highly doped drain, HDD, in CMOS transistors), and the L_t is the transfer length calculated by

$$L_t = \sqrt{\frac{\rho_c}{R_s}} \tag{2}$$

When an ultralow L_c of 10-20 nm is dictated by CMOS downscaling, a low R_c with the expression (1) demands both ultralow ρ_c and small L_t. A small L_t is important, because R_c would skyrocket when $L_t > L_c$. In the expression of L_t in (2), the R_s term cannot vary much, as its value is specified with the S/D shape and dopant activation at S/D which are not easily changed. Therefore, a small L_t again relies on an ultralow ρ_c; and this further increases the R_c dependence on the ρ_c. In addition, as small dimensions of a L_c challenge harshly lithography and etching

precisions, L_c errors are increasingly problematic in advanced transistors [14]; an ultralow ρ_c is thus also important to suppress L_c errors induced transistor performance variations.

In short, experimental investigations of ultralow-ρ_c contact solutions are demanded by advanced CMOS technology. This snapshot review is based on our previous ρ_c investigations, which have been summarized in the thesis [15]. In this review, we introduce investigations of ultralow ρ_c on Si CMOS relevant substrates—n-Si and p-SiGe. In the 2nd section, we construct ρ_c test structures with high sensitivity and accuracy; in the 3rd section, we evaluate a metal-insulator-semiconductor (MIS) contact scheme on n-Si; in the 4th section, we demonstrate pre-contact amorphization implantation based Ti alloy contacts with ultralow ρ_c on n-Si and p-SiGe that beat the 2×10^{-9} Ω·cm^2 target; in the 5th section, we briefly discuss n^+-Ge and n^+-InGaAs ρ_c investigations; in the 6th section, we will conclude this review and propose remaining topics that require further efforts in future.

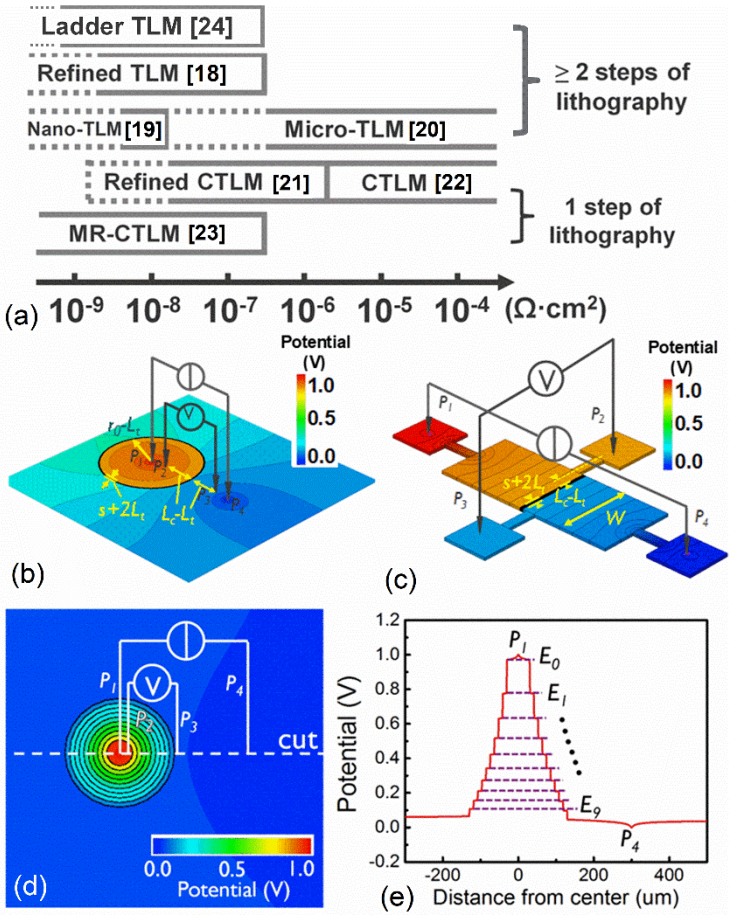

Fig. 2 (a) Comparison of ρ_c accuracy among various TLM test structures [18]–[25]. Accuracy of different TLMs is estimated based on effectiveness of metal resistance correction, fabrication complexity, and sampling capacity. If not corrected, potential dropped over metal resistances cause significant ρ_c extraction inaccuracy for TLMs. TCAD simulated potential drop on metal electrodes are compared between (b) CTLM, (C) refined TLM, and (d) MR-CTLM structures [26]. Potential profile along the "cut" in (d) is shown in (e), featuring equipotential metal rings in MR-CTLM. Simulation conditions: $\rho_c = 1\times10^{-8}$ Ω·cm^2, $R_s = 100$ Ω/sq, and metal sheet resistance $R_{sm} = 0.2$ Ω/sq.

2. Accurate Contact Resistivity Measurement

The latest advanced 7 nm and 5nm CMOS technology demands ρ_c as low as 2×10^{-9} Ω·cm^2 [16], [17]. Novel contact solutions are required to accomplish such low ρ_c. Before that, accurate ρ_c measurement is essential for correct evaluation. Accurate ρ_c extraction from a test device requires careful precluding impacts of the parasitic series resistance—including metal electrode resistances—and device dimension errors. A family of ρ_c test structures named transmission line models (TLM), as summarized in Fig. 2e, have been widely applied in ρ_c measurement because of their simple structures and simple ρ_c extraction principles: The simple fabrication reduces processes induced dimension errors; the simple ρ_c extraction principle makes parasitic factors transparent and easy to correct. As shown in Fig. 2a, among various TLM structures [18]–[24], the group of circular TLM (CTLM) and multiring CTLM (MR-CTLM) structures benefits from particularly simple fabrication that requires (A) only one step of lithography. The MR-CTLM further features (B) a high contact area sampling capacity and (C) effective suppression of the metal resistance impact (Fig. 2d and Fig. 2e). The features (A, B, C) make MR-CTLM stand out in ρ_c accuracy compared to other frequently applied TLM structures, like the CTLM (Fig. 2b) and the refined TLM (Fig. 2e).

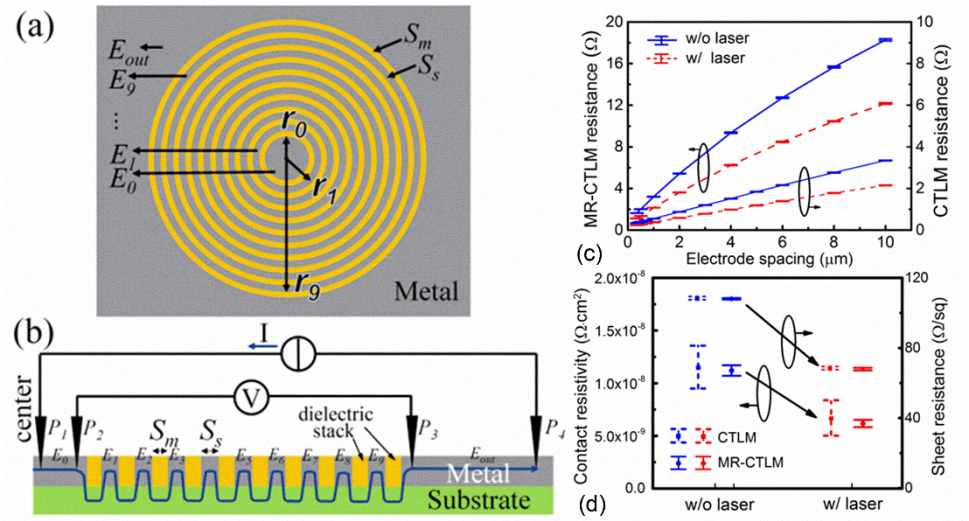

Fig. 3 Schematic (a) top view and (b) cross-section view of MR-CTLM [26]. Exemplary (c) curve-fitting and (d) ρ_c and R_s extraction using MR-CTLM [26] and CTLM [21] measurement resistances based on Ti/Si:P contacts. The Si:P with and without laser anneal have a carrier concentration of 2.7 × 10^{20} cm^{-3} and 4.6 × 10^{20} cm^{-3} respectively. Ultralow ρ_c of (6.17 ± 0.35) × 10^{-9} Ω·cm^2 and (1.12 ± 0.05) × 10^{-8} Ω·cm^2 were extracted with MR-CTLM for Ti/Si:P contacts with and without laser activation anneal of the Si:P [26].

One key in improving ρ_c accuracy of TLM structures is reduction of the parasitic metal resistance impacts. This requires not only reduction of the sheet resistance of the metal but also reduction of the effective metal electrode length in TLM structures. In the TLM families, the MR-CTLM [26], the refined TLM [18] and the laddar TLM [24] have effectively reduced metal electrode lengths and thus own high ρ_c accuracy. As shown in the schematic Fig. 3b, in a MR-CTLM structure, each ring of CTLM has a very small effective metal length of S_S (10 μm in [26]). Combined with a small metal sheet resistance of <100 mΩ/sq, the MR-CTLM provides high sensitivity and resolution for ρ_c exploration in the order of 10^{-9} Ω·cm^2—see Fig. 3c and Fig. 3d for instances. We

have thus used MR-CTLM extensively to evaluate contact solutions that target <2×10^{-9} $\Omega\cdot cm^2$ requirement by advanced CMOS technology nodes.

3. Metal-insulator-semiconductor (MIS) contacts vs metal-semiconductor (MS) contacts

There are two types of surface states that cause surface Fermi-level pinning for a semiconductor. One is the interfacial defects induced gap states (DIGS), including dangling bonds of surface Si atoms; the other is the metal induced gap states (MIGS) [27], [28], which are generated due to penetration of the tails of the electron waves from the metal into the band gap of a semiconductor [27], [29]. Inserting an insulator may passivate semiconductor surface states and help to achieve ultralow Schottky barrier height φ_b for a contact. Researchers have reported that by putting an ultrathin (~1 nm) insulator interlayer—such as TiO_2 [30], ZnO [31], Al_2O_3 [32], Si_3N_4 [33], Ge_3N_4 [34], MgO [35]—between the metal and the semiconductor and form a metal-insulator-semiconductor (MIS) contact, both DIGS and MIGS are passivated, and the semiconductor surface Fermi level is depinned. A low Schottky barrier height φ_{bn} for n-Si could thus be achieved by forming a MIS contact with a low-work function metal. MIS contacts attracted much attention for n-Si, because the surface Fermi-level pinning of Si leads to a commonly large φ_b for n-Si MS contacts. It was speculated a low φ_b would contribute to ultralow ρ_c in the 10^{-9} $\Omega\cdot cm^2$ range. To verify validity of this speculation, we have systematically evaluated the potentials of MIS contacts in terms of of both φ_b and ρ_c [36]–[38].

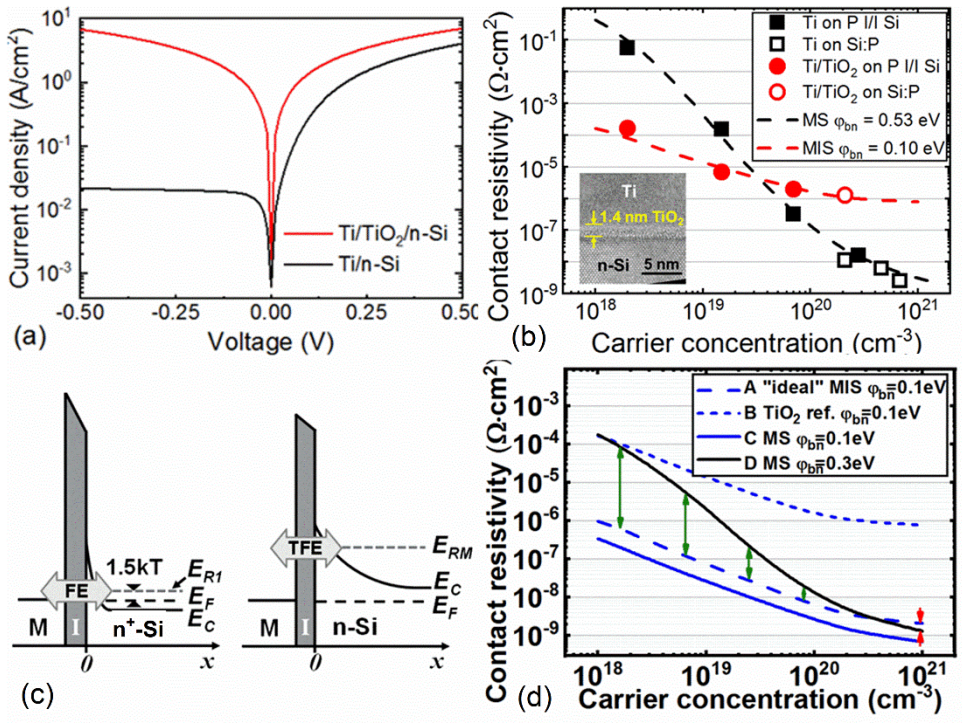

Fig. 4 Comparison of Ti/TiO_2/n-Si and Ti/n-Si contacts based on (a) room-temperature I-V curves measured with SBD, and (b) ρ_c measured with (MR-)CTLM [36]. An XTEM image of Ti/TiO_2/n-Si contact is shown in the inset of (b). (c) Schematic band diagram of MIS contacts with highly and moderately doped n-Si, where electron transmission over contacts is based on field emission (FE) and thermionic-field emission (TFE), respectively. (d) Theoretical comparison of ρ_c of MIS vs MS contacts based on calculation method in [36].

To evaluate the potential of MIS contact, we fabricated Ti/TiO_2/n-Si MIS contacts and compared them to Ti/n-Si MS contacts (without silicidation). The comparison was carried out with Schottky barrier diodes on lowly doped n-Si substrates which have an electron concentration of 2×10^{14} cm^{-3} and with (MR-)CTLM devices on moderately and highly doped substrates which have electron concentrations of 2.0×10^{18}, 1.5×10^{19}, 7.0×10^{19}, 2.1×10^{20}, 2.8×10^{20}, 4.6×10^{20}, 6.8×10^{20} cm^{-3}. The TiO_2 is a promising insulator candidate for n-Si MIS contacts because of its low ΔE_c with silicon [39].

In Fig. 4a, the current-voltage (I-V) characteristics of SBD of the Ti/TiO_2/n-Si MIS contact show an ohmic behavior, while the Ti/n-Si MS contact shows a typical rectifying behavior. The φ_{bn} of the MIS and the MS contacts are 0.12 eV and 0.47 eV, respectively, extracted with a low-temperature capacitance-voltage (C-V) measurement of the SBD samples [40]. From the SBD samples, we confirm the effective φ_{bn} reduction by inserting a TiO_2 interlayer between the Ti and the n-Si. However, we find that the low φ_{bn} does not lead to a low ρ_c on the highly doped n^+-Si. As shown in Fig. 4b for relatively lowly doped n-Si with n of 2.0×10^{18} and 1.5×10^{19} cm^{-3}, the ρ_c of Ti/TiO_2/n-Si is lower than that of Ti/n-Si; however, when n is higher than 5×10^{19} cm^{-3}, the Ti/n-Si outperforms the Ti/TiO_2/n-Si.

We have performed theoretical calculation of ρ_c of MIS vs MS contacts in [36] and understood that the ρ_c of an MIS contact is increased due to reduced tunneling probability of electrons through the insulator interlayer. The schematics in Fig. 4c help illustrate electron transmission over MIS contacts on moderately and highly doped n-Si. The lowering of φ_b and the hindering of electron tunneling by an insulator make two opposite impacts on electron transmission over a MIS contact. Under the thermionic emission related regimes on lowly and moderately doped n-Si, the former advantage of MIS contacts is more dominant and thus contributes to improved SBD current and ρ_c; under the field emission dominated regime on highly doped n^+-Si, the latter disadvantage gets pronounced and thus compromises ρ_c.

Admittedly, the TiO_2 may not be a perfect insulator to achieve low ρ_c of an MIS contact. In Fig. 4d, we assign optimal parameters to an imaginary ideal MIS contact (A) and compared it to ideal MS contacts (C) and (D) [36]. Even an ideal MIS contact would lose its edge in the high doping range above 3×10^{20} cm^{-3}—the relevant doping level for the source/drain of advanced Si nMOSFETs. Besides a compromised carrier tunneling probability, MIS contacts have another major concern about its thermal stability. MIS contacts for n-Si require a low work function metal—such as Al, Ti, Mg—to approach a low $q\varphi_b$. However, the low-work function metals are typically reactive and they are thus difficult to preserve a stable interface with a ~1 nm thin insulator of an MIS contact. Thermal degradation of MIS contacts has been reported experimentally below 400ºC [37] or even during metal depositions [37], [41]. This makes MIS contacts hardly possible to survive several 400-450°C heating steps in the CMOS back-end-of-line (BEOL) manufacturing. Therefore, we focus on developing MS contacts in the next section to meet the 10^{-9} $\Omega\cdot cm^2$ ρ_c requirement of the advanced CMOS technology.

4. Advanced Ti (germano-)silicide contacts for both n-Si and p-SiGe

It cannot be overstressed that the Schottky barrier height is no longer a dominant parameter behind the ρ_c when the active doping concentration is beyond 3×10^{20} cm^{-3}. On Si:P substrates with an active donor of 7×10^{20} cm^{-3} [42], we have demonstrated that the Ti silicides with φ_{bn} of ~0.5 eV have nearly one order lower ρ_c than the La silicides counterpart with φ_{bn} as low as ~0.3 eV [43]. This is because tunneling based carrier transmissions

dominate MS interface conduction on highly doped semiconductors; here the theoretical dominant factors behind the ρ_c become the active doping concentration of a semiconductor and the effective mass and the Fermi energy of a contact metal [44]. In realistic implementation of MS contacts in advanced CMOS transistors, we shall also consider several practical factors, including impurity scavenging capability of the metal, diffusion rates of the metal in a semiconductor, MS interface morphology and stability, dopant redistribution after MS reaction, and available metal deposition methods [15]. In this overview picture, Ti and its (germano-)silicides make excellent candidates for source/drain contacts of both NMOS and PMOSFETs. A summary of research and development of advanced Ti (germano-)silicide refers to [15], [45], [46].

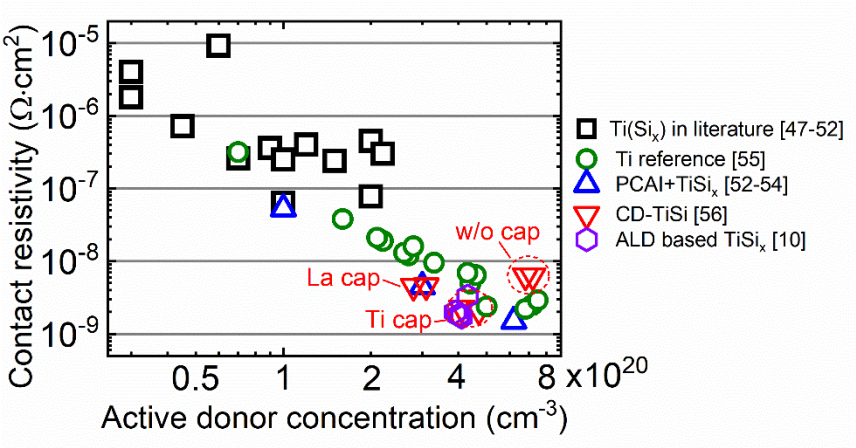

Fig. 5 Benchmark of ρ_c of $TiSi_x$ on n^+-Si. Only those ρ_c reported together with specific active donor concentration of n^+-Si in literature are included in this figure.

High dopant activation and (germano-)silicidation methods are the key to ultralow ρ_c, which is clear from the ρ_c benchmark collected for Ti and $TiSi_x$ [10], [47]–[56] in Fig. 5. In the following sub-sections, we will introduce three (germano-)silicidation methods: the first one is based on pre-contact amorphization implantation (PCAI) [53], [54], [57], the second on Ti/Si co-deposition (CD-TiSi) [56], [58], the third on atomic layer deposited Ti [10]. All three methods feature low-thermal budget, work for both n^+-Si and p^+-SiGe, and help approach the ρ_c of 2×10^{-9} $\Omega\cdot cm^2$ 5/7 nm CMOS technology target; the three methods have sequentially increasing compatibility to advanced 3D CMOS transistors.

(I) Pre-contact amorphization implantation based $TiSi_x(Ge_y)$

A schematic process flow utilizing the PCAI technique is illustrated in Fig. 6. The PCAI induced ρ_c improvement is demonstrated in Fig. 7a and Fig. 7b. XTEM images of the $TiSi_x(Ge_y)$ before and after post-metal annealing (PMA) are shown in Fig. 7c-f. The PCAI could improve $TiSi_x$ nucleation and crystallinity [59]. Moreover, the PCAI creates Si interstitial point defects near the Si surface, which compensate the vacancy defects induced by Ti silicidation [60]. Both improvement may have contributed to the ultralow ρ_c of $TiSi_x(Ge_y)$ on both highly doped Si:P and SiGe:B. We have systematically screened the PCAI and post-metal anneal (PMA) conditions for $TiSi_x(Ge_y)$ [53], [58]. Note that there is a common process window that results in ultralow ρ_c for both n-type and p-type substrates in Fig. 6c and Fig. 6d: optimal (germano-)silicidation is achieved by 3keV

6×10^{14} cm^{-2} Ge PCAI and around 500°C 1min PMA in N_2. The mild amorphization by the low-energy low-dose PCAI and the low thermal-budget PMA are relatively compatible to the 3D transistors.

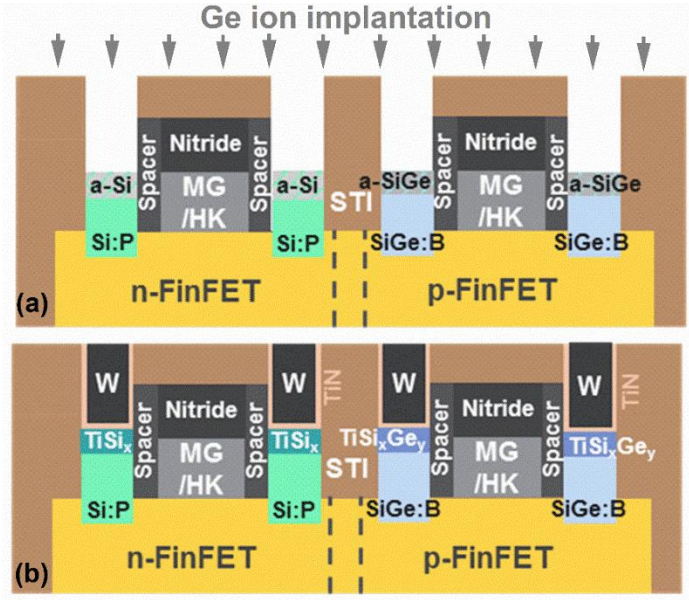

Fig. 6 PCAI based contact formation for both NMOS and PMOS: (a) PCAI with 3keV 6×10^{14} cm^{-2} Ge I/I after contact opening; followed by (b) Ti/TiN deposition, 500°C 1min N_2 PMA, W CVD, and W CMP.

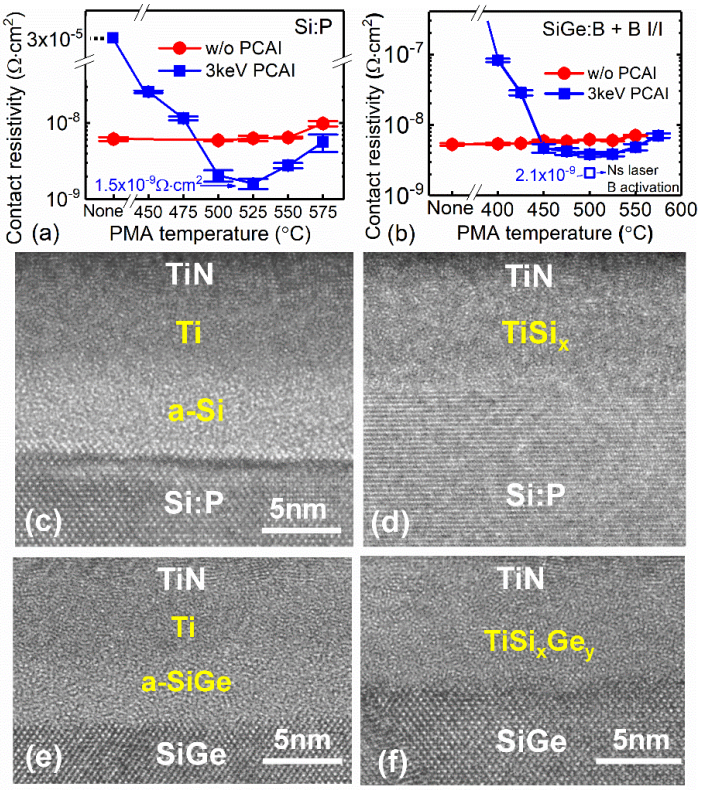

Fig. 7 ρ_c of (a) $TiSi_x$/Si:P and (b) $TiSi_xGe_y$/SiGe:B with and without PCAI; ρ_c were evaluated with MR-CTLM. XTEM of (c,d) $TiSi_x$/Si:P and (e,f) $TiSi_xGe_y$/SiGe:B that received 6 keV 6×10^{14} cm^{-2} Ge PCAI (c,e) before and (d,f) after 1 min N_2 PMA [22], [24]. Sample in (c) received 550°C PMA [22] while sample in d) received 500°C PMA [24].

Note that the low-ρ_c phases of $TiSi_x(Ge_y)$ in Fig. 7d and Fig. 7f are different with traditional low-resistivity fully-crystalline $TiSi_2$. The low-ρ_c $TiSi_x(Ge_y)$ formed with relatively low-temperature ($\leq$550°C) thermal annealing is in an amorphous phase with embedded $TiSi_x(Ge_y)$ crystallites—the crystallites could be detected by X-ray diffraction [53]; the $TiSi_x(Ge_y)$ in such low-ρ_c phases usually maintain a smooth interface with n-Si or p-SiGe. This differs with fully-crystalline $TiSi_2$ formed after $\geq$800°C annealing which usually has a rough interface with Si; formation of $TiSi_2$ and degradation of MS morphology lead to significant ρ_c degradation [47], [53]—such ρ_c degradation is already observed in Fig. 7a and Fig. 7b with near 600°C PMA.

(II) TiSi Co-deposition Based $TiSi_x$

The phase of low-ρ_c $TiSi_x$ can also be achieved by a TiSi co-deposition (CD-TiSi) technique. Like the PCAI based $TiSi_x$, the amorphous Ti and Si mixture in as-deposited CD-TiSi also enhances $TiSi_x$ crystallite formation [61]. The CD-TiSi has three advantages over the PCAI based one: it prevents Si substrate consumption; it avoids potential ion implantation induced damages; and it is flexible to modulate a composition ratio between the amorphous Si and the Ti [62]. But due to a low oxygen solubility in the CD-TiSi, oxide residues may segregate at the CD-TiSi/semiconductor interface and degrade ρ_c. The oxygen may origin from the TiSi deposition process or from an oxide residue on semiconductor surfaces. Solutions to the oxide interlayer may include an additional oxygen scavenging cap layer on top of the CD-TiSi [56].

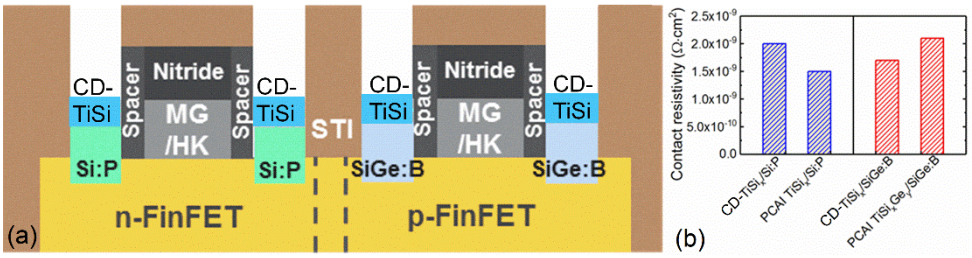

Fig. 8 (a) Co-deposition of TiSi for both NMOS and PMOS contacts followed by 450~500°C PMA. (b) Ultralow ρ_c achieved by CD-$TiSi_x$ on Si:P and SiGe:B [56], [58] compared to the PCAI based $TiSi_x(Ge_y)$ [53], [58]; ρ_c evaluated with MR-CTLM.

A schematic of TiSi co-deposition based silicidation technique is shown in Fig. 8. The CD-TiSi can be accomplished by laminated physical vapor deposition (PVD) of Ti and Si monolayers in cycles. As shown in Fig. 8, the CD-TiSi also achieves ρ_c as low as those achieved by the PCAI based $TiSi_x(Ge_y)$. We have also observed that CD-TiSi forms a similar phase of $TiSi_x$ (not shown) [56], [58] to the PCAI based one in Fig. 7d and Fig. 7f .

(III) Conformal Ti or $TiSi_x$

The PCAI and CD-$TiSi_x$ based $TiSi_x(Ge_y)$ have shown several advantages including ultralow ρ_c. However, those metal PVD based methods get increasingly incompatible to source/drain formation on a FinFET due to a shrinking contact opening area. Besides, there is increasing interests in forming a wrap-around contact (WAC) on a raised source/drain to maximize the contact area, which requires conformal metal deposition. In this regard, like in the schematics of Fig. 1e and Fig. 1f, conformal Ti or $TiSi_x$ by chemical vapor deposition (CVD) or atomic layer deposition (ALD), appeals to the modern transistors.

The CVD or ALD Ti or $TiSi_x$ techniques are difficult because Ti has very negative electrochemical potentials. Only recently have ALD or CVD Ti based wrap-around contacts (WAC) on fins been reported [10], [11]. In our demonstration, the Ti/TiN ALD was performed on both MR-CTLM and Fin-TLM using an experimental, showerhead based chamber on a TEL Triase$^+$ platform^{TM} [10]. The Ti ALD process was slowly conducted at 430°C, which provides sufficient thermal heating for *in situ* Ti (germano-)silicidation during the ALD. In Fig. 9a and Fig. 9b, the ALD Ti can approach ultralow ρ_c around 2×10^{-9} $\Omega\cdot cm^2$ after mild (germano-)silicidation; unlike the PVD Ti in Fig. 7, the PCAI treatment is unnecessary to achieve such low ρ_c. In the XTEM images and energy-dispersive X-ray spectroscopy images in Fig. 9c, we not only observe an increased contact area with WAC but *in-situ* silicidation without intentional PMA [10].

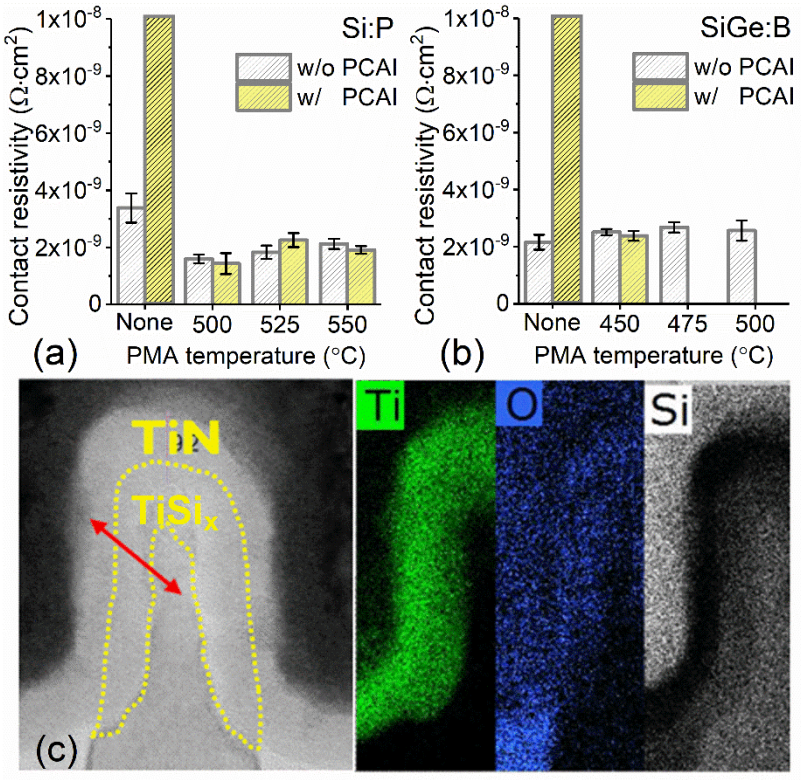

Fig. 9 ρ_c of ALD Ti on (a) Si:P and (b) SiGe:B with and without PCAI; ρ_c was evaluated with MR-CTLM [10]. (c) XTEM image and energy-dispersive X-ray spectroscopy for a WAC on Si fin after Ti/TiN ALD and W CVD without intentional PMA [10].

5. Contact challenges for Ge and InGaAs NMOS

Since electrons have higher mobility in Ge and InGaAs than in Si, Ge and InGaAs were considered potential channel material candidates for advanced NMOS transistors. However, the high R_c together with challenging gate oxide passivation remain major bottlenecks that prevent replacement of Si NMOS with Ge and InGaAs candidates. The high R_c of n^+-Ge and n^+-InGaAs are caused by insufficient donor activation and/or thermally unstable donor super-activation.

Limited donor activation and fast donor diffusion in Ge are caused by donor-vacancy pairing and clustering [63]. Typical active donor concentration in heavily doped n^+-Ge after rapid thermal annealing activation is limited

at 2~5×10^{19} cm^{-3}. This leads to relatively high ρ_c of n^+-Ge under the thermionic-field emission regime. It is encouraging that short-pulse laser anneal activation helps break the donor-vacancy bond and achieve super-activation of donors in Ge while limiting the donor diffusion [64]–[67]. As shown in the benchmark of Fig. 10a [15], [64]–[74], low ρ_c of n^+-Ge in the orders of 10^{-9} and 10^{-8} $\Omega \cdot cm^2$ have been achieved by laser based donor activation [64]–[67]. Making use of high P chemical doping up to 10^{20}~10^{21} cm^{-3} in Si:P, a Si:P interlayer based metal/Si:P/n^+-Ge contact scheme has been demonstrated for n^+-Ge contact [67], [74], [75]. Further, van Dal *et al.* combine the metal/Si:P/n^+-Ge contact with laser anneal donor activation and achieve record-low ρ_c of n^+-Ge of ~1.6×10^{-9} $\Omega \cdot cm^2$ [67]. However, laser anneal based superactivated donors are prone to deactivation after 300~500°C heating [15], [76], [77]. This implies that the low ρ_c of Ge NMOS achieved by laser super-activation could hardly maintain after BEOL processing, where several steps are performed at near 400°C. Therefore, donor super-activation and prevention of donor deactivation are currently major challenges for low R_c of Ge NMOS.

As for n^+-InGaAs contacts, low donor activation is a major challenge to achieve low R_c. As reviewed by Lind *et al.* [78], the highest reported active donor concentration in n^+-$In_{0.53}Ga_{0.47}As$ is merely ~5×10^{19} cm^{-3}. In investigations of n^+-InGaAs contacts in Fig. 10b [79], we observe that the ρ_c of n^+-InGaAs contacts are not sensitive to contact metal species and are favored by a very low φ_{bn}. These observations are aligned with the InGaAs (001) surface Fermi level pinning effect in the conduction band [80]. As indicated in Fig. 10b by extrapolation, the donor activation level for n^+-InGaAs must be boosted far above 10^{20} cm^{-3} to meet the 2×10^{-9} $\Omega \cdot cm^2$ target for advanced NMOS applications. Effective super-activation methods for donors in InGaAs are wanted.

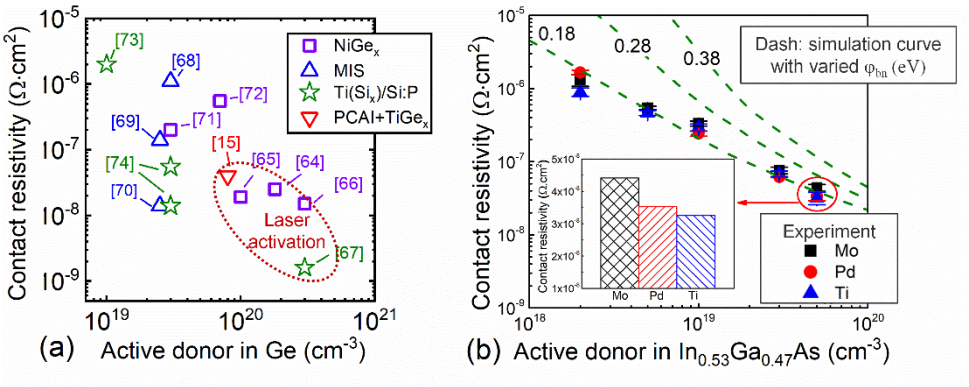

Fig. 10 (a) Benchmark of ρ_c of n^+-Ge contacts [15], [64]–[74]. (b) Comparison of ρ_c of n^+-InGaAs contacts with varied active donor concentration achieved by in-situ Si, S, or Se doping [79].

6. Conclusions and outlook

We have established accurate ρ_c test structures with a simple fabrication scheme to facilitate efficient and systematic experimental investigations on ρ_c. By putting 10 CTLMs in series, we develop a multiring CTLM (MR-CTLM) method to improve the sampling capacity and suppress the parasitic metal resistance impact on ρ_c extraction.

We have evaluated the MIS contact scheme for n-Si but found two limitations to its realistic applications. One limitation is the insulator reduced carrier transmission, which prevents the MIS contacts from meeting the

10^{-9} Ω·cm^2 ρ_c target; the other limitation is the low thermal stability of the MIS contacts, which cannot withstand a standard BEOL thermal budget of CMOS manufacturing.

We evaluate and optimize ρ_c of Ti alloy contacts on n^+-Si and p^+-SiGe. By applying three Ti (germano-) silicidation techniques, we demonstrate Ti alloys with ultralow ρ_c of (1-3)×10^{-9} Ω·cm^2 on both substrates, which meet the ρ_c target of 7 nm/5 nm CMOS technology nodes. The first (germano-)silicidation technique is based on pre-contact amorphization implantation, the second on Ti/Si co-deposition, and the third on atomic layer deposited Ti. An *in-situ* anneal or post-metal anneal at around 450-550^{o}C helps $TiSi_x(Ge_y)$ approach a low-ρ_c phase. The low-ρ_c $TiSi_x(Ge_y)$ is at an amorphous state but embedded with small crystallites.

We briefly summarize the status of n^+-Ge and n^+-InGaAs contact investigations. Donor activation and prevention of donor deactivation remain challenging for those two NMOS candidates. For n^+-Ge, thermal stability of super-activated donors requires improvement. For n^+-InGaAs, effective donor activation methods are wanted to boost the active donor concentration above 10^{20} cm^{-3}.

Based on the contact exploration for advanced CMOS technology in this review, we suggest that the following topics require further investigations in future:

1. Apart from Ti alloys, contact metal candidates should be experimentally evaluated with respect to ρ_c and thermal stability. Such a broad screening of contact metals is of high significance, but is still lacking, especially on highly doped substrates;
2. Prevention of donor deactivation from thermal heating in BEOL steps is important for n^+-Si substrates [81], because donor deactivation causes a directly increase of ρ_c and R_c;
3. Ga is an attractive acceptor candidate for S/D doping of group-IV PMOS transistors because of high Ga activation in high-Ge content SiGe [82], [83];
4. Besides accurate ρ_c measurement on planar devices, all contact schemes should be reevaluated on 3D nanoscale devices to test their compatibility;
5. As the next generation of integrated circuits (IC) may feature 3D sequential integration [7], there are two types of contacts that would be required in such IC: contacts with low formation thermal budget and low ρ_c for top-tier devices, and contacts with high thermal stability and low ρ_c for the bottom-tier devices. These two types of contacts require further exploration;
6. Finally, the interface resistivity between the via metal and the silicide has rarely been studied. But this interface resistivity may become significant when ρ_c enters the order of 10^{-10} Ω·cm^2.

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References

[1] H. P. Wong, S. Member, D. J. Frank, P. M. Solomon, C. H. J. Wann, and J. J. Welser, "Nanoscale CMOS," *Proceedings of the IEEE*, vol. 87, no. 4, pp. 537–570, 1999.

[2] S. Thompson, "Tutorial IEDM 2015 : Advance Device Concepts for 7nm Node and Beyond," 2015.

[3] B. B. Doris, "Front end of line integration issues and opportunities beyond 7nm node," in *Short course of IEEE International Electron Devices Meeting*, 2015.

[4] T. Shibata, K. Hieda, M. Sato, M. Konaka, R. L. M. Dang, and H. Iizuka, "An optimally designed process for submicron mosfets," in *IEDM Tech Dig.*, 1981, pp. 647–650.

[5] S. Natarajan *et al.*, "A 14nm Logic Technology Featuring 2 nd -Generation FinFET Interconnects , Self-Aligned Double Patterning and a 0 . 0588 m 2 SRAM cell size," *IEDM, IEEE Technical Digest - International Electron Devices Meeting*, pp. 3.7.1-3.7.3, 2014, doi: 10.1109/IEDM.2014.7046976.

[6] C. Lavoie *et al.*, "Contacts in advanced CMOS: History and emerging challenges," *ECS Trans*, vol. 77, no. 5, pp. 59–79, 2017, doi: 10.1149/07705.0059ecst.

[7] G. Yeric, "Moore ' s Law at 50 : Are we planning for retirement ?," *IEDM Tech. Dig.*, pp. 1–8, 2015.

[8] S. Natarajan *et al.*, "A 14nm Logic Technology Featuring 2 nd -Generation FinFET Interconnects , Self-Aligned Double Patterning and a 0 . 0588 m 2 SRAM cell size," *IEDM, IEEE Technical Digest - International Electron Devices Meeting*, pp. 3.7.1-3.7.3, 2014, doi: 10.1109/IEDM.2014.7046976.

[9] C. W. Sohn *et al.*, "Analytic model of S/D series resistance in trigate FinFETs with polygonal epitaxy," *IEEE Trans Electron Devices*, vol. 60, no. 4, pp. 1302–1309, 2013, doi: 10.1109/TED.2013.2246790.

[10] S. A. Chew *et al.*, "Ultralow resistive wrap around contact to scaled FinFET devices by using ALD-Ti contact metal," *IITC 2017 - 2017 IEEE International Interconnect Technology Conference*, pp. 5–7, 2017, doi: 10.1109/IITC-AMC.2017.7968969.

[11] N. Breil *et al.*, "Highly-selective superconformal CVD Ti silicide process enabling area-enhanced contacts for next-generation CMOS architectures," in *Digest of Technical Papers - Symposium on VLSI Technology*, 2017, pp. T216-217.

[12] C. N. Ni *et al.*, "Ultra-low NMOS contact resistivity using a novel plasma-based DSS implant and laser anneal for post 7 nm nodes," *Digest of Technical Papers - Symposium on VLSI Technology*, pp. 70–71, 2016, doi: 10.1109/VLSIT.2016.7573383.

[13] D. K. Schroder, *MATERIAL AND DEVICE SEMICONDUCTOR MATERIAL AND DEVICE Third Edition*, 3rd ed., vol. 44, no. 4. Hoboken, New Jersey: John Wiley & Sons, 2006. doi: 10.1063/1.2810086.

[14] C. Auth *et al.*, "A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," *Digest of Technical Papers - Symposium on VLSI Technology*, vol. m, no. 2003, pp. 131–132, 2012, doi: 10.1109/VLSIT.2012.6242496.

[15] H. Yu, "Advanced Metal Semiconductor Contacts for 14nm CMOS Technology and Beyond," Katholieke Universiteit Leuven, Leuven, 2019.

[16] C. Ni *et al.*, "Ultra-Low Contact Resistivity with Highly Doped Si : P Contact for nMOSFET," in *Symposium on VLSI Technology Digest of Technical Papers*, 2015, no. 2012, pp. T118-119.

[17] O. Gluschenkov *et al.*, "FinFET performance with Si:P and Ge:group-III-metal metastable contact trench alloys," *IEDM Tech Dig.*, pp. 448–451, 2016.

[18] R. Dormaier and S. E. Mohney, "Factors controlling the resistance of ohmic contacts to n-InGaAs factors controlling the resistance of ohmic contacts to n-InGaAs," *Journal of Vacuum Science & Technology B*, vol. 30, pp. 031209-1-031209–10, 2012, doi: 10.1116/1.4705730.

[19] W. Lu, A. Guo, A. Vardi, and J. A. Alamo, "A Test Structure to Characterize Nano-Scale Ohmic Contacts in III – V MOSFETs," *IEEE Electron Device Letters*, vol. 35, no. 2, pp. 178–180, 2014.

[20] H. H. Berger, "Contact resistance on diffused resistors," in *ISSCC*, 1969, pp. 160–161.

[21] H. Yu *et al.*, "A simplified method for (circular) transmission line model simulation and ultralow contact resistivity extraction," *IEEE Electron Device Letters*, vol. 35, no. 9, pp. 957–959, 2014.

[22] G. K. Reeves, "Specific contact resistance using a circular transmission line model," *Solid State Electron*, vol. 23, pp. 487–490, 1980.

[23] H. Yu *et al.*, "Multiring Circular Transmission Line Model for Ultralow Contact Resistivity Extraction," *Electron Device Letters, IEEE*, vol. 36, no. 6, pp. 600–602, 2015.

[24] Y. Wu, H. Xu, X. Gong, and Y. C. Yeo, "A Ladder Transmission Line Model for the Extraction of Ultralow Specific Contact Resistivity - Part I: Theoretical Design and Simulation Study," *IEEE Trans Electron Devices*, vol. 67, no. 7, pp. 2682–2689, Jul. 2020, doi: 10.1109/TED.2020.2992988.

[25] H. Yu *et al.*, "Process options to enable (sub-) 1e-9 Ohm.cm2 contact resistivity on Si devices," in *2016 IEEE International Interconnect Technology Conference/Advanced Metallization Conference (IITC/AMC)*, 2016, pp. 66–68.

[26] H. Yu *et al.*, "Multiring circular transmission line model for ultralow contact resistivity extraction," *IEEE Electron Device Letters*, vol. 36, no. 6, pp. 600–602, Jun. 2015, doi: 10.1109/LED.2015.2425792.

[27] J. Tersoff, "Schottky barrier heights and the continuum of gap states," *Phys Rev Lett*, vol. 52, no. 6, pp. 465–468, 1984, doi: 10.1103/PhysRevLett.52.465.

[28] W. Mönch, "Barrier heights of real Schottky contacts explained by metal-induced gap states and lateral inhomogeneities," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 17, no. 4, p. 1867, 1999, doi: 10.1116/1.590839.

[29] J. E. Rowe, S. B. Christman, and G. Margaritondo, "Metal-induced surface states during Schottkybarrier formation on Si, Ge, and GaAs," *Phys Rev Lett*, vol. 35, no. 21, pp. 1471–1475, 1975.

[30] J. Y. J. Lin, A. M. Roy, A. Nainani, Y. Sun, and K. C. Saraswat, "Increase in current density for metal contacts to n-germanium by inserting TiO2 interfacial layer to reduce Schottky barrier height," *Appl Phys Lett*, vol. 98, no. 9, pp. 092113-1-092113–3, 2011, doi: 10.1063/1.3562305.

[31] P. Paramahans Manik *et al.*, "Fermi-level unpinning and low resistivity in contacts to n-type Ge with a thin ZnO interfacial layer," *Appl Phys Lett*, vol. 101, no. 18, pp. 1–6, 2012, doi: 10.1063/1.4764909.

[32] T. Nishimura, K. Kita, and A. Toriumi, "A significant shift of schottky barrier heights at strongly pinned metal/germanium interface by inserting an ultra-thin insulating film," *Applied Physics Express*, vol. 1, no. 5, pp. 0514061–0514063, 2008, doi: 10.1143/APEX.1.051406.

[33] D. Connelly, C. Faulkner, P. A. Clifton, and D. E. Grupp, "Fermi-level depinning for low-barrier Schottky source/drain transistors," *Appl Phys Lett*, vol. 88, pp. 012105-1-012105–3, 2006, doi: 10.1063/1.2159096.

[34] R. R. Lieten, S. Degroote, M. Kuijk, and G. Borghs, "Ohmic contact formation on n-type Ge," *Appl Phys Lett*, vol. 92, no. 2, pp. 022106-1-022106–3, 2008, doi: 10.1063/1.2831918.

[35] Y. Zhou *et al.*, "Investigating the origin of Fermi level pinning in Ge Schottky junctions using epitaxially grown ultrathin MgO films," *Appl Phys Lett*, vol. 96, no. 10, pp. 102103-1-102103–3, 2010, doi: 10.1063/1.3357423.

[36] H. Yu *et al.*, "Contact resistivities of metal-insulator-semiconductor contacts and metal-semiconductor contacts," *Appl Phys Lett*, vol. 108, pp. 171602-1-171602–5, 2016.

[37] H. Yu *et al.*, "Thermal stability concern of metal-insulator-semiconductor contact: a case study of Ti/TiO2/n-Si contact," *IEEE Trans Electron Devices*, vol. 63, no. 7, pp. 2671–2676, Jul. 2016, doi: 10.1109/TED.2016.2565565.

[38] H. Yu *et al.*, "MIS or MS? Source/drain contact scheme evaluation for 7nm Si CMOS technology and beyond," *2016 16th International Workshop on Junction Technology (IWJT)*, pp. 19–24, 2016, doi: 10.1109/IWJT.2016.7486665.

[39] J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 18, no. 3, p. 1785, 2000, doi: 10.1116/1.591472.

[40] R. R. Lieten, V. V. Afanas'ev, N. H. Thoan, S. Degroote, W. Walukiewicz, and G. Borghs, "Mechanisms of Schottky barrier control on n-type germanium using Ge3N4 interlayers," *J Electrochem Soc*, vol. 158, no. 4, p. H358, 2011, doi: 10.1149/1.3545703.

[41] H. Yu, Q. Xie, Y. L. Jiang, D. Deduytsche, and C. Detavernier, "Fermi level depinning failure for Al/GeO2/Ge contacts," *ECS Solid State Letters*, vol. 1, no. 5, 2012, doi: 10.1149/2.004206ssl.

[42] E. Rosseel *et al.*, "Selective epitaxial growth of high-P Si:P for source/drain formation in advanced Si nFETs," *ECS Trans*, vol. 75, no. 8, pp. 347–359, 2016, doi: 10.1149/07508.0347ecst.

[43] H. Yu *et al.*, "Lanthanum and lanthanum silicide contacts on N-type silicon," *IEEE Electron Device Letters*, vol. 38, no. 7, pp. 843–846, Jul. 2017, doi: 10.1109/LED.2017.2700233.

[44] A. Dabral *et al.*, "Study of the intrinsic limitations of the contact resistance of metal/semiconductor interfaces through atomistic simulations," *ECS Journal of Solid State Science and Technology*, vol. 7, no. 6, pp. 73–80, 2018, doi: 10.1149/2.0041806jss.

[45] H. Yu *et al.*, "Titanium (germano-)silicides featuring 10-9 Ω·cm2 contact resistivity and improved compatibility to advanced CMOS technology," in *18th International Workshop on Junction Technology (IWJT)*, 2018, pp. 9–13.

[46] S. Mao and J. Luo, "Titanium-based ohmic contacts in advanced CMOS technology," *Journal of Physics D: Applied Physics*, vol. 52, no. 50. Institute of Physics Publishing, Sep. 17, 2019. doi: 10.1088/1361-6463/ab3dc9.

[47] S. Zaima, T. Yamauchi, Y. Koide, and Y. Yasuda, "Study on determining factors of low contact resistivity in transition metal-silicon systems," *Appl Surf Sci*, vol. 70–71, pp. 624–628, 1993, doi: 10.1016/0169-4332(93)90591-X.

[48] H. R. Liauh, M. C. Chen, J. F. Chen, and L. J. Chen, "Electrical and microstructural characteristics of Ti contacts on (001)Si," *J Appl Phys*, vol. 74, no. 4, pp. 2590–2597, 1993, doi: 10.1063/1.354672.

[49] J. Hui, S. Wong, and J. Moll, “Specific contact resistivity of TiSi2 to p+ and n+ junctions,” *IEEE Electron Device Letters*, vol. 6, no. 9, pp. 479–481, 1985, doi: 10.1109/EDL.1985.26199.

[50] Y. Taur *et al.*, “Source-drain contact resistance in CMOS with self-aligned TiSi2,” *IEEE Trans Electron Devices*, vol. 34, no. 3, pp. 575–580, 1987.

[51] Y.-C. S. Yu and V. F. Drobny, “Optimization of TiSi2/n+-polysilicon process for applications to polysilicon emitter bipolar integrated circuits,” *Journal of electrochemical society*, vol. 136, no. 7, pp. 2076–2082, 1989.

[52] S. Mao *et al.*, “Impact of Ge Preamorphization Implantation on Both the Formation of Ultrathin TiSix and the Specific Contact Resistivity in TiSix/n-Si Contacts,” *IEEE Trans Electron Devices*, vol. 65, no. 10, pp. 4490–4498, Oct. 2018, doi: 10.1109/TED.2018.2864558.

[53] H. Yu *et al.*, “Titanium silicide on Si:P with pre-contact amorphization implantation treatment: contact resistivity approaching 1×10-9 Ohm-cm2,” *IEEE Trans Electron Devices*, vol. 63, no. 12, pp. 4632–4641, 2016, doi: 10.1109/TED.2016.2616587.

[54] H. Yu *et al.*, “1.5×10-9 Ω·cm2 contact resistivity on highly doped Si:P using Ge pre-amorphization and Ti silicidation,” in *Proc. 2015 IEEE Int. Electron Devices Meeting (IEDM)*, 2015, pp. 592–595.

[55] E. Rosseel *et al.*, “Contact Resistivity of Highly Doped Si:P, Si:As, and Si:P:As Epi Layers for Source/Drain Epitaxy,” *ECS Trans*, vol. 98, no. 5, pp. 37–42, Sep. 2020, doi: 10.1149/09805.0037ecst.

[56] H. Yu *et al.*, “Oxygen Gettering Cap to Scavenge Parasitic Oxide Interlayer in TiSi Contacts,” *IEEE Electron Device Letters*, vol. 40, no. 11, pp. 1712–1715, Nov. 2019, doi: 10.1109/LED.2019.2940819.

[57] H. Yu *et al.*, “Ultralow-resistivity CMOS contact scheme with pre-contact amorphization plus Ti (germano-)silicidation,” *Digest of Technical Papers - Symposium on VLSI Technology*, pp. 66–67, 2016, doi: 10.1109/VLSIT.2016.7573381.

[58] H. Yu *et al.*, “TiSi(Ge) contacts formed at low temperature achieving around 2×10-9 Ohm-cm2 contact resistivities to p-SiGe,” *IEEE Trans Electron Devices*, vol. 64, no. 2, pp. 500–506, 2017, doi: 10.1109/TED.2016.2642888.

[59] Q. Xu and C. Hu, “New Ti-SALICIDE process using Sb and Ge preamorphization for sub-0.2 ??m CMOS technology,” *IEEE Trans Electron Devices*, vol. 45, no. 9, pp. 2002–2009, 1998, doi: 10.1109/16.711367.

[60] D. S. Wen, P. L. Smith, C. M. Osburn, and G. A. Rozgonyi, “Defect annihilation in shallow p+ junctions using titanium silicide,” *Appl Phys Lett*, vol. 51, no. 15, pp. 1182–1184, 1987, doi: 10.1063/1.98726.

[61] I. J. M. M. Raaijmakers, A. H. Reader, and P. H. Oosting, “The formation of an amorphous silicide by thermal reaction of sputter-deposited Ti and Si layers,” *J Appl Phys*, vol. 63, no. 8, pp. 2790–2795, 1988, doi: 10.1063/1.340979.

[62] A. Quintero, M. Libera, C. Cabral, C. Lavoie, and J. M. E. Harper, “Two-step codeposition process for enhanced C54-TiSi2 formation in the Ti-Si binary system,” *J Appl Phys*, vol. 89, no. 9, pp. 4879–4885, 2001, doi: 10.1063/1.1360698.

[63] H. Bracht, “Defect engineering in germanium,” *Physica Status Solidi (A) Applications and Materials Science*, vol. 211, no. 1, pp. 109–117, 2014, doi: 10.1002/pssa.201300151.

[64] W. Hsu *et al.*, “Laser spike annealing for shallow junctions in Ge CMOS,” *IEEE Trans Electron Devices*, vol. 64, no. 2, pp. 346–352, 2017.

[65] H. Miyoshi, T. Ueno, K. Akiyama, Y. Hirota, and T. Kaitsuka, “In-situ contact formation for ultra-low contact resistance NiGe using carrier activation enhancement (CAE) techniques for Ge CMOS,” in *2014 Symposium on VLSI Technology Digest of Technical Papers*, 2014, pp. 146–147.

[66] S. H. Huang, F. L. Lu, W. L. Huang, C. H. Huang, and C. W. Liu, “The ∼3 × 1020 cm-3 electron concentration and low specific contact resistivity of phosphorus-doped Ge on Si by in-situ chemical vapor deposition doping and laser annealing,” *IEEE Electron Device Letters*, vol. 36, no. 11, pp. 1114–1117, 2015, doi: 10.1109/LED.2015.2478916.

[67] M. van Dal *et al.*, “Ge CMOS gate stack and contact development for Vertically Stacked Lateral Nanowire FETs,” in *Proc. 2018 International. IEEE Electron Devices Meeting (IEDM)*, 2018, pp. 492–495.

[68] J. Y. J. Lin, A. M. Roy, Y. Sun, and K. C. Saraswat, “Metal-insulator-semiconductor contacts on Ge: Physics and applications,” *2012 International Silicon-Germanium Technology and Device Meeting, ISTDM 2012 - Proceedings*, vol. 453, no. 2009, pp. 92–93, 2012, doi: 10.1109/ISTDM.2012.6222473.

[69] P. P. Manik and S. Lodha, “Contacts on n-type germanium using variably doped ZnO and highly doped ITO interfacial layers,” *Applied Physics Express*, vol. 8, p. 051302, 2015.

[70] S. Dev, N. Remesh, Y. Rawal, P. P. Manik, B. Wood, and S. Lodha, “interfacial layer Low resistivity contact on n-type Ge using low work-function Yb with a thin TiO 2 interfacial layer,” *Appl Phys Lett*, vol. 108, pp. 103507-1-103507–4, 2017.

[71] K. Gallacher, P. Velha, D. J. Paul, I. MacLaren, M. Myronov, and D. R. Leadley, “Ohmic contacts to n-type germanium with low specific contact resistivity,” *Appl Phys Lett*, vol. 100, no. 2, 2012, doi: 10.1063/1.3676667.

[72] B. Yang *et al.*, “Low-contact-resistivity nickel Germanide contacts on n+Ge with phosphorus/antimony co-doping and Schottky Barrier Height lowering,” in *Proceedings of ISTDM 2012*, 2012, vol. 13, no. 1, pp. 90–91. doi: 10.1109/ISTDM.2012.6222472.

[73] K. Martens *et al.*, “Record low contact resistivity to n-type Ge for CMOS and memory applications,” *Technical Digest - International Electron Devices Meeting, IEDM*, pp. 428–431, 2010, doi: 10.1109/IEDM.2010.5703387.

[74] H. Yu *et al.*, “Heterostructure at CMOS source/drain: contributor or alleviator to the high access resistance problem?,” in *Proc. 2016 International. IEEE Electron Devices Meeting (IEDM)*, 2016, pp. 604–607.

[75] K. Martens *et al.*, “Contact resistivity and Fermi-level pinning in n-type Ge contacts with epitaxial Si-passivation,” *Appl Phys Lett*, vol. 98, no. 1, pp. 2012–2015, 2011, doi: 10.1063/1.3530437.

[76] W. Hsu *et al.*, “High Phosphorus Dopant Activation in Germanium Using Laser Spike Annealing,” *IEEE Electron Device Letters*, vol. 37, no. 9, pp. 1088–1091, Sep. 2016, doi: 10.1109/LED.2016.2587829.

[77] R. Milazzo *et al.*, “Low temperature deactivation of Ge heavily n-type doped by ion implantation and laser thermal annealing,” *Appl Phys Lett*, vol. 110, no. 1, pp. 011905-1-011905–4, 2017, doi: 10.1063/1.4973461.

[78] A. G. Lind, H. L. Aldridge, C. Hatem, M. E. Law, and K. S. Jones, “ Review—Dopant Selection Considerations and Equilibrium Thermal Processing Limits for n + -In 0. 53Ga 0.47 As ,” *ECS Journal of Solid State Science and Technology*, vol. 5, no. 5, pp. Q125–Q131, 2016, doi: 10.1149/2.0201605jss.

[79] J. Zhang *et al.*, “Effective Contact Resistivity Reduction for Mo/Pd/n-In0.53Ga0.47 as Contact,” *IEEE Electron Device Letters*, vol. 40, no. 11, pp. 1800–1803, Nov. 2019, doi: 10.1109/LED.2019.2944245.

[80] W. Melitz *et al.*, “Scanning tunneling spectroscopy and Kelvin probe force microscopy investigation of Fermi energy level pinning mechanism on InAs and InGaAs clean surfaces,” *J Appl Phys*, vol. 108, no. 2, Jul. 2010, doi: 10.1063/1.3462440.

[81] Y. Takamura, P. B. Griffin, J. D. Plummer, Y. Takamura, P. B. Griffin, and J. D. Plummer, “Physical processes associated with the deactivation of dopants in laser annealed silicon Physical processes associated with the deactivation of dopants in laser annealed silicon,” *J Appl Phys*, vol. 92, no. 1, pp. 235–244, 2002, doi: 10.1063/1.1481974.

[82] L. L. Wang *et al.*, “Comprehensive study of Ga activation in Si, SiGe and Ge with 5 × 10-10 Ω·cm2 contact resistivity achieved on Ga doped Ge using nanosecond laser activation,” in *2017 Technical Digest - International Electron Devices Meeting, IEDM*, 2017, pp. 22.4.1-22.4.4. doi: 10.1109/IEDM.2017.8268441.

[83] J.-L. Everaert *et al.*, “Sub-10-9 Ω·cm2 contact resistivity on p-SiGe achieved by Ga doping and nanosecond laser activation,” in *Digest of Technical Papers - Symposium on VLSI Technology*, 2017, pp. T214–T215. doi: 10.23919/VLSIT.2017.7998176.