**Polarity-induced threshold voltage shift in ovonic threshold switching chalcogenides and the impact of material composition**

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Amorphous chalcogenide-based ovonic threshold switch (OTS) selectors are an important part of the cross-point memory arrays. It is known that the threshold voltage ($V_{th}$) of the OTS device can be affected by operating conditions, such as pulse amplitude and ramp rate. In this work, we investigate the impact of pulse polarity on OTS parameters. We summarize our recent findings on the polarity-induced $V_{th}$ shift observed in SiGeAsTe and SiGeAsSe materials. This effect is manifested as a stable and reversable change in $V_{th}$ resulting from the reversal of applied pulse polarity, thus allowing $V_{th}$ to be electrically controlled. Here, we report for the first time exceptionally large polarity-induced $V_{th}$ shift in GeSe OTS. We compare the behavior observed in binary GeSe and quaternary SiGeAs(Te/Se) material systems and discuss the dependence of polarity effects on composition of OTS devices. We further investigate the impact of film thickness, interface, and stoichiometry in GeSe OTS.

## 1. Introduction

In recent years a lot of attention has been devoted towards the development of storage class memory (SCM) technologies, such as phase-change memory (PCM),[1] promising to deliver high-performance non-volatile memory at low-cost to fill the growing gap in the existing memory hierarchy.[2] One of the strategies for achieving the desired cost-effectiveness of SCM solutions is the adoption of cross-point array architecture, which reduces the cost-per-bit by providing smallest-possible cell area and the possibility of stacking multiple memory planes or vertical 3D integration.[3] This design, in turn, requires a non-linear two-terminal selector device to suppress the so-called „sneak currents“ – unavoidable leakage paths through half-selected cells.[4] When considering PCM memory element, the most commonly used selector is the amorphous chalcogenide-based ovonic threshold switch (OTS),[5] thanks to its strong non-linearity and compatibility with PCM materials.[6]

There are certain challenges associated with the operation of OTS devices originating from the nature of threshold switching phenomena. One of them is the instability of the threshold voltage ($V_{th}$). For example, one of the known issues is the $V_{th}$ relaxation effect (drift),[7,8] manifested as an increase of $V_{th}$ after prolonged delay time in between the measurement pulses. Additionally, it has been reported that the properties of the pulse itself can also have noticeable impact on $V_{th}$ as well. This includes the dependence on pulse amplitude,[9] pulse width,[10] and the ramp rate.[11]

Moreover, we have demonstrated that pulse polarity can strongly affect the value of $V_{th}$ in various OTS materials. We have described a polarity-induced $V_{th}$ shift in SiGeAsTe OTS, manifested as an increase of $|V_{th}|$ upon the reversal of pulse polarity.[12] More recently, we have observed a similar effect in Se-based SiGeAsSe OTS with much stronger magnitude of threshold voltage shift ($\Delta V_{th}$).[13] On the one hand, this effect constitutes an additional source of $V_{th}$ instability. On the other hand, it provides a way of electrically tuning the $V_{th}$, which may open new possibilities for the use of OTS materials. One possibility is to implement an OTS-only self-selecting memory cell.[12,14] In order to facilitate these new applications, it is necessary to identify the tuning knobs responsible for the $V_{th}$ shift to be able to optimize the material and device architecture to reach the desired specifications. The aim of the present work is to provide an initial assessment of the polarity effect observed in different material systems, including SiGeAsTe, SiGeAsSe and various flavors of GeSe.

## 2. Polarity-induced $V_{th}$ shift in quaternary SiGeAs(Te/Se) materials

### 2.1. Bipolar operation of the OTS selectors

Normally, the OTS devices are targeted for the use as selector devices together with PCM memory element, which is a unipolar technology (i.e., can be operated with only one polarity). As a result, the impact of pulse polarity is not often considered.[15–18] In this work, we aim at exploring this aspect of OTS device operation.

First, consider the standard unipolar operation of an OTS selector. **Figure 1a** shows a schematic of one of the investigated devices, based on 20nm SiGeAsTe OTS integrated into a pillar cell configuration. A typical I-V characteristics measured with positive polarity pulses (as depicted in Figure 1b) is shown in Figure 1c. Naturally, during the first-fire (FF) pulse the threshold voltage ($V_{FF}$) is larger as compared to the $V_{th}$ during the subsequent switching (SW) pulse in the same direction. This can be attributed to the formation of a conduction cluster consisting of delocalized defects, some of which can remain quenched in the delocalized state after the switch-off and result in a reduced $V_{th}$ during the SW pulse.[8] In the same way, the OTS can be switched in the negative direction, as demonstrated in Figure 1d and Figure 1e. In both polarities, similar values of the absolute values of $|V_{th}|$ are obtained. Note, that in this case the device structure is symmetric, with the same top (TE) and bottom electrodes (BE). While the OTS can be switched in either positive or negative polarity separately, it is interesting whether reversing the pulse polarity can affect device properties.

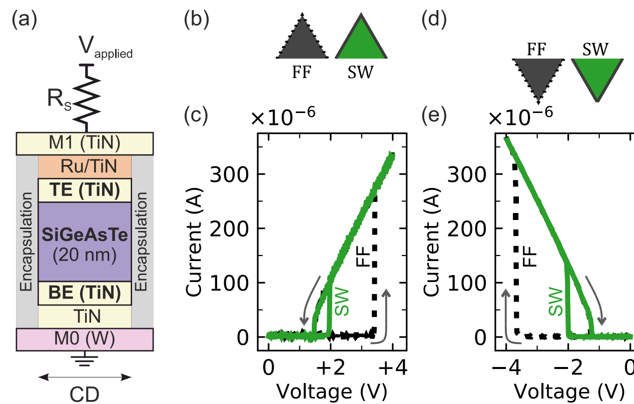


**Figure 1.** (a) Schematic of a SiGeAsTe OTS selector device in a pillar cell structure. (b) Test sequence and (c) corresponding I-V characteristics measured with positive polarity pulses. (d), (e) – same for the nagative polarity pulses. OTS can operate in both polarities, since the device structure is symmetric. Here, CD=55nm is used.

**2.2. Polarity effect in Te-based SiGeAsTe**

To investigate the impact of the reversal of pulse polarity we have extensively studied the behavior of OTS device under the application of a sequence of bipolar pulses, as shown in **Figure 2a**. We have previously reported the results of such an experiment in SiGeAsTe material, which are summarized below.[12] Figure 2b shows the I-V characteristics measured during the first five pulses in the measurement sequence (FF, followed by two positive and then two negative pulses). Focusing on the data obtained from the negative polarity one can see a clear increase in $|V_{th}|$ value for the first negative pulse as compared to the subsequent cycle in the same direction. We refer to this difference as the polarity-induced threshold voltage shift ($\Delta V_{th}$). Note that for this particular device such a shift is only present in the negative (NEG) read-out branch ($\Delta V_{th}^{NEG}$), while it is practically absent in the positive (POS) branch ($\Delta V_{th}^{POS}$).

Throughout this work we will adopt the following convention for the threshold voltage shift ($\Delta V_{th}$), calculated according to Equation (1).

$$\Delta V_{th} = \left|V_{th}^{opp}\right| - \left|V_{th}^{same}\right| \quad (1)$$

where $V_{th}^{opp}$ corresponds to the $V_{th}$ extracted from the pulse with the *opposite* polarity compared to the previous one, and $V_{th}^{same}$ is the $V_{th}$ for the *same* polarity pulse. Focusing separately on the POS and NEG read-out branches this will result in Equation (2) and Equation (3), respectively.

$$\Delta V_{th}^{POS} = \left|V_{th,NEG}^{POS}\right| - \left|V_{th,POS}^{POS}\right| \quad (2)$$

$$\Delta V_{th}^{NEG} = \left|V_{th,POS}^{NEG}\right| - \left|V_{th,NEG}^{NEG}\right| \quad (3)$$

where the superscript denotes the polarity of the current (Read) pulse and the subscript – polarity of the previous (Write) pulse.

To highlight the consistent nature of the polarity-induced $V_{th}$ shift, the distributions of $\Delta V_{th}^{POS}$ and $\Delta V_{th}^{NEG}$ values extracted from the measurement repeated on multiple devices are shown in Figure 2c. Most of the devices show a noticeable shift in the NEG branch, with median $\Delta V_{th}^{NEG} \approx 280$mV. It is also important to note that this effect is preserved even after repeated bipolar cycling.[12]

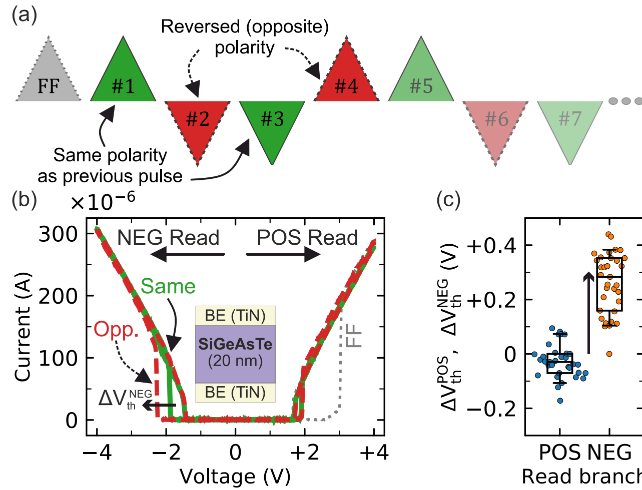


**Figure 2.** Bipolar operation in SiGeAsTe OTS. (a) Pulse sequence consisting of pairs of bipolar pulses and (b) corresponding I-V characteristics (CD=60nm). $|V_{th}|$ increases after the reversal of pulse polarity from positive to negative. Adapted with permission.[12] © 2021, IEEE. (c) Distributions of the threshold voltage shift ($\Delta V_{th}$) extracted in positive and negative read-out branches. Consistent $\Delta V_{th}^{NEG}$ ~300mV is observed in the NEG direction.

### 2.3. Polarity effect in Se-based SiGeAsSe

Following the initial observation of the polarity-dependent effect in Te-based SiGeAsTe, we have recently reported an even larger magnitude of this effect in Se-based SiGeAsSe OTS.[13] **Figure 3a** shows the result of a bipolar I-V measurement. Note, that a carbon-based electrode material is used for TE and BE in this device (see inset in Figure 3a). There are few things that deserve attention here. Firstly, the magnitude of the $\Delta V_{th}$ shift is much stronger ($\Delta V_{th}^{NEG}$ ~ 1.3V). Secondly, the effect appears to become more symmetric with opening of a non-zero $\Delta V_{th}$ in POS read-out branch ($\Delta V_{th}^{POS}$ ~ 0.6V). Figure 3b shows the distribution of the shifts in both read branches. Note that in both cases, the $|V_{th}|$ increases whenever the polarity is reversed (either from positive to negative, or from negative to positive). Therefore, the $V_{th}$ state of the SiGeAsSe OTS depends on the *relative polarity* of the Write and Read pulses. For example, after a POS pulse, the device will be in a low-$V_{th}$ state when read in POS direction, but the same POS pulse results in a high-$V_{th}$ state when read in the NEG direction.

The relatively large $\Delta V_{th}$ in SiGeAsSe material enables practical applications of this effect. For example, we have demonstrated that the performance of 1OTS-1PCM cell can be greatly enhanced when operated in bipolar mode.[13] In addition to increased memory window, we have shown that the memory effect in OTS is present at a current level which is much lower than RESET current of PCM cell, making it useful for low-power applications.

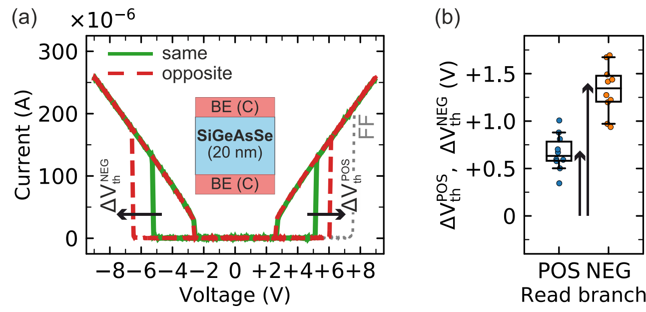


**Figure 3.** Bipolar operation in SiGeAsSe OTS. (a) I-V characteristics measured with a sequence of bipolar pulses (same as in Figure 2a). Adapted with permission.[13] © 2022, IEEE. (b) Extracted $\Delta V_{th}$ distributions. The magnitude of the polarity-induced shift is much stronger ($\Delta V_{th}^{NEG}$~1.3V) compared to SiGeAsTe. Also, the effect is more symmetric and is observed in both POS and NEG read-out directions.

## 2.4. Diminishing $\Delta V_{th}$ at high-current regime in SiGeAs(Te/Se)

To elaborate more on the impact of operating current ($I_{op}$) on the polarity effect we subject both SiGeAsTe and SiGeAsSe OTS devices to the operation under rather high $I_{op}$ values. **Figure 4a** shows the result for SiGeAsSe operated at $I_{op}$ ~ 4mA. Note that the polarity-induced shift has disappeared completely, both in POS and NEG directions. This is confirmed on multiple devices, as shown in Figure 4b. In both directions the median $\Delta V_{th} \approx 0$. Same is true for SiGeAsTe OTS already at $I_{op}$ ~ 2mA, as demonstrated in Figure 4c. Here, the dashed lines represent the median values of $\Delta V_{th}$, measured at $I_{op}$ ~ 300μA in both materials.

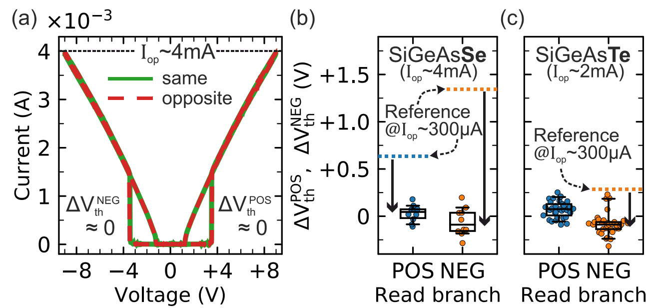


**Figure 4.** Behavior at high operating current. (a) I-V characteristics measured using a bipolar test sequence (same as in Figure 2a) on SiGeAsSe OTS at $I_{op}$~4mA. No $V_{th}$ shift is observed in this regime. (b) Extracted $\Delta V_{th}$ distribution for SiGeAsSe at $I_{op}$ ~ 4mA and (c) SiGeAsTe at $I_{op}$ ~ 2mA. In both cases $\Delta V_{th} \approx 0$. Dashed lines represent median values at low-$I_{op}$ regime.

## 3. Polarity effect in binary GeSe OTS

In this section we report the results of the bipolar measurements on a different material system, namely a binary GeSe.[19,20] We compare its behavior to that of the SiGeAsTe and SiGeAsSe,[21] and establish the different factors that control the properties of the effect, focusing on the high-current regime.

### 3.1. Exceptionally strong polarity effect in GeSe OTS at high $I_{op}$

First, we limit our investigation to a 20nm GeSe (with nominal composition of $Ge_{50}Se_{50}$) integrated into a mushroom cell (see **Figure 5a**). Note, that the structure is different compared to the pillar cell used in SiGeAs(Te/Se) devices.

#### *3.1.1. Magnitude and direction of the $\Delta V_{th}$ shift*

Figure 5b shows the bipolar I-V characteristics measured on GeSe at high-current regime ($I_{op}$~4mA). One can clearly see significant differences in behavior compared to SiGeAs(Te/Se) materials. Firstly, the magnitude of the shift in the POS branch is dramatically enhanced, up to $\Delta V_{th}^{POS} > 3V$. Secondly, the direction of the shift in the NEG branch is reversed, resulting in $\Delta V_{th}^{NEG} < 0$. This means that the $|V_{th}|$ measured in the NEG polarity is lower if the previously was positive (even though it corresponds to the opposite polarity). Therefore, the *absolute polarity* determines the $V_{th}$ state of the GeSe OTS. Specifically, the device is in the low-$V_{th}$ state after a POS Write pulse (both for POS and NEG read-out), while the NEG pulse leads to a high-$V_{th}$ state. Also note that the magnitude of the $\Delta V_{th}$ is different for the two read-out directions, with stronger shift in POS branch ($\Delta V_{th}^{POS} \approx 3.5V$, $\Delta V_{th}^{NEG} \approx -1V$).

It is interesting that GeSe exhibits such a strong polarity-induced $V_{th}$ in the high-$I_{op}$ regime, while the SiGeAs(Te/Se) OTS lose the polarity effect completely at this current level. It is also worth mentioning that even at such a high current, the device can be repeatedly switched between the low-$V_{th}$ and high-$V_{th}$ states (see **Figure S1** and **Figure S2**). Nevertheless, one can expect some degradation of the OTS after continued operation at such a stress level. Therefore, we will limit our study to a slightly lower $I_{op}$~2mA (which is nonetheless rather high). Figure 5c shows the distribution of $\Delta V_{th}$ values measured across multiple devices at $I_{op}$~2mA. A very strong positive shift with median $\Delta V_{th}^{POS} \approx 2.5V$ is consistently observed.

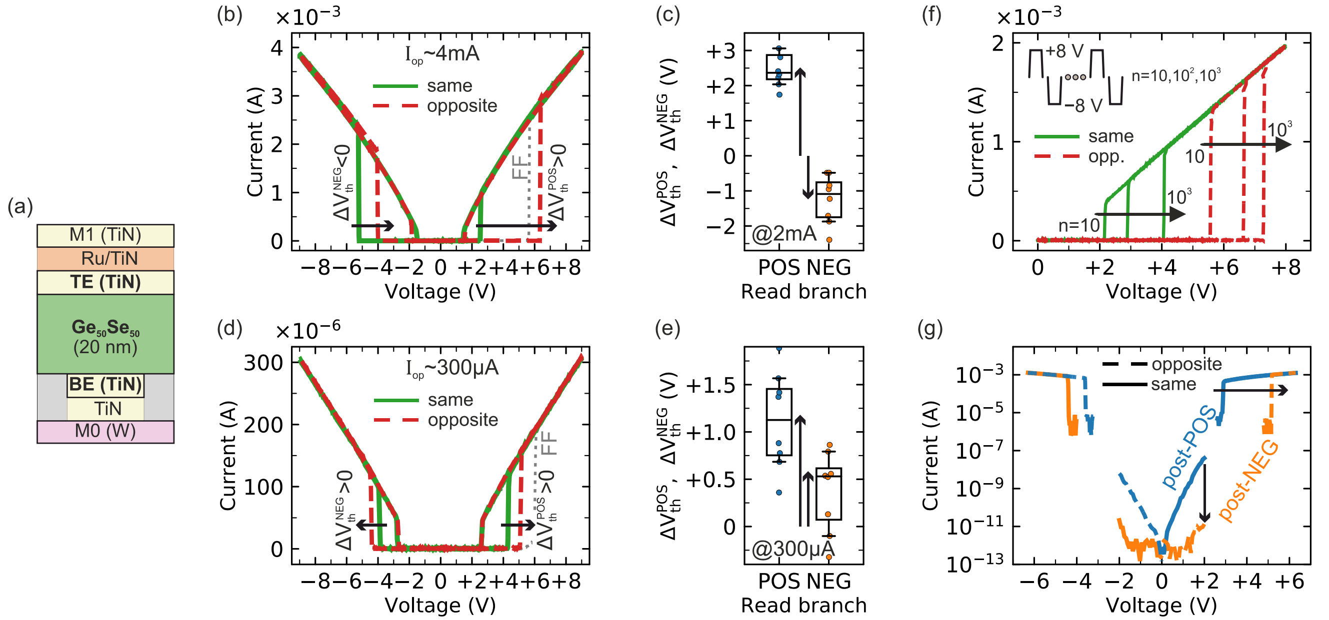


**Figure 5.** Polarity effect in GeSe OTS. (a) Schematic of a GeSe OTS selector device in a mushroom cell structure. (b) Bipolar I-V characteristics measured at high $I_{op}$~4mA, showing exceptionally large $\Delta V_{th}^{POS}$. (c) $\Delta V_{th}$ distributions measured at $I_{op}$~2mA. Note, that in addition to much increased magnitude of the ffect the direction of the $V_{th}^{NEG}$ shift in the NEG polarity is reversed compared to SiGeAsTe and SiGeAsSe. (d) Same measurement performed in the low-$I_{op}$ regime (~300µA) and (e) the distribution of corresponding $\Delta V_{th}$ values. The direction of the $V_{th}$ shift is the same as for SiGeAs(Te/Se). (f) Evolution of the $V_{th}$ after bipolar stress cycling (at high $I_{op}$~2mA). The polarity-induced shift is preserved even after $10^3$ cycles. (g) DC I-V characteristics (CD=65nm), showing significant change in the sub-threshold conduction, depending on the polarity of the previous applied pulse. Overlayed is the AC switching data.

### *3.1.2. Comparison of GeSe operated at low $I_{op}$*

For completeness, we also study the polarity effect in GeSe operated in the low-$I_{op}$ regime, to be compared with the behavior observed in SiGeAs(Te/Se) materials. The result of a bipolar measurement performed at $I_{op}$~300µA is shown in Figure 5d and Figure 5e. One can see that the polarity effect is preserved also at a lower $I_{op}$. However, the behavior is qualitatively different, with the direction of the $\Delta V_{th}^{NEG}$ shift being the same as in the case of SiGeAsTe (as shown in Figure 2) and SiGeAsSe (Figure 3). This may point to the similar mechanism being responsible for the low-$I_{op}$ behavior in all three studied material systems, as will be discussed in Section 4.2. Interestingly, only GeSe experiences a pronounced polarity effect at high $I_{op}$.

Quantitatively, it is clear that the magnitude of the low-$I_{op}$ shift is much smaller compared to that observed at high $I_{op}$. Moreover, polarity effect in GeSe at low $I_{op}$ is less stable and $\Delta V_{th}$ experiences larger variability compared to SiGeAs(Te/Se). Therefore, for the rest of this work we will focus on the high-$I_{op}$ (~2mA) regime in various flavors of GeSe devices.

*3.1.3. Robustness of the $V_{th}$ shift against bipolar cycling*

It is worthwhile to note that the above-described polarity effect is preserved even after repeated cycling. Figure 5f shows the evolution of $V_{th}$ measured with positive read-out voltage after a sequence of bipolar stress cycles (see inset in Figure 5f). It is clear that even after 1000 pulses the device is still functional, and the polarity-induced $V_{th}$ shift is maintained. Additionally, there is a tendency towards increasing $V_{th}$ values for increasing number of cycles. In fact, after prolonged cycling the device appears to fail (stuck as OPEN), because the $V_{th}$ in high-$V_{th}$ state drifts above the applied test voltage (see **Figure S3**). While the endurance of GeSe under bipolar operation at a high-$I_{op}$ regime (~$10^3$ cycles) is not good enough for practical applications, it does illustrate the fact that the polarity-induced effect is reversible and can sustain certain amount of cycling stress.

*3.1.4. Impact of polarity on the sub-threshold conduction*

Finally, we explore the impact of pulse polarity on the sub-threshold conduction in GeSe OTS. Figure 5g shows the low-field ($V = -2V \rightarrow +2V$) DC I-V measurement performed after either a positive or a negative AC pulse. A dramatic change in the leakage current ($I_{leak}$) can be observed, depending on the polarity of the AC pulse used to set the device. Overlayed is the AC switching data. Note the correlation between the DC and AC data: POS Write pulse results in a low-$V_{th}$ & high-$I_{leak}$ state, while NEG pulse results in a high-$V_{th}$ & low-$I_{leak}$ state.

**3.2. Impact of GeSe thickness**

Next, we focus on the dependence of the polarity effect in GeSe OTS on different factors. Firstly, we examine the dependence on the thickness of the OTS layer. So far, we have limited our discussion to 20nm-thick GeSe. For the reference, **Figure 6a** shows the distribution of the threshold voltage in 20nm GeSe for the *same* and *opposite* polarity pulses. Figure 6b presents the result of a similar measurement performed on a thinner 10nm GeSe film. As expected, for decreasing thickness of the chalcogenide layer the $V_{th}$ reduces. Additionally, the polarity-induced shift is also present in a thinner device. As for the magnitude of the $\Delta V_{th}$, it also

reduces somewhat with thickness, as shown in Figure 6c. Note, that the magnitude of $\Delta V_{th}^{POS}$ is reduced compared to 20nm reference sample, while $\Delta V_{th}^{NEG}$ remains almost unchanged.

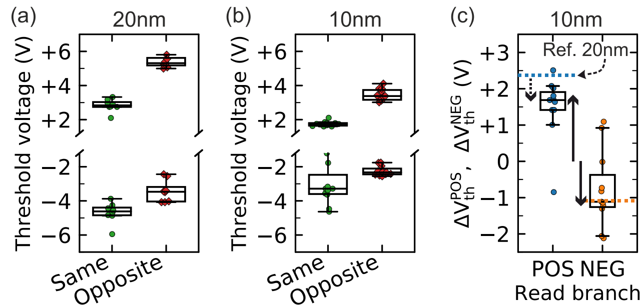


**Figure 6.** Thickness dependence. (a) Threshold voltage distribution for *same* and *opposite* polarity pulses for 20nm GeSe (CD=70nm) and (b) same for 10nm GeSe OTS devices (CD=75nm). (c) Calculated $V_{th}$ shifts for 10nm GeSe. The effect is preserved for the thinner OTS film, but with smaller amplitude (dashed lines represent median values for 20nm GeSe).

### 3.3. Impact of interface oxidation

Secondly, we investigate the impact of the interface quality. For this we study two 10nm GeSe samples that are identical except for the difference in the deposition process of the TiN top electrode. In one case it was deposited in-situ immediately after the deposition of GeSe OTS layer. This ensures that the interface between GeSe OTS and TiN TE is not excessively oxidized (see **Figure 7a**). In the other sample, the TiN TE was deposited ex-situ, meaning that there was a vacuum break after the deposition of GeSe. This exposes the GeSe to air prior to TiN deposition, resulting in an additional oxidation of the top interface, as depicted in Figure 7b. The results of bipolar test sequence performed on both samples are compared in Figure 7c and Figure 7d, focusing only on the positive read-out branch (i.e., $\Delta V_{th}^{POS}$).

First, consider the distribution of $\Delta V_{th}^{POS}$ measured on fresh devices (i.e., in the beginning of the bipolar test sequence, see Figure S1). Interestingly, the sample with ex-situ deposited TE shows tighter distribution and hence smaller variability in $\Delta V_{th}^{POS}$. Moreover, it seems to be more stable after cycling. Figure 7d shows the same distributions but measured after 35 bipolar pulses. Note that for the sample with in-situ TE, most of the devices lose the polarity shift completely. In contrast, the ex-situ TE sample (with oxidized TE interface) preserves the effect even after cycling, despite the increase in $\Delta V_{th}^{POS}$ variability. It appears that the presence of the oxidized interfacial layer is beneficial for the stability of the polarity effect in GeSe OTS.

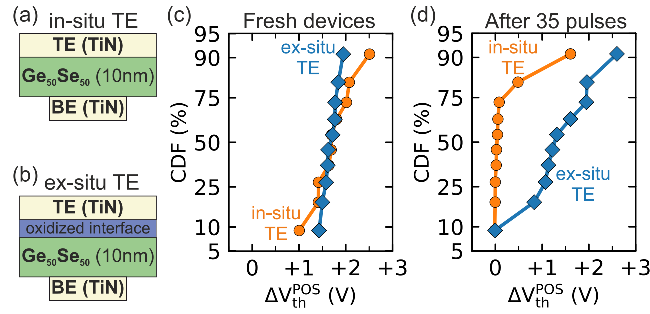


**Figure 7.** Impact of interface oxidation. (a) Schematic of a GeSe mushroom cell with an in-situ deposited top TiN electrode (no extra oxidation of GeSe at TE electrode). (b) Sample fabricated with an ex-situ deposited TiN TE, resulting in an additional oxidation. Here, CD=75nm is used. (c) Distribution of $\Delta V_{th}^{POS}$ values in the beginning of the test sequence and (d) same for the values extracted after 35 bipolar pulses. Ex-situ TE results in tighter $\Delta V_{th}^{POS}$ distribution, as well as better stability against cycling.

### 3.4. Impact of GeSe stoichiometry

Finally, we discuss the dependence of the polarity effect on the stoichiometry of the GeSe film. Until now, we focused on the $Ge_{50}Se_{50}$ composition (nominal composition). In **Figure 8** we compare the target $Ge_{50}Se_{50}$ (Figure 8a) with a Ge-rich $Ge_{60}Se_{40}$ (Figure 8b) material. Both samples are 10nm thick with ex-situ deposited TiN TE. Figure 8c shows the distribution of $\Delta V_{th}$ for $Ge_{50}Se_{50}$, while the same data for $Ge_{60}Se_{40}$ is shown in Figure 8d. Note the degradation in the magnitude of $\Delta V_{th}$ as well an increased variability in the Ge-rich sample. We can conclude that higher Se content is beneficial for the polarity effect.

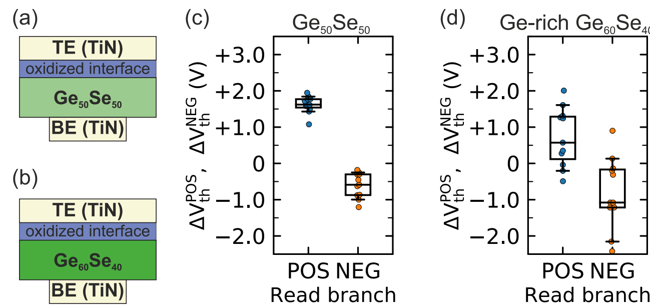


**Figure 8.** Impact of GeSe stoichiometry. (a) GeSe mushroom cell with Ge-poor and (b) Ge-rich GeSe compositions, both with ex-situ deposited TE (CD=75nm). (c) Distribution of $\Delta V_{th}^{POS}$ values for $Ge_{50}Se_{50}$ and (d) Ge-rich samples. Clear improvements in the magnitude and stability of polarity effect is observed for lower Ge (or higher Se) concentration.

## 4. Discussion on material dependence and possible mechanisms

### 4.1. Comparison of the behavior in different devices

In this work we have investigated the polarity-dependent effects in different OTS materials, namely SiGeAsTe, SiGeAsSe and $Ge_xSe_{1-x}$. However, the comparison between these samples is not trivial due to the fact that in some cases in addition to the change in material composition, also the cell structure (pillar vs mushroom) and electrode material (TiN vs C-based) was varied. Nonetheless, here we would like to outline some of the observations obtained across multiple samples. These preliminary conclusions may prove to be useful for designing dedicated experiments aimed at in-depth investigation of the polarity effect and its applications.

There are qualitative as well as quantitative differences in behavior depending on the material composition. First, let us focus on the previously reported SiGeAsTe and SiGeAsSe material systems. The two material families show qualitatively similar behavior, which is more pronounced in Se-based material. In this case, the *relative* polarity between the Read and Write pulses determines the $V_{th}$ state of the device. In contrast, for GeSe the *absolute* polarity of the previously applied pulse is solely responsible for the $V_{th}$ and $I_{leak}$ value.

In terms of quantitative differences, the Se-based materials clearly show a stronger $V_{th}$ shift. This is true when comparing SiGeAsTe ($\Delta V_{th}^{NEG} \approx 0.3V$) and SiGeAsSe ($\Delta V_{th}^{NEG} \approx 1.3V$) at low-$I_{op}$ regime. Also, the Se-containing GeSe exhibits very large $V_{th}$ shift ($\Delta V_{th}^{POS} \approx 2.5V$). Of course, this is the case at high-$I_{op}$ regime, at which both SiGeAsTe and SiGeAsSe stop showing any polarity dependence.

### 4.2. Discussion of the mechanism behind polarity effect

Based on these observations, we suggest that depending on a material and an operating current there may be different mechanisms responsible for the polarity effect. For example, it has been suggested in the literature, that the chalcogenide material may experience segregation upon the application of electric field, with different atomic species migrating towards the opposite electrodes, depending on their relative electronegativity.[22] Recently, Hong et al. demonstrated memory functionality based on polarity effect and suggested elemental segregation as a possible mechanism.[23] This may explain the difference in $V_{th}$ and $I_{leak}$ properties of the OTS under the application of different pulse polarities due the change in local composition. In the case of GeSe in the high-$I_{op}$ regime the Joule heating generated due

to large current passing through the device may facilitate such atomic migration. This is in line with increasing $\Delta V_{th}$ observed at higher $I_{op}$ in GeSe. Our preliminary physical characterization results seem to confirm the presence of atomic segregation, but only at high operating current (see the discussion in Supporting Information Section D).

Therefore, we believe that at a low-$I_{op}$ regime (in all three material systems) the mechanism may be different. For instance, in the absence of significant Joule heating, the elemental segregation, if present, may be limited to the localized OTS conduction cluster (and therefore not easily detectable). Otherwise, the mechanism may be of electronic nature. For example, Lee et al. explain the polarity effect in Ge-doped SbTe as "formation of an asymmetric trap-band structure" and the resulting difference in charge trapping and transport.[24] Alternatively, the polarity dependence may arise from the directional properties of the defects forming the conduction cluster,[12] as discussed in Supporting Information. It should be noted that the mechanism of this effect is not clear at the moment and the proposed hypotheses remain to be tested.

**5. Conclusion**

We study the impact of pulse polarity on the threshold voltage of OTS selectors and compare the polarity-dependent effect in different OTS materials. The investigated SiGeAs(Te/Se) and $Ge_xSe_{1-x}$ materials all experience polarity-induced $V_{th}$ (and $I_{leak}$) shift under certain conditions. The magnitude of the shift depends on the material composition, ranging from $\Delta V_{th}$ ~ 0.3V in SiGeAsTe and ~1V in SiGeAsSe, up to >2.5V in GeSe. The SiGeAs(Te/Se) and $Ge_xSe_{1-x}$ material families exhibit different signatures of the polarity effect, with reversed direction of the shift and different $I_{op}$ dependence. We focus specifically on the $Ge_xSe_{1-x}$ system at high-$I_{op}$ regime and establish the impact of film thickness and stoichiometry on the device properties. With this work we hope to encourage further research into the mechanism behind these phenomena, which is yet to be understood. This is especially important, considering the potential applications of polarity-induced effect for memory applications.

**6. Experimental Section/Methods**

*Device fabrication*: To measure the experimental parameters, a set of devices with different OTS material compositions was fabricated. Two device architectures were investigated: mushroom cell and pillar cell. The device consisted of an OTS film sandwiched between the top (TE) and bottom (BE) electrodes. In a mushroom cell the BE was etched into a pillar with critical dimension (CD) defined down to 55nm. A 20nm or 10nm thick OTS film together with TE metal was deposited on top of BE, resulting in a mushroom-type cell structure. In a pillar cell, the whole BE/OTS/TE stack was etched into a pillar. Various OTS compositions were tested, including quaternary Si-Ge-As-Te (with nominal composition $Si_{0.18}Ge_{0.08}As_{0.46}Te_{0.28}$) and Si-Ge-As-Se (with composition $Si_{0.09}Ge_{0.16}As_{0.30}Se_{0.45}$), as well as binary $Ge_xSe_{1-x}$ (x=0.5, 0.6) material systems, deposited by means of physical vapor deposition (PVD) technique.[25]

*Electrical characterization*: The devices were electrically characterized using a series of triangular ac pulses with a rise time of $t_{rise}$=5 μs with alternating voltage polarity. From these measurements the threshold voltage ($V_{th}$) values were extracted. Additionally, sub-threshold leakage was characterized by means of a dc measurement. Structures with nominal CD ranging from 55nm to 75nm were tested (CD=70nm assumed, unless specified otherwise). An integrated series resistor ($R_s$) was used to limit the operating current in the ON-state ($I_{op}$).

**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

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In this work the impact of pulse polarity on the threshold voltage ($V_{th}$) is investigated in different chalcogenide-based OTS materials. We demonstrate exceptionally large $V_{th}$ shift in $Ge_xSe_{1-x}$ OTS and compare it with behavior observed in Si-Ge-As-(Te/Se) material system. Focusing on $Ge_xSe_{1-x}$ material, we study the impact of stoichiometry, thickness, and interface oxidation on the $V_{th}$ shift.

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**Polarity-induced threshold voltage shift in ovonic threshold switching chalcogenides and the impact of material composition**