Supplementary Information

Unraveling the Impact of Nano-scaling on Silicon Field-Effect Transistors for the Detection of Single Molecules

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1. Source-drain dopant profile

We use p-type inversion mode FET devices. The background donor dopant density is set to 1 × 10^{17} cm^{-3} in all silicon segments. The source-drain regions have an acceptor dopant density of 2 × 10^{20} cm^{-3}. The diffusion of the acceptor dopants into the channel is modeled as a Gaussian profile with a σ of 3 nm. The dopant concentration starts to fall off at the interface between the channel and the source-drain segments. This position aligns with the edges of the oxide source-drain passivation. In figure S1, the acceptor dopant profile is shown for a FET with a 100 nm channel or gate length and 20 nm long source-drain regions.

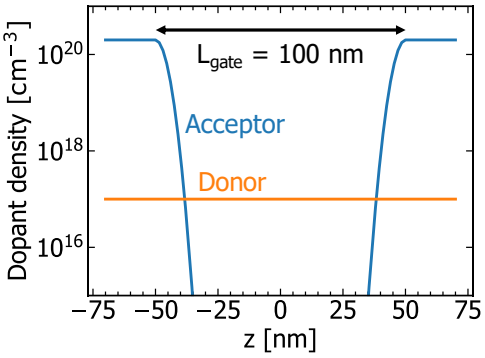

Figure S1. a) The longitudinal acceptor and donor dopant density profile for a FET device with a 100 nm gate length.

2. Discussion on sensitivity metric

In the main text, we use the threshold voltage shift to represent the single-molecule signal of the FET sensor.[1] The threshold voltage shift (ΔV) is extracted using the constant current method evaluated at a drain current 100 mV below the threshold voltage (subthreshold regime). In the subthreshold regime and for small signals (< $\phi_t = \frac{kT}{q}$), the relationship between the gate voltage (V_{GS}) and the drain current (I_{DS}) can be linearized and becomes: $dI_{DS}/I_{DS} = \frac{1}{n\phi_t} dV_{GS}$ with n the ideality factor (>1) and ϕ_t the thermal voltage.[2] The ideality factor n is close to 1 when the electrostatic control of the FET channel is near-ideal and increases when the electrostatic control decreases by for example short-channel effects. $n\phi_t$ is closely related to the subthreshold swing $SS = n\phi_t \ln(10)$. Consequently, when the SS does not change significantly small FET signals either expressed as $\Delta I_{DS}/I_{DS}$ or ΔV are directly proportional. When the subthreshold swing increases due to short-channel effects the current signal $\Delta I_{DS}/I_{DS}$ decreases with respect to the voltage signal ΔV.

3. The effective channel length

To obtain a better metric for the total channel resistance compared to the physical gate length L_{gate}, we introduce the effective channel length L_{eff}. This effective channel length includes the effect that holes from the source-drain regions penetrate the channel and locally reduce the channel resistance. To derive the effective channel length, we study the threshold voltage shift or signal ΔV caused by a positive singularly charged trap at the silicon-gate oxide interface (fig. S2a). This eliminates electrolyte screening effects and focuses on channel electrostatics only. We discuss the trap signal for an electrolyte-gated FET with a 15 mM ionic strength electrolyte. Figure S2a shows the local modulation of the channel potential induced by a trap located in the center of the channel. The potential modulation changes the local hole concentration and thus the local channel resistance. Since the channel can be considered as a series connection of resistances, the change of the total channel resistance is high when a highly resistive location of the channel is modulated i.e. the center of the channel. At the source-drain junctions, the penetration of source-drain holes into the channel locally reduces the channel resistance. Therefore, a trap near the lowly resistive source-drain regions causes a smaller modulation of the total channel resistance ΔR and a strong drop of the trap signal $\Delta V \propto \Delta R/R$ (fig. S2b) occurs.[3]

Based on the results for the trap signal position dependence, we calculate L_{eff} as follows: $L_{eff} = \int \Delta V(z)dz / \Delta V_{center}$ with $\Delta V(z)$ the trap signal at the longitudinal position z and ΔV_{center} the trap signal in the center (z = 0). We integrate over the entire gate length (fig. S2a and methods in main text). For long gate lengths, the difference between the physical gate length L_{gate} and the effective channel length L_{eff} represents the penetration depth of the source-drain holes into the channel (fig. 2c). The difference is constant for gate lengths larger than 100 nm. For shorter gate lengths the difference reduces since the effective channel length cannot become negative. Furthermore, the difference increases for a larger cross-section for which the electrostatic control is reduced i.e. source-drain holes penetrate deeper into the channel (see SI sections 4 and 5).

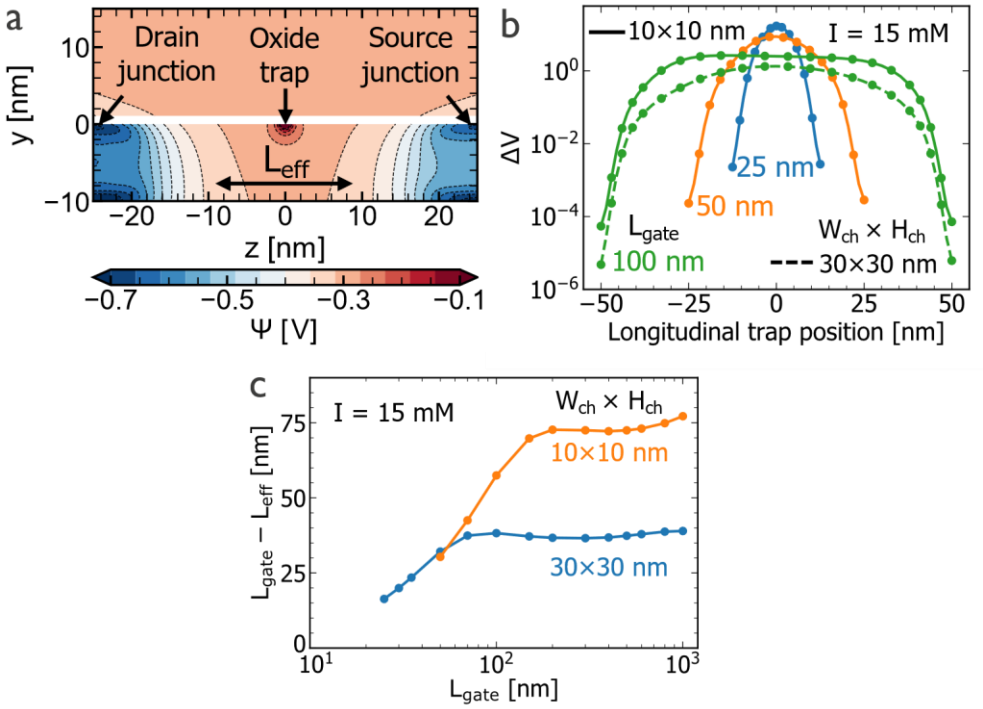

Figure S2. a) The distribution of the potential for a tri-gate FET with 10x10 nm^2 cross-section and 50 nm gate length. Electrolyte ionic strength is 15 mM. A positively charged oxide trap is present at the silicon-gate oxide interface in the middle of the channel. The effective channel length (L_{eff}) is indicated. b) The longitudinal position dependence of the trap signal for 10x10 nm^2 FETs with three different gate lengths and a 30x30 nm^2 FET with 100 nm gate length (L_{gate}). c) Offset between L_{gate} and L_{eff} as a function of L_{gate}.

4. FET short-channel effects

When downscaling the FET gate length, short-channel effects can occur. Short-channel effects are visible in the FET I_{DS}-V_{GS} curves as a threshold voltage roll-off and the increase of the subthreshold swing. In figure S3, we show that for our simulated FETs with 10×10 nm^2 and 30×30 nm^2 cross-sections, the SS increase and V_T roll-off kick in for gate lengths below 50 and 100 nm respectively (fig. S3ab). For the largest cross-section, short-channel effects are more pronounced due to a decreased electrostatic control over the FET channel. When the electrostatic gate control over the channel reduces, the build-up of the channel potential barrier is less steep and spreads more into the channel (fig. S3cd). Short-channel effects arise when the channel potential barrier starts to reduce. For the 10×10 nm^2 and 30×30 nm^2 cross-section, the decrease of the barrier occurs for a gate length below 50 nm and 100 nm respectively (fig. S3cd). This agrees with the onset of the threshold voltage roll-off and subthreshold swing increase.

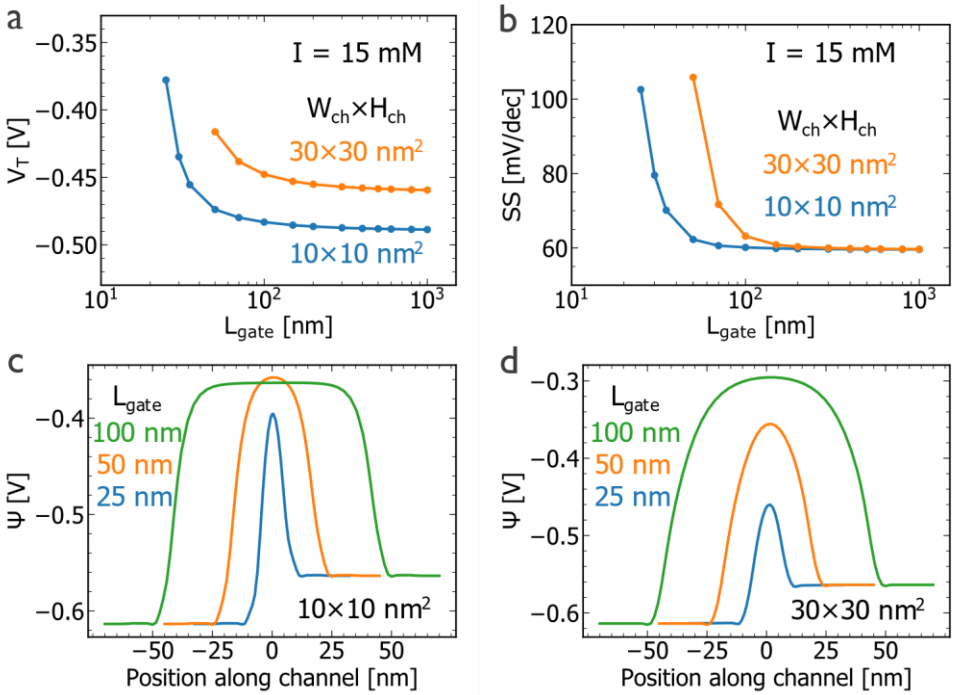

Figure S3. a and b) The threshold voltage V_T and subthreshold swing SS as a function of the gate length for 10×10 nm² and 30×30 nm² FET channel cross-sections. ed) Potential profiles along the FET channel for different gate lengths. c and d) Potential profiles for 10×10 nm² and 30×30 nm² FET channel cross-sections respectively. Potential profiles are taken from the center of the channel and are extracted at 100 mV below V_T in the subthreshold regime. The electrolyte ionic strength is 15 mM.

5. Charge carrier concentration along channel length

In figure S4 we show the charge carrier or hole concentration along the channel length for different gate lengths. The FET is operated in the subthreshold regime at 100 mV underdrive. The hole concentration is high at the source-drain regions and reduces in the channel. However, the hole concentration is not symmetrical and is lower at the drain side of the channel. Since the local channel resistance is inversely proportional to the local hole concentration, the channel resistance is higher at the drain side of the channel. Consequently, modulation of the more resistive drain region side results in a larger modulation of the total channel resistance. This agrees with the somewhat stronger signal obtained for single charges situated at the drain side of the channel as observed in figure 5 of the main text.[3]

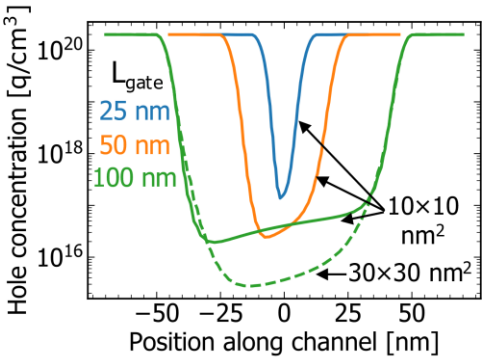

Figure S4. The hole concentration along the channel for different gate lengths and two FET cross-sections equal to 10×10 nm² (solid) and 30×30 nm² (dashed). Hole concentrations are taken from the center of the channel at 100 mV below V_T in the subthreshold regime. The electrolyte ionic strength is 15 mM.

6. Impact of cross-section scaling on drain current

The drain current is used in our reasoning to understand the cross-section-dependent FET signal. Therefore, it is important to determine the drain current scaling trends as a function of the FET dimensions for the different FET architectures (fig. S5). Drain currents are extracted at 100 mV below the threshold voltage in the subthreshold regime (V_{GS}-V_T = 100 mV). For the tri-gate FET, it is observed that for the considered height and width range, the drain current approximately scales with the gated perimeter W_{ch}+2H_{ch}. Remember that for the tri-gate FET the bottom surface is passivated. Also, for the suspended FET, the drain current approximately scales with the gated perimeter 2W_{ch}+2H_{ch}. The suspended FET is surrounded by the electrolyte solution. For the embedded FET the largest deviation from the gated perimeter trend (W_{ch}) occurs. The drain current scaling trend shows that there is a small impact of the FET height on the drain current. This may suggest that some gating arises through the passivated sidewalls of the embedded FET.

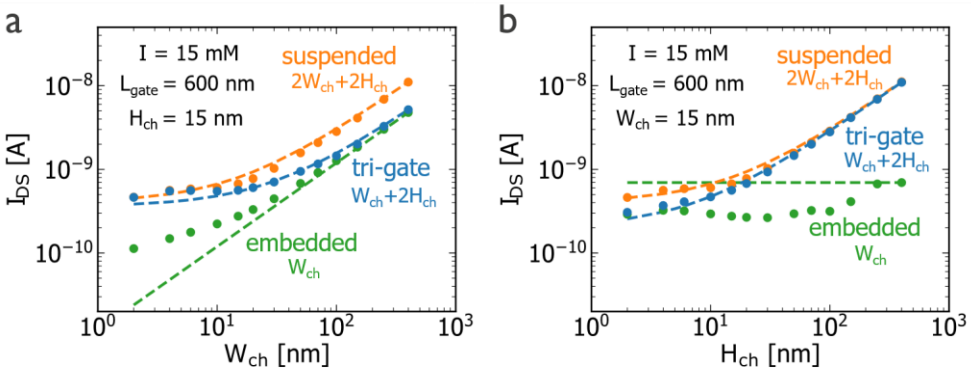

Figure S5. a and b) The drain current I_{DS} as a function of the channel width and height for the different FET architectures. Dots represent simulation data. Dashed lines represent the perimeter trends which are normalized towards the largest channel width and height respectively. The drain current is extracted 100 mV below the threshold voltage in the subthreshold regime.

Next, we discuss the current density distribution in the FET channel which influences the drain current modulation (ΔI_{DS}) trends as a function of channel cross-section. We show that the current density J_z across the entire channel cross-section strongly increases for small FET cross-sections (fig. S6). The current density increase in the bulk of the channel is expected from the overlap of the inversion layers and more densely packed charge carriers (fig. 6cdef). But also at the oxide interfaces, the current density somewhat increases. It is important to notice that for small FETs the threshold voltage decreases (fig. S12d) such that a more negative gate bias is applied at a constant underdrive (V_{GS}-V_T = 100 mV). This results in stronger band bending in the FET channel and contributes to the increased current density at oxide interfaces for small FETs. Consequently, for small cross-sections, the larger current density results in a larger inversion layer capacitance and can increase the fraction of charge mirrored in the inversion channel. This effect boosts ΔI_{DS} and the signal for small FET heights.

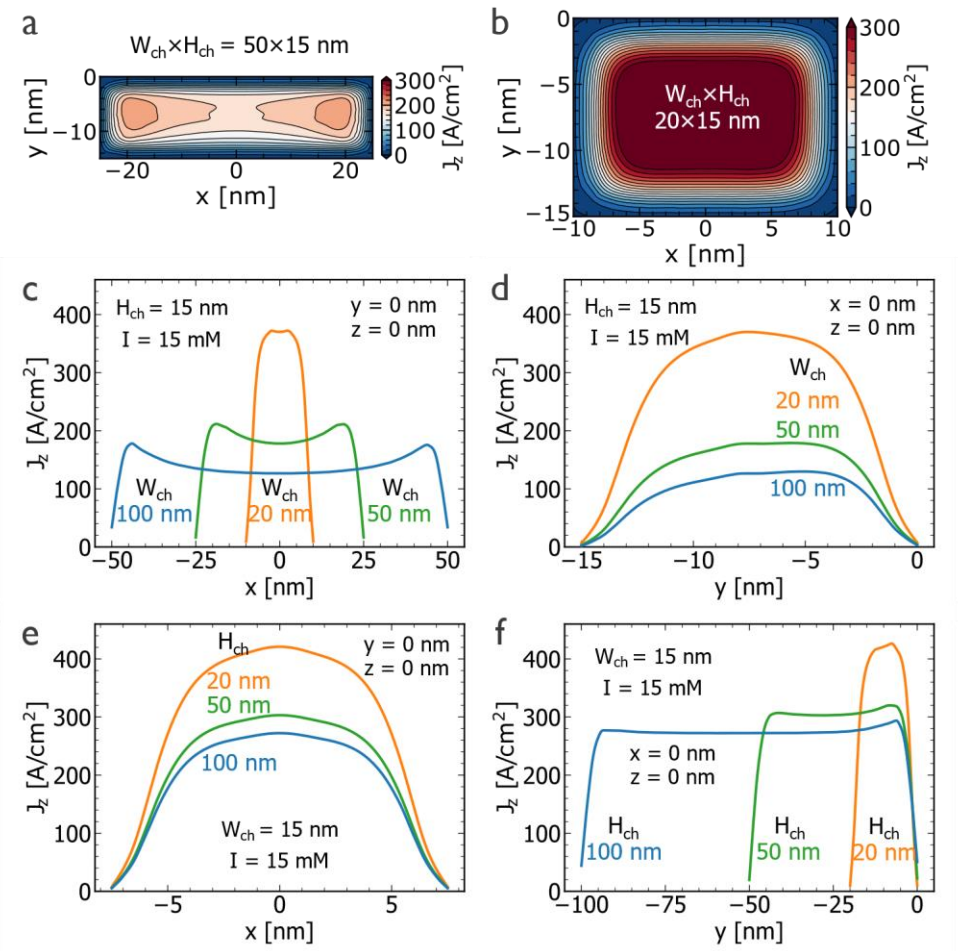

Figure S6. a and b) The current density J_z across the cross-section in the middle of a tri-gate FET (z = 0 nm) with two different channel widths. c and d) Cuts through the middle of the channel (z = 0) along the width (x) and height (y) with the colors representing different channel widths. e and f) Cuts through the middle of the channel (z = 0) along the width (x) and height (y) with the colors representing different channel heights. V_{GS}-V_T = 100 mV.

7. Impact of geometry scaling on FET noise

In the main text, we introduced a noise model based on the ensemble impact of many individual silicon-oxide interface traps that can charge and discharge leading to fluctuations of the threshold voltage shift. We calculate the noise amplitude $V_{noise} = \sqrt{s \int \Delta V_{tr}{}^2 N_{tr,norm}(E_F)\, dA [\ln 1000 - \ln 1]}$. Here, s is a constant calibration factor that represents the spatial trap density and rescales the trap density to match the silicon-SiO_2 interface quality of the used technology. $N_{tr,norm}(E_F)$ is the normalized energy-dependent trap density that represents the number of traps with an energy level equal to the channel Fermi level E_F and ΔV_{tr} is the threshold voltage shift caused by an individual trap at a specific location near the silicon-oxide interface.[4] We integrate over the entire area of the FET interface A = 2×(W_{ch} + H_{ch})×L_{gate}. The variation of the Fermi level and the trap threshold voltage shift across the silicon interface are extracted from our TCAD simulations. We extract the Fermi level, which is referenced to silicon midgap, to calculate $N_{tr,norm}(E_F)$. $N_{tr,norm}(E_F)$ increases for more negative trap level energies, which means that for lower Fermi level energies in the channel more traps contribute to the FET noise. The factor $[\ln 1000 - \ln 1]$ results from the considered frequency range from 1 to 1000 Hz. s is assumed constant for the different interfaces of the device and the different architectures.

Apart from the geometry or device area, the two variable parameters that determine FET noise are the trap threshold voltage shift ΔV_{tr} and the normalized trap density $N_{tr,norm}(E_F)$. Notice that when the mean trap threshold voltage shift follows the expected $1/A$ trend and the normalized trap density $N_{tr,norm}(E_F)$ does not change significantly, a $\sim 1/\sqrt{A}$ trend of the FET noise amplitude occurs. Here, we show how the variation of the trap threshold voltage shift ΔV_{tr} and $N_{tr,norm}(E_F)$ explain the impact of length and width scaling on the FET noise amplitude.

To understand the FET noise as a function of gate length we consider the mean trap induced threshold voltage shift ΔV_{mean} and the mean normalized trap density $N_{tr,norm}(E_F)_{mean}$ for the three different FET architectures: tri-gate, suspended and embedded FET. For all FET architectures, the mean threshold voltage shift follows the expected $1/A$ trend, but the mean trap density increases while scaling down the gate length (fig. S7). The increase in the mean trap density thus makes the FET noise amplitude increase beyond the expected $1/\sqrt{A}$ trend (fig. 12b main text). Furthermore, figure S7 shows that the mean trap induced threshold voltage shift ΔV_{mean} is lowest for the suspended FET but increases for the tri-gate FET and is highest for the embedded FET. Also, $N_{tr,norm}(E_F)_{mean}$ increases in the same order. Since ΔV_{mean} and $N_{tr,norm}(E_F)_{mean}$ are the lowest for the suspended FET, this FET type results in the lowest noise amplitude.

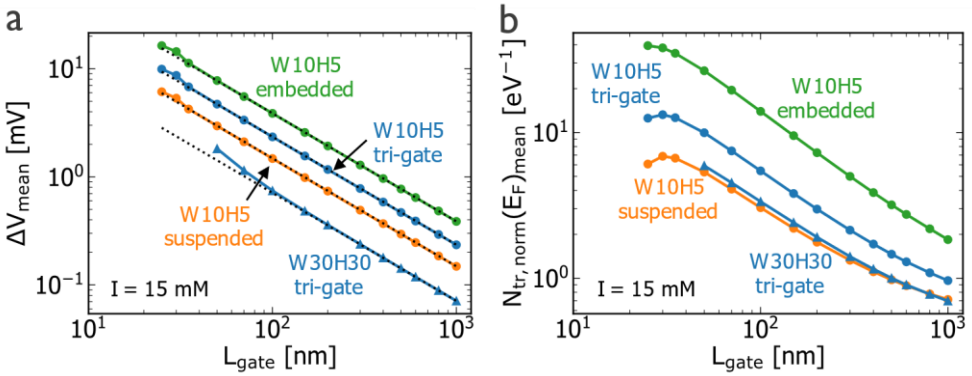

Figure S7. a) The mean trap induced threshold voltage shift ΔV_{mean} as a function of the gate length. Dashed lines represent the expected $1/A = 1/L_{gate}$ scaling trends. b) The mean normalized trap density $N_{tr,norm}(E_F)_{mean}$ as a function of the gate length. Results are shown for the three different FET architectures with W_{ch}×H_{ch} = 10×5 nm^2 (dots) and a tri-gate FET with 30×30 nm^2 cross-section (triangles). The electrolyte ionic strength is 15 mM. The FET is operated in subthreshold: V_{GS}-V_T = 100 mV.

In figure S8, we show the impact or threshold voltage shift due to single traps across the FET surface for the different FET architectures. First, a larger impact of traps is obtained at the passivated surfaces. For example, traps at or close to the passivated bottom surface of the tri-gate FET result in a larger threshold voltage shift compared to traps at the gated top surface. The increased impact of a single trap $\Delta V_{tr} \approx q/C_g$,[5] directly follows from the reduction of the local gate capacitance at the oxide passivated surface. Second, a more passivated FET architecture also results in a larger trap impact at the gated surfaces. For example, at the top surface, the trap impact is highest for the embedded FET and decreases for the tri-gate and suspended FET. This effect is explained by the reduced overall gate capacitance for a more passivated FET architecture. As such a larger modification of the gate voltage or threshold voltage shift is required to compensate for the trap charge. Consequently, the larger the fraction of passivated surfaces, the larger the mean trap induced threshold voltage shift becomes.

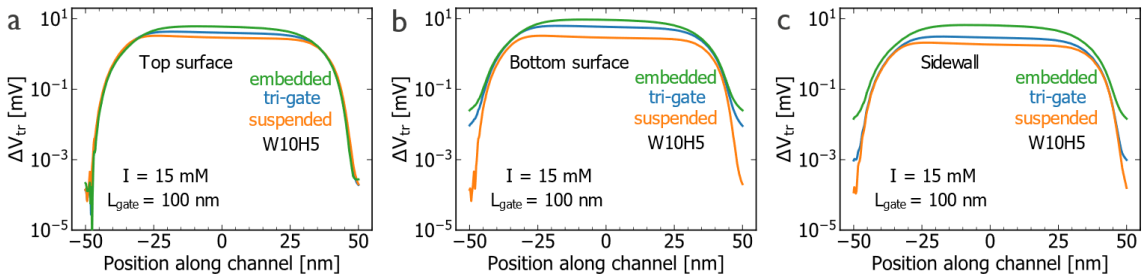

Figure S8. a, b and c) The single trap induced threshold voltage shift ΔV_{tr} as a function of the longitudinal position of the trap. a, b and c) show the values for the top surface, bottom surface and sidewall respectively. Results are shown for the three different FET architectures with W_{ch}×H_{ch} = 10×5 nm^2 and a 15 mM ionic strength of the electrolyte. V_{GS}-V_T = 100 mV.

Furthermore, we elaborate on the variation of the Fermi level energy across the FET surface (fig. S9). This is to understand the increase in the number of traps contributing to the FET noise $N_{tr,norm}(E_F)_{mean}$ for more passivated FET architectures and downscaled gate lengths. In the middle of the channel, the Fermi level energy and normalized trap density are roughly equal for all FET architectures and surfaces (fig. S9). Therefore, the middle region of the channel cannot explain the variation of the mean trap density when downscaling the gate length. However, figure S9 shows that close to the source-drain regions the Fermi level is reduced compared to the center of the channel and $N_{tr,norm}(E_F)$ increases strongly. Consequently, when downscaling the gate length, a larger contribution of the source-drain regions leads to the increase of the mean trap density. At a passivated surface, the Fermi level at the source-drain junctions is even further reduced compared to a gated surface and $N_{tr,norm}(E_F)$ increases further. This results in a larger mean trap density for more passivated FET architectures.

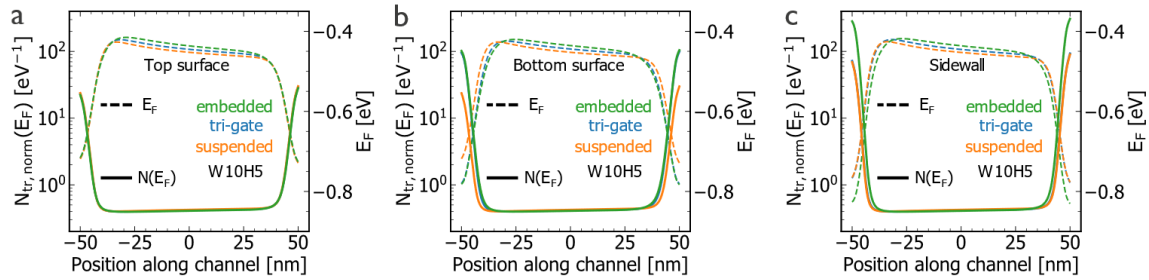

Figure S9. a, b and c) The normalized energy-dependent trap density $N_{tr,norm}(E_F)$ (solid lines) and the Fermi level energy (dashed lines) as a function of the position along the gate length. a, b and c) show the values for the top surface, bottom surface and sidewall respectively. Results are shown for the three different FET architectures with W_{ch}×H_{ch} = 10×5 nm^2 and L_{gate} = 100 nm. V_{GS}-V_T = 100 mV.

Next, we show the mean trap induced voltage shift ΔV_{mean} and mean normalized trap density $N_{tr,norm}(E_F)_{mean}$ as a function of FET width for the different FET architectures (fig. S10). As expected, the ΔV_{mean} and $N_{tr,norm}(E_F)_{mean}$ are lowest for the suspended FET but increase for the tri-gate and embedded FET due to the larger impact of traps at the passivated surfaces. In contrast to length scaling, the different FET types now show a different dependency of ΔV_{mean} and $N_{tr,norm}(E_F)_{mean}$ as a function of FET width.

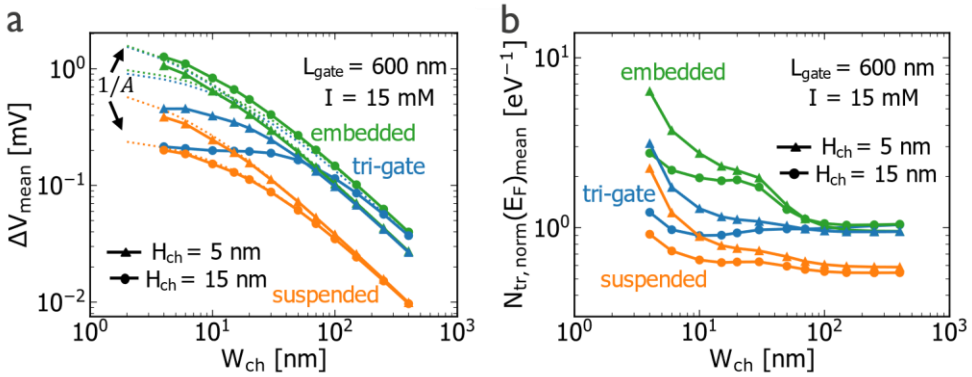

Figure S10. a,b) The mean trap threshold voltage shift ΔV_{mean} and mean normalized trap density $N_{tr}(E_F)_{mean}$ as a function of FET width for different FET architectures with FET heights of 5 and 15 nm. Colors indicate different FET architectures. The $1/A$ trend is indicated with A = 2×(W_{ch} + H_{ch})×L_{gate} the FET interface area. The physical gate length is 600 nm and ionic strength is 15 mM. V_{GS}-V_T = 100 mV.

First, we discuss ΔV_{mean} as a function of FET width which dominates the observed trend of the noise amplitude. To understand the trend of ΔV_{mean} as a function of FET width, the variation of the individual trap induced threshold voltage shift ΔV_{tr} must be considered (fig. S11). For the suspended FET, ΔV_{mean} approximately follows the expected $1/A$ trend across the entire width range. This is expected from the symmetric impact of traps across the FET surface. For the embedded FET, ΔV_{mean} slightly exceeds the $1/A$ trend due to the increased impact from the traps at the passivated sidewalls. For the suspended and embedded FET, this results in the ~$1/\sqrt{A}$ noise amplitude scaling trend reported in the main text (fig. 12). For the tri-gate FET, ΔV_{mean} only follows the $1/A$ trend for large widths (> 200 nm) but starts to saturate for smaller widths. The saturation for small widths is attributed to a decreased fraction of the passivated bottom surface where the gate capacitance is lower and traps have a higher impact (fig. S11). For smaller FET heights this fraction of the bottom surface is less influenced by width downscaling. Therefore, the saturation of ΔV_{mean} when downscaling the tri-gate FET width is less outspoken for smaller FET heights (fig. S10b).

Furthermore, for wide tri-gate FETs (> 50 nm) and embedded FETs, ΔV_{mean} and the noise amplitude counterintuitively decrease for FETs with a lower height (fig. S10a). This is attributed to the decrease of the trap impact at the side and bottom surfaces (fig S11bc) due to an increase of the overall gate capacitance or electrostatic control. Moreover, the ΔV_{mean} of the tri-gate FET equals the ΔV_{mean} of the embedded FET (fig. S10a) for large FET widths when the tri-gate and embedded FET architectures become equivalent. For small FET widths, the tri-gate and suspended FET architectures become equivalent and the ΔV_{mean} values become similar.

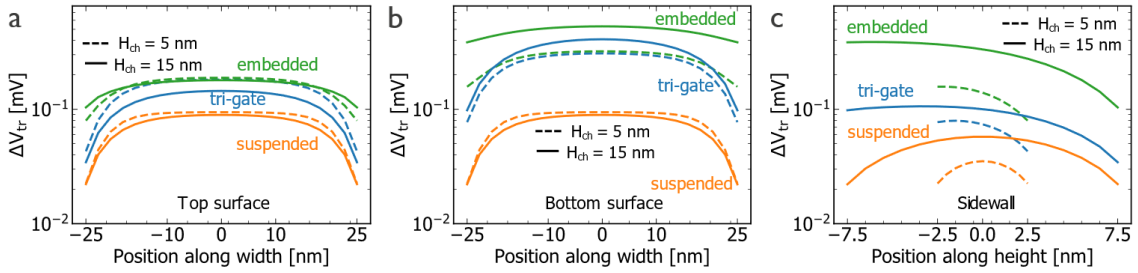

Figure S11. a, b and c) The single trap induced threshold voltage shift ΔV_{tr} as a function of the position along the FET perimeter in the center of the channel (z =0). a, b and c) show the values for the top surface, bottom surface and sidewall respectively. Results are shown for the three different FET architectures with W_{ch}×H_{ch} = 10×5 nm^2 and a 15 mM ionic strength of the electrolyte. The gate length is 600 nm. V_{GS}-V_T = 100 mV.

Second, we elaborate on the mean normalized trap density $N_{tr,norm}(E_F)_{mean}$ as a function of FET width (fig. S10b). As we have shown earlier, the trap density is larger at a passivated surface close to the source-drain regions due to a decrease of the Fermi level energy. Downscaling the FET width reduces the fraction of the top and bottom surfaces while increasing the fraction of the sidewalls. For the tri-gate FET, downscaling thus leads to a reduced contribution of the bottom surface where the trap density is higher (fig. S9). This effect is more pronounced for higher FETs and is expected to result in the initial decrease of the mean trap density at moderate FET widths of about 50 nm (fig. S10b). On the other hand, for the embedded FET, the trap density is higher at the passivated sidewalls compared to the gated top surface (fig. S9). When scaling down the FET width, the increased contribution of the passivated sidewalls leads to an increase of the mean trap density at moderate FET widths of about 50 nm (fig. S10b).

Finally, for all FET architectures, the Fermi level significantly decreases for small FET widths and heights (fig. S12b). Figure S12c shows that the variation of the Fermi level along the perimeter of the channel is small and cannot explain the observed trend. The Fermi level is most negative at the corners and the least negative in the center of the passivated bottom surface. This agrees with the gate capacitance which is higher at the FET corners and smaller at the passivated surfaces. A higher local gate capacitance enhances electrostatic gating locally and induces a stronger local band bending in the channel, i.e. a more negative Fermi level. For small cross-sections, a more negative Fermi level originates from the more negative gate bias that is needed to accumulate holes in the channel i.e. a more negative threshold voltage is obtained (fig. S12d). This is a direct result of the density gradient model which prevents the accumulation of holes close to the oxide interface. Remember that we operate the FET at 100 mV underdrive. The significant decrease of the Fermi level results in a larger density of traps for small FET widths and heights smaller than 10 nm. This explains the increase in noise amplitude for the smallest FET cross-sections (fig. 12a).

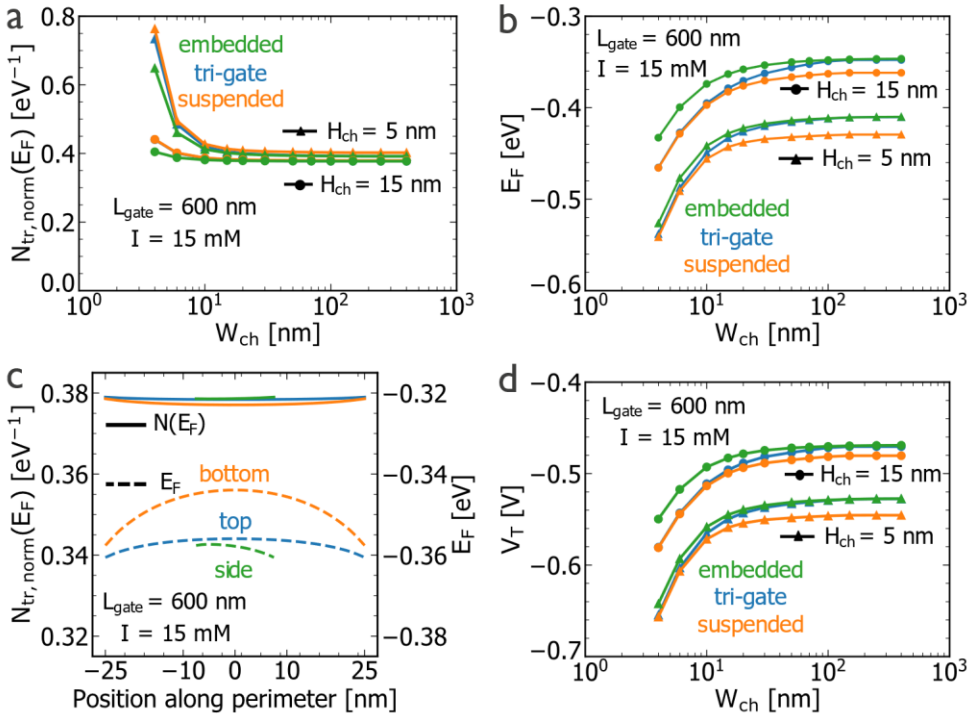

Figure S12. a,b) The normalized trap density $N_{tr,norm}(E_F)$ and the Fermi level energy as a function of the FET width for three different FET architectures with 5 nm and 15 nm FET height. Fermi level and normalized trap density are shown for the top center of the device (x,y,z = 0). c) The normalized trap density $N_{tr,norm}(E_F)$ (solid lines) and the Fermi level energy (dashed lines) along the perimeter in the center of the FET (z = 0). Blue, orange and green colors indicate the position of the trap at the top, bottom and side surface respectively. d) The threshold voltage as a function of FET width. V_{GS}-V_T = 100 mV.

8. Impact of ionic strength on FET noise

In the main text, we first elaborate on the trap signal or trap-induced threshold voltage shift to better understand the molecule signal. Second, the trap signal also strongly influences the FET noise amplitude. Here, we show that a reduction of the electrolyte ionic strength can somewhat increase the trap induced threshold voltage shift ΔV_{tr} and the resulting ΔV_{mean} (fig. S13ab). The increase in ΔV_{tr} for a reduced ionic strength I is explained by a decrease of the double-layer capacitance $C_{DL} = \varepsilon_0 \varepsilon_w / \lambda_D$ with ε_w the dielectric constant of water and $\lambda_D \propto 1/\sqrt{I}$ the Debye length. Since the electrolyte double layer capacitance is in series with the gate oxide capacitance $C_{ox} = \varepsilon_0 \varepsilon_{ox} / t_{ox}$, the effective gate capacitance $1/C_g \approx 1/(C_{ox} + C_{DL})$ decreases when the ionic strength reduces. Consequently, $\Delta V_{tr} \approx q/C_g$ increases for lower ionic strengths. However, this effect is only noticeable when the double layer capacitance is of the same order or smaller compared to the oxide capacitance. Since the dielectric constant of water is about 78 which is much smaller than the dielectric constant of 3.9 for SiO_2, the oxide capacitance is typically lower and dominates the gate capacitance. This is observed by the small difference in magnitude of ΔV_{tr} between the metal gated ($C_{metal} \approx \infty$) FET and the liquid-gated FETs with ionic strengths equal to 15 and 150 mM respectively. For an electrolyte ionic strength of 1.5 mM (λ_D= 7.8 nm) the double layer capacitance approaches the oxide capacitance resulting in a more pronounced increase of ΔV_{tr} and ΔV_{mean} (fig. S13ab). Here, we simulated bioFETs with an oxide thickness of only 1 nm. Typical bioFETs have thicker gate oxides for which the impact of the ionic strength on the trap-induced threshold voltage shift will be even lower. Lastly, the trend of ΔV_{mean} as a function of width and gate length does not significantly change with a varying electrolyte ionic strength.

Next, a reduction of the ionic strength also somewhat increases the mean normalized trap density $N_{tr,norm}(E_F)_{mean}$ (fig. S13cd). Remember from the impact of the surface passivation that a reduced gate capacitance can decrease the Fermi level at the source-drain junctions and increases the mean normalized trap density. The increase for lower ionic strengths is thus expected from the reduction of the gate capacitance. Again, the trend for the mean normalized trap density as a function of width and gate length does not change with a varying electrolyte ionic strength.

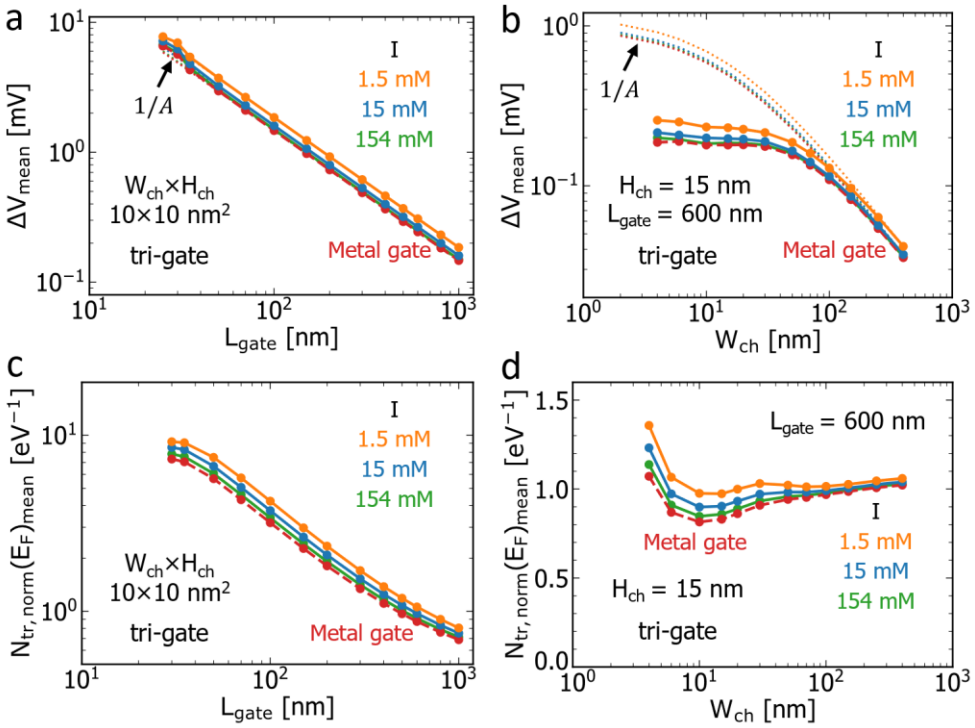

Figure S13. a, b) The mean trap threshold voltage shift ΔV_{mean} as a function of FET gate length and width for different electrolyte ionic strengths and a metal gated FET (dashed line). The $1/A$ trends are indicated with A = 2×(W_{ch} + H_{ch})×L_{gate} the FET interface area. c, d) The mean normalized trap density $N_{tr,norm}(E_F)_{mean}$ as a function of FET gate length and width for different electrolyte ionic strengths I. V_{GS}-V_T = 100 mV.

9. Impact of gate length on cross-section scaling

In figures S14ab, we show the impact of cross-section scaling on the single-molecule signal for FETs with a gate length of 50 and 600 nm. As expected, the signals for a 50 nm gate length are significantly increased compared to the signals for 600 nm long FETs. However, the scaling trends for the long and short FETs are almost identical. Consequently, the optimal cross-section that maximizes the single-molecule signal is not significantly affected by the gate length of the FET sensors. The same holds for the FET noise amplitude (fig. S14cd). The noise trends as a function of the cross-section do not significantly change for a reduced gate length. Naturally, this results in a similar single-molecule SNR scaling trend for short and long gate lengths respectively (fig. S13ef). Therefore, we can conclude that the optimal cross-section for single-molecule detection does not significantly depend on the gate length of the FET sensor.

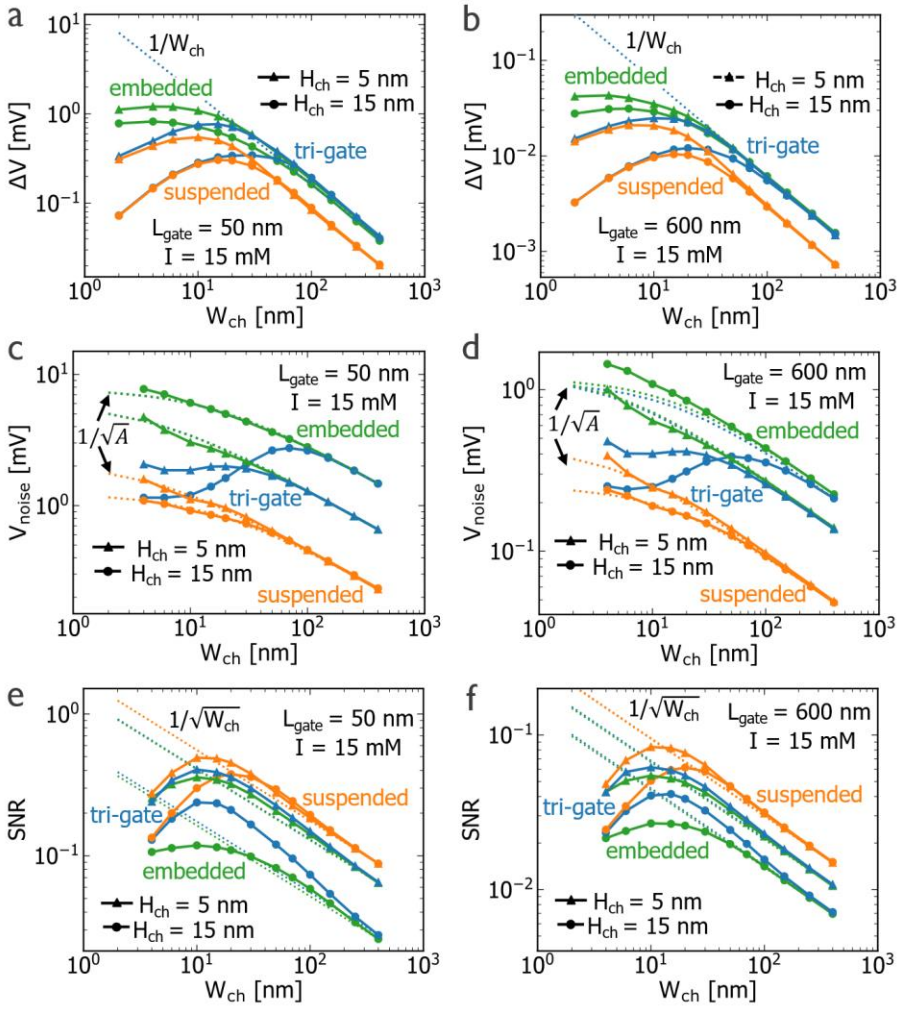

Figure S14. The single-molecule signal, noise amplitude and single-molecule SNR as a function of the channel width for FETs with a 50 nm (a,c,e) and 600 nm (b,d,f) gate length respectively. Triangles and circles indicate a channel height of 5 and 15 nm respectively.

10. Impact of channel carrier mobility and model on geometry scaling trends

The impact of the channel carrier mobility and the mobility model on the single-molecule signal scaling trends are investigated. Two mobility models are considered: the standard GTS TCAD MM6 mobility model (solid line fig. S15)[6,7] and a constant mobility model (dashed line fig. S15). The single-molecule signals are simulated for hole mobilities equal to 200 (orange line fig. S15), 460 (blue line fig. S15) and 1000 cm^2/Vs (green line fig. S15). Figure S15a and S15b show the singularly charged single-molecule signals as a function of gate length and channel width respectively. Equal signal magnitudes and geometry scaling trends are obtained for the different models as well as the different hole mobilities.

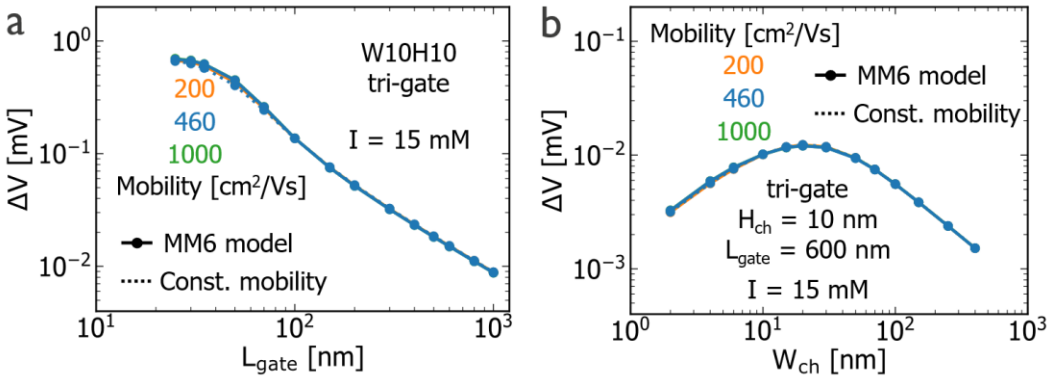

Figure S15. a,b) The single-molecule signals as a function of gate length and channel width of a tri-gate FET. Dashed lines: constant mobility model. Solid lines: GTS TCAD MM6 mobility model. Orange, blue and green lines represent hole mobilities of 200, 460 (default) and 1000 cm^2/Vs. The electrolyte ionic strength is 15 mM. V_{GS}-V_T = 100 mV.

11. Impact of pH sensitivity on geometry scaling trends

Here, we show the impact of the pH sensitivity of the oxide surface on the geometry scaling trends for the single-molecule signal. To model the pH sensitivity of the gate oxide, we apply the Shockley-Read-Hall (SRH) interface trap model of the TCAD simulator at the gate oxide-electrolyte interface. The interface charge density is given by: $Q_{int} = \pm qN_T f$ with q the elementary charge. The interface charge density Q_{int} is negative for an acceptor-type trap and positive for a donor-type trap. N_T represents the trap surface density and f is the trap occupancy function:

$$f = \frac{1}{1 + exp\left(\frac{E_T - q\Psi_0}{kT}\right)}$$

Here, E_T represents the trap level energy and Ψ_0 the potential at the oxide surface referenced to the bulk electrolyte potential at the gate contact. k and T are the Boltzmann constant and the temperature. We have previously shown that this model is equivalent to the site-binding model which is typically used to describe the pH sensitivity of an oxide surface.[8] The first requirement is that the trap surface density N_T must equal the oxide silanol group density. The second requirement is that the trap level energy E_T must be selected equal to $2.3kT\ (pK - pH)$. Here, pK represents the pK value of the oxide surface silanol groups and $pH = -\log_{10}[H_3O^+]$ is the bulk pH value with $[H_3O^+]$ the bulk hydronium concentration. In the simulations reported here, we consider a neutral pH of 7. Since we simulate a SiO_2 gate oxide which becomes negatively charged for pH values exceeding 2, the assumption of a single pK or trap energy level is validated. Acceptor type traps are used to obtain a negative oxide surface charge. Notice that it is not required that the hydronium ion distributions are calculated in the electrolyte segment when employing this model. The self-consistent calculation of the trap occupancy function and the local potential at the oxide-electrolyte interface Ψ_0 ensure the pH dependence of the surface charge.

The blue lines in figure S16 represent the single-molecule signal without assuming oxide surface charges as also shown in the main text (fig. 10). This signal is the highest as it is not affected by nonlinear screening or the pH interference effect.[9] The pH sensitivity of the oxide surface groups

is described by the model described above assuming only the deprotonation reaction of the surface groups.[9,10] We calculate the single-molecule signal using a pK of 4.5 and a surface group density of 4×10^{13} cm^{-2} (orange curves). Also, we calculate the single-molecule signal assuming a fixed oxide surface charge of -3.7×10^{13} q/cm^2 (green curves). This is the oxide surface charge density that is obtained for the site-binding model at a planar surface. The molecule charge changes the pH locally which induces counter charges at the pH-sensitive oxide surface, i.e. the pH interference effect. [9] Consequently, the single-molecule signal reduces about 13% for a pH-sensitive surface (orange curve) compared to the oxide surface with a fixed charge (green curve). However, the observed geometry scaling trends are approximately equal for both models. In other words, the pH sensitivity of the oxide surface is not expected to significantly influence the optimal geometry that maximizes the single-molecule signal.

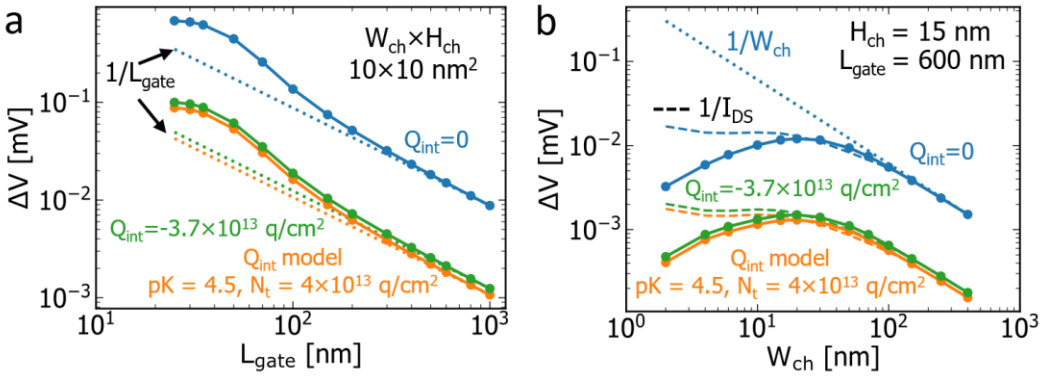

Figure S16. a,b) The single-molecule signals as a function of gate length and channel width of a tri-gate FET. Blue lines: no oxide surface charge. Green lines: fixed oxide surface charge density equal to the charge density of the full site-binding model (-3.7×10^{13} q/cm^2). Orange lines: pH-dependent oxide surface charge using site-binding model with pK of 4.5 and a trap density N_t of 4×10^{13} cm^{-2}. The electrolyte ionic strength is 15 mM and the pH is 7. V_{GS}-V_T = 100 mV.

12. Impact of recognition molecule on FET signal and geometry scaling trends

In the main text, we initially assume the direct binding of the single target molecule to the FET sensor surface with a distance or linker length of 1 nm. However, the selective detection of target molecules often requires the usage of recognition molecules on the FET surface. Here, we study the impact of such a recognition or probe molecule on the single-molecule signal and geometry scaling trends. More specifically, hybridization with a DNA and PNA probe is investigated to show the impact of the probe molecule's charge. The influence of the distance of the target molecule to the surface is investigated to identify the impact of the size of the biorecognition molecule.

A commonly targeted molecule in medical diagnostics is DNA. Therefore, to study the impact of the probe molecule's charge, we consider the binding or hybridization of a 15-base single-stranded DNA oligo (15b DNA) to both a neutral complementary peptide nucleic acid (PNA) probe and a negatively charged DNA probe. For both detection schemes, we assume a 1 nm linker length which determines the distance of the probe and target molecule to the FET surface. The volumes of the PNA and DNA probes and the hybridized complexes are assumed identical and are modeled by a dielectric box with a height of 5 nm and width and depth of 2 nm.[11] The charge density is selected accordingly to acquire the correct number of elementary charges in the dielectric box. More specifically, the volume charge density equals -7.5×10^{20} q/cm^3 for the DNA probe and the hybridized DNA-PNA complex and equals -1.5×10^{21} q/cm^3 for the hybridized DNA-DNA complex (-7.5×10^{20} q/cm^3 for 15 bases). The molecule dielectric box is placed above the center of the FET and has a dielectric constant of 5. We consider the optimized 10×5 nm^2 ($W_{ch}\times H_{ch}$) suspended FET architecture to calculate the hybridization signals.

For DNA-PNA hybridization in a 15 mM electrolyte, the signal varies from 0.066 mV to 4.7 mV for a 1000 nm and 35 nm long gate length respectively (fig. S17a). Due to additional nonlinear

screening induced by the negatively charged DNA probe, the signal for DNA-DNA hybridization is reduced to 0.026 and 1.8 mV for the long and short FET respectively. The more than 2-fold increase in signal when using PNA probes instead of DNA probes indicates the preference for neutral PNA probes over traditional DNA probes for DNA sensing. No significant impact of the PNA or DNA probes is observed on the gate length scaling trends. Moreover, in a 1.5 mM electrolyte, the simulated PNA-DNA hybridization signal for a gate length of 35 nm is boosted to 15 mV.

Next, we calculate the SNR values for various gate lengths by including bioFET noise. We initially consider our bioFET noise power density of 500 $\mu V^2\mu m^2/Hz$ at 1 Hz and integrate over a frequency range from 1 Hz to 1 kHz (see also methods main text). In a 15 mM electrolyte, this results in a DNA hybridization SNR of 0.13 and DNA-PNA hybridization SNR of 0.35 for a micron long FET (fig. S17b). For a 35 nm long FET, the SNR values for DNA-DNA and DNA-PNA hybridization respectively increase to 1.2 and 3.2. Furthermore, decreasing the electrolyte ionic to 1.5 mM results in a sufficient DNA-PNA hybridization SNR of about 10 and can even be boosted further to 28 by considering a commercial solid-state FET noise level (50 $\mu V^2\mu m^2/Hz$ at 1 Hz). These results indicate the potential to realize a DNA screening platform with a single-molecule resolution using nano-scaled silicon FETs.

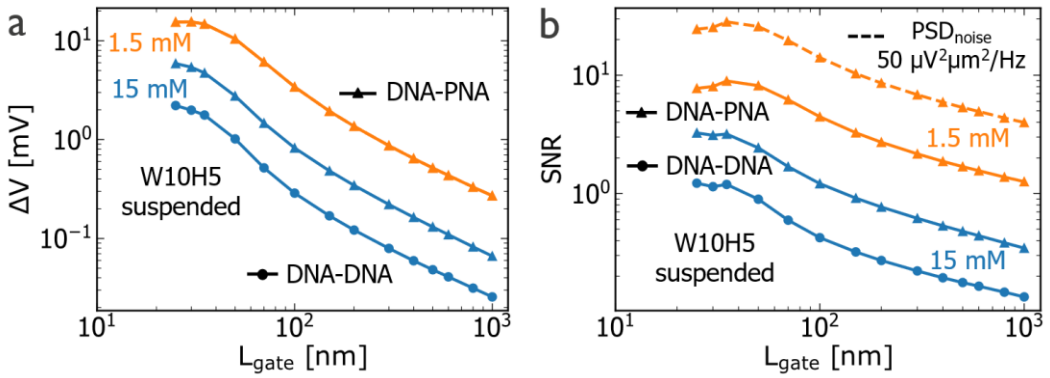

Figure S17. a,b) The single-molecule DNA-DNA (dots) and DNA-PNA (triangles) hybridization signals and SNR values as a function of gate length for a suspended FET with 10×5 nm^2 cross-section. Orange and blue lines correspond to 1.5 mM and 15 mM electrolyte ionic strengths respectively. In b) solid and dashed lines represent SNRs assuming a 500 $\mu V^2\mu m^2/Hz$ and 50 $\mu V^2\mu m^2/Hz$ noise power spectral density respectively.

Detecting other types of target molecules typically requires different types of recognition molecules like antibodies, nanobodies, aptamers etc. which can vary significantly in size and alter the distance of the target molecule to the FET surface. To study the impact of the molecule distance on the magnitude of the signal and the geometry scaling trends, we again use our standard model system consisting of a singularly charged molecule placed above the center of a tri-gate FET (see main text). As expected, our simulations show that small recognition molecules resulting in smaller distances boost the single-molecule signal by limiting electrolyte screening (fig. S18ab). A decrease of the target molecule's distance to the surface from 4 nm to 0 nm results in a 6-9 fold increase of the signal which depends on the geometry of the FET channel. Nanobodies are thus preferred over the larger antibodies as biorecognition elements. Here, we must also mention that our simulations do not incorporate the dielectric volume of these probe molecules. As such electrolyte screening is overestimated. Moreover, polymer layers can be used to limit electrolyte screening for larger recognition molecules.[12]

On the other hand, the smaller the molecule distance to the FET surface, the smaller the modulated channel region becomes. As such, smaller molecule distances somewhat decrease the negative impact of the source-drain junctions for gate length scaling and the convex FET corners for width scaling. When the molecule binds closer to the surface, this directly results in a somewhat weaker saturation of the signal for short gate lengths (fig. S18a) but also results in a somewhat smaller optimal channel width (fig. S18b). More specifically, the channel width that maximizes the single-molecule signal reduces from 20 nm to 15 nm when the molecule distance reduces from 4 nm to 0 nm.

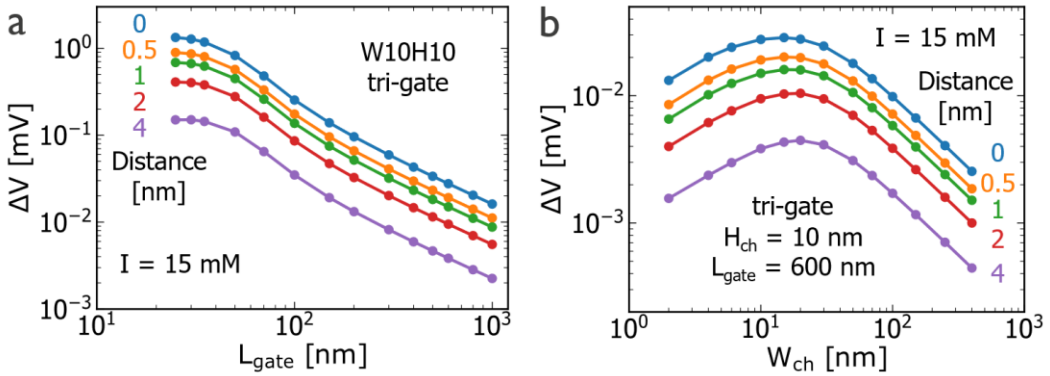

Figure S18. a,b) The singularly charged single-molecule signals as a function of gate length and channel width for a tri-gate FET. Colors indicate different distances of the molecule to the FET surface. The electrolyte ionic strength is 15 mM.

13. TCAD simulation of single-molecule experiments

Detection of single F1-ATPase molecules[13] and the monitoring of single hairpins[14] using silicon nanowire FET sensors has been reported. Here, we compare these experimental results with the predicted signal from our TCAD model which has been successful in quantitatively describing the experimental signal of a layer of DNA molecules binding to the FET surface.[9,15] We simulate silicon p-type FET sensors with a cross-section of 20 by 20 nm with micron-scale lengths mimicking the bottom-up silicon nanowires used by Li et al. (fig. S19 right) but also include shorter FETs with nano-scaled gate lengths. A constant doping density of 1×10^{17} cm^{-3} is considered and a SiO_2 gate oxide thickness of 5 nm is selected. No pH-dependent or fixed FET surface charges are assumed that further degrade the signal due to the pH interference effect and nonlinear screening.[9] The relative drain current signals are extracted from the simulated I_{DS}-V_{GS} curve with a source-drain bias of 100 mV in the subthreshold region.

First, we simulate the F1-ATPase binding experiment. The ionic strength is set to 30 mM to mimic the experimental conditions. The F1-ATPase protein is modeled as a 10 nm-sized dielectric cube with a dielectric constant of 5 and is positioned above the center of the FET (fig. S19 right). A continuous molecule charge density is selected to match the predicted net charge of -92 at a pH of 8 (calculated from http://protcalc.sourceforge.net/). The distance between F1-ATPase and the FET oxide surface is 2 nm which represents the length of the functional layer and linker. Initially, we assume the first 1 nm of this layer to be inaccessible to electrolyte ions. As such this layer is modeled as a dielectric layer with a dielectric constant of 40 (orange curve fig. S19 left). Further away from the surface (> 1 nm), electrolyte ions can move freely and lead to electrolyte screening. The simulated signals, expressed as relative drain current change, range from 0.1% to 0.3% for FETs with a gate length of 3 and 1 µm respectively (orange curve fig. S19 left). These signals are several orders of magnitude lower compared to the experimentally reported signal of 20% for an approximately 3 µm long FET (green star fig. S19 left). To check the impact of the functional layer model on the signal, we also show the most optimistic scenario where the entire functional layer is modeled as a pure dielectric layer, i.e. no electrolyte screening occurs between 0 to 2 nm from the FET's surface (blue curve fig. S19 left). The simulated signal increases to 0.47% for a FET with 3 µm gate length but is still more than an order of magnitude lower compared to the experimental signal. However, for the shortest simulated gate length of 50 nm, the single F1-ATPase signal reaches up to 34%.

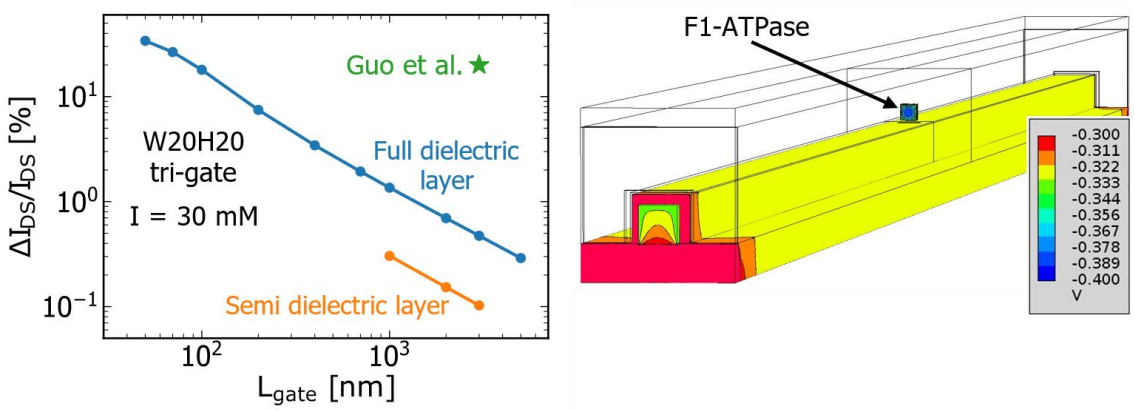

Figure S19. Left: The measured single F1-ATPase signal (green star) compared to the simulated F1-ATPase signals (solid lines) as a function of gate length. Orange and blue lines indicate respectively simulations with half of the functional layer and the complete functional layer modeled as a dielectric. Right: Potential distribution in a simulated tri-gate FET architecture with F1-ATPase molecule. The ionic strength is 30 mM.

Next, we include the FET noise amplitude based on an area normalized noise power density of 500 $\mu V^2\mu m^2/Hz$ at 1 Hz over a frequency range from 1 Hz to 1 kHz.[16] Considering this state-of-the-art bioFET noise level, the noise amplitude is calculated using the approach described in the main text (see signal-to-noise ratio calculation in the experimental section of the main text). The calibration is done for the bioFET structure with 20×20 nm^2 cross-section and 3 µm gate length. The Li et al. F1-ATPase SNR based on the experimental signal becomes 35 for a 3 µm long FET (green star fig. S20). In contrast, assuming the full dielectric functional layer, the SNR based on the simulated signal amounts to only 0.8 for a 3 µm long FET. Signals resulting in such low SNR values are typically not detectable. However, a sufficient SNR of about 7 can be obtained for a FET with a 50 nm gate length. This again indicates the importance of downscaling the gate length to boost the single-molecule detection capabilities of a silicon FET sensor.

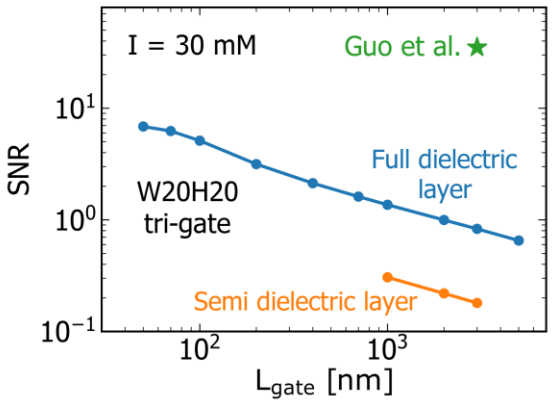

Figure S20. The measured single F1-ATPase SNR (green star) compared to the simulated F1-ATPase SNR values (solid lines) as a function of gate length. Measured and simulated SNR values are calculated assuming state-of-the-art electrolyte-gated FET noise power density of 500 $\mu V^2\mu m^2/Hz$. Orange and blue lines indicate respectively simulations with half of the functional layer and the complete functional layer modeled as a dielectric.

Second, the opening and closing of a 25-base DNA hairpin resulting in a discrete random telegraph signal have been proposed to explain an experimental signal.[14] For simplicity, we simulate the direct binding of the complete DNA hairpin to the FET surface which gives an upper bound on the expected signal. The hairpin molecule is modeled as a 4 nm high dielectric box with 2 nm width and depth and a dielectric constant of 5. The functional layer of 2 nm is again modeled as a pure dielectric layer and the electrolyte ionic strength is 10 mM. For a 3 µm long silicon FET as used in

He et al.'s work, our model with optimistic model parameters predicts a DNA hairpin binding signal of only 0.1 % (blue curve fig. S21 left). This signal is more than an order of magnitude lower compared to the reported signal of about 6 % for the opening and closing of the DNA hairpin (green star fig S21 left). Including FET noise (500 $\mu V^2 \mu m^2/Hz$), the SNR for DNA hairpin opening and closing based on the experimental signal becomes approximately 10 (green star fig. S21 right), whereas the SNR using the simulated signal only reaches a value of 0.18 for a 3 µm long silicon FET (blue curve fig. S21 right). Even for the shortest gate length of 50 nm, the simulated hairpin SNR of 1.15 is below the typical detection limit.

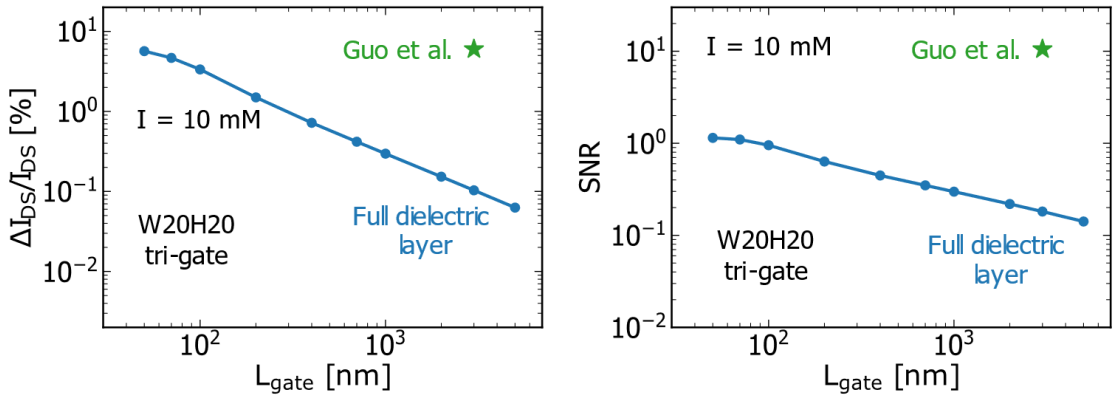

Figure S21. Left: The measured single hairpin signal (green star) compared to the simulated hairpin signals (solid line) as a function of gate length. Right: The single hairpin SNR (green star) compared to the simulated hairpin SNR values (solid line) as a function of gate length. SNR values are calculated assuming state-of-the-art electrolyte-gated FET noise power density of 500 $\mu V^2 \mu m^2/Hz$. The complete functional layer is modeled as a dielectric. The ionic strength is 10 mM.

We conclude that the reported single-molecule signals in the work of Li et al. (F1-ATPase) and He et al. (hairpin) are typically several orders of magnitude larger than expected based on our TCAD model. Our model successfully explained the experimental signal for a layer of many DNA molecules binding to a FET surface. For single-molecule experiments, discrete dopant effects, which are not considered in our model, could for example result in a larger variation of the single-molecule signal. However, a systematic increase of the signal by several orders of magnitude compared to the average signal that we simulate here is unlikely.[3] Our model captures the electrostatic effect that charged molecules modify the local concentration of mobile charge carriers in the channel. Therefore, this large offset between the reported experimental signals and our simulated signals indicates that the experimental signals cannot be explained by a pure electrostatic effect from the molecule's charge.

Furthermore, the sign of the reported hairpin signal is opposite to what is expected from an electrostatic effect. The closer presence of the negatively charged hairpin to the FET reduces the drain current whereas electrostatically an increase in drain current is expected due to the accumulation of holes in p-type FETs. A mobility-degrading scattering effect is suggested.[14] However, this effect is unlikely to be significant when a non-ballistic, drift-diffusion transport regime is present such as in long silicon FETs.[17] Also, note that for the binding of the negatively charged F1-ATPase a drain current increase is reported which does agree with an electrostatic effect. Further work could elucidate the encountered contradictions between the reported single-molecule sensing experiments and our model. Our work provides a path towards the unambiguous realization of single-molecule sensing with silicon FETs in quantitative agreement with a physical model.

14. Overview of model parameters

Table 1: Overview of the model parameters including the default values.

Parameter	**Default value**
Gate length, L_{gate}	600 nm
Channel width, W_{ch}	10 nm
Channel height, H_{ch}	10 nm
Gate oxide thickness, T_{ox}	1 nm
Source-drain region length	20 nm
Donor channel doping, N_D	1×10^{17} cm^{-3}
Acceptor source-drain doping, N_A	2×10^{20} cm^{-3}
Standard deviation of Gaussian source-drain doping profile, σ	3 nm
Electron mobility channel, MM6 model	1430 cm^2/Vs
Hole mobility, MM6 model	460 cm^2/Vs
Ionic strength, I	15 mM
Bulk ion concentration, c_0	15 mM
Ion valency, z_i	1
Hydrated ion diameter, a	0.6 nm
Electrolyte dielectric constant	78
Molecule distance to FET surface	1 nm
Molecule size	1 nm^3
Molecule volume charge density	1×10^{21} cm^{-3}
Density of hydroxyl surface groups, N_T	4×10^{13} cm^{-2}
pK of hydroxyl surface groups, pK	4.5
pH	7
Fixed gate oxide-electrolyte interface charge, Q_{int}	0 q/cm^2

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