Degradation mechanisms in Germanium Electro-Absorption Modulators

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***Abstract*—Reliability analysis on Ge Electro-Absorption Modulators suggest that different physical mechanisms are involved in the dark current degradation during electrical stress. An "incubation time" followed by a power-law dependent dark current increase suggests the filling of pre-existing defects and the creation of traps at the Ge/Si and Ge/Ox interface. Even though the dark current degrades during reliability testing, actual failures are not expected to happen at nominal operation conditions and times. Finally, performance evaluation after more than 4000h of electrical stress, reveals no degradation of the electro-optical parameters.**

***Index Terms*-- Electro-absorption modulator, Dark current degradation, Lateral p-i-n diode, Reliability, Silicon photonics**

I. Introduction

The exponential growth of data applications and the continuous demand for high-performance computing systems [1], has resulted to a bottleneck reach of the standard copper interconnects. From long distance communication [2] to sensors and imagers, the answer to this "problem", over the last decade, has been the industry's transition to Silicon Photonics (SiPho). The biggest advantage of SiPho is the manufacturing capability, in the existing - and mature - complementary metal oxide semiconductor (CMOS) platforms [3], [4]. Over the years, it has proven to be a scalable, cost-effective and with high yield technology, that allows monolithic integration of Silicon (Si) and Germanium (Ge) on a Si wafer [5].

One of the key building blocks, used to send data in the optical domain deploying a silicon photonics integrated circuit (PIC) [6], are the optical modulators. Among them, the Ge Electro-Absorption Modulator (EAM), that exploits the Franz-Keldysh (FK) effect, according to which the absorption coefficient near the band edge is increased due to band-tilting caused by an applied electric field [7] and is beneficial for enabling high-speed modulation in the L-band for optical communication [7]. For these components, a guaranteed electrical and electro-optical performance during normal operation is crucial, with misfit defects at the Ge/Si interface, dislocation defects in the Ge layer and surface defects due to improper passivation being the main sources of low signal-to-noise ratio [8]. As a result, the degradation of the dark current, I_{dark}, due to trap filling and/or the creation of new defects is a concern here, as reported earlier on GeSi EAMs [9].

The goal of this work is to investigate the dark current degradation mechanisms of pure Ge EAMs, over an extensive set of measurements and attempt to better understand its origin. Section II describes the design of experiments, including device configurations and measurement procedures. Short and long voltage stress results are presented in Section III, along with Human Body Model (HBM) tests and performance evaluation after electrical stress. A new semi-empirical fitting methodology of the I_{dark} degradation is presented that allows lifetime predictions to the use conditions. Finally, key points and conclusions are summarized on Section IV.

II. Devices and Stress Procedure

The Ge EAMs used in this study are lateral p-i-n diodes fabricated in imec's iSiPP25G Si Photonics platform, which is based on 200 mm Silicon-On-Insulator (SOI) wafer with 220nm top Si layer on 2μm thick Buried Oxide (BOX). Ge was grown using Selective-area Epitaxial Growth (SEG), followed by an annealing step to decrease the threading dislocation density [10]. After Chemical Mechanical Polishing (CMP), the final Ge thickness reached 350nm and the annealing temperature used to activate the dopants was 550°C [7]. A detailed cross-section is shown in Figure 1, indicating the p-type and n-type ion implants for both Ge and Si.

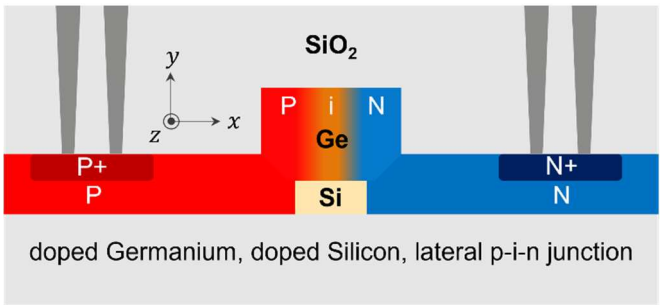

Figure 1. Cross-section illustration of the lateral p-i-n Ge EAM, used for high-speed modulation (L-band).

Three different geometries (S1 to S3) with variations on length and width of the Ge (Table I) were used for this work, for short and long stress time duration. For the short-term stress, only S3 structure was studied, while for the long-term part, all three of them were stressed and analyzed.

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TABLE I. DESIGN OF EXPERIMENTS USED IN THIS WORK

Structure name	Width [um]	Length [um]
S1	0.5	49.6
S2	0.6	40.0
S3	0.5	81.6

In the first part, for the short term stress measurements, we apply the Bias Temperature Stress (BTS), a wafer-level test methodology presented in [11]. It is a combination of constant voltage stress (at elevated temperatures) and I-V sweep sense (from 0V to -2.5V) measurements. The stress temperatures and voltage conditions are presented in Fig. 2, while the stress time is ~60h for each combination. This methodology enables more understanding of the conduction and degradation mechanisms in our Ge EAM devices.

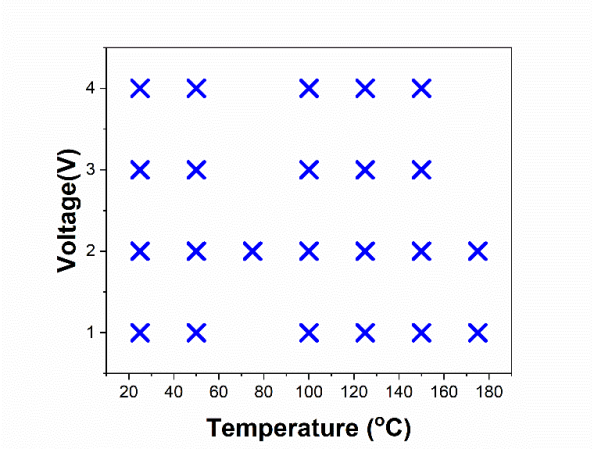

Figure 2. Test conditions used during Bias Temperature Stress (BTS) tests.

In the second part, long term voltage stress results, on all diode variations, will be discussed. Accelerating aging as described in [9], is applied over a wide range of test conditions (125°C/150°C/175°C/200°C and 85°C/85%RH), monitoring the I_{dark} degradation, during T_{stress} and T_{op}, for up to 5000h of stress time. Since the damp heat test is taking place in the data treatment/operating temperature, we will not report the dark current values. Nevertheless, the devices stressed in this condition, will also be included in the electro-optical performance evaluation results, in Section III.D.

III. RESULTS AND DISCUSSION

A. Electric field modeling

In order to better understand possible damage locations, using Sentaurus™ TCAD software, we simulated the diode operation at -2V, the nominal voltage in order to use these components as EAMs [12]. From *sprocess* [13] and *sdevice* [14] modules, we extracted the electric field of the device, giving us an indication on where the defect generation process could be located. Looking at the cross-section in Fig. 3 and the highest values of the e-field, it is clear that the most affected regions are expected to be the Ge/Si and the Ge/Ox interface.

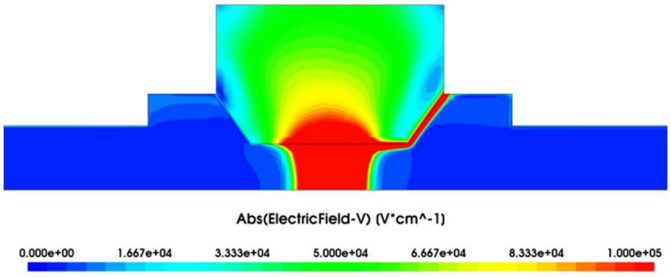

Figure 3. Electric field simulation at -2V, for S1, where the highest values are obtained at the Ge/Si and Ge/Ox interface. Similar results were obtained for S2 and S3 and are therefore not shown in this work.

B. BTS results

Performing an initial characterization with current-voltage (I-V) sweeps at various temperatures, is the first step towards the activation energy extraction. However, I_{dark} trends versus temperature, of our structures, show that the Arrhenius relation $I \sim e^{\frac{-E_A}{k_b T}}$ [15] does not apply [11] and thus, local E_A's had to be calculated showing different conduction mechanisms to be present, at different voltage and temperature combinations (Fig. 4). Without clear boundaries, for lower temperatures the Shockley-Read-Hall process (~0.33eV) is more dominant. On the contrary, at higher T's, the diffusion (~0.66eV) process starts taking over.

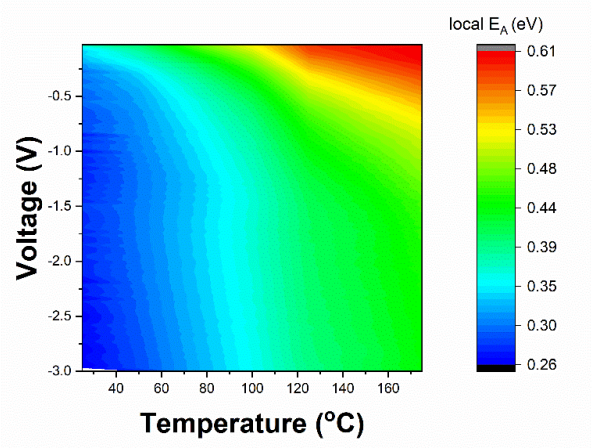

Figure 4. Local activation enegry E_A obtained at various voltages and temperatures shows different conduction mechanisms, not complying with the Arrhenious law.

Following the methodology of [11], we evaluated the change of sense leakage current for different stress conditions. We expect a negative change of sense current to represent carrier trapping in defects/traps, while a positive change is related to the creation of new defects/traps. As shown in Fig. 5, for most of the stress conditions (with given local E_A of the I_{dark} at stress condition), the rate of sense current change is observed to be negative at -1V, suggesting that the filling of the traps is significant at this voltage [11].

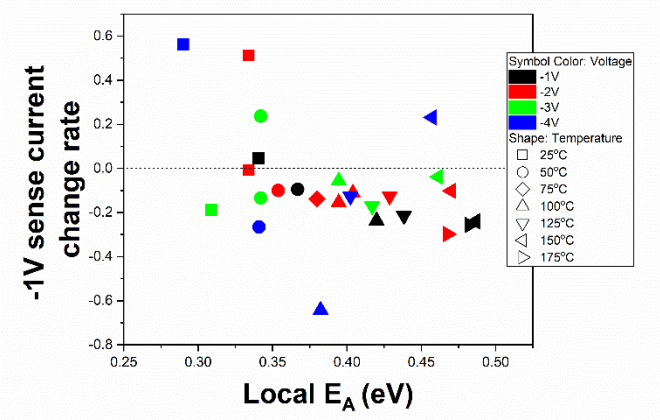

Figure 5. Sense leakage current change rate obtained at -1 V vs. local E_A of the I_{dark} at stress condition.

From contour maps (Fig. 6) representing the slopes of sense current change versus stress (temperature and voltage on X and Y axis) and sense conditions in (a) and (b) for -1V and -2.5V, respectively it is evident that defect generation and defect filling are simultaneously present, where one of the two is dominant.

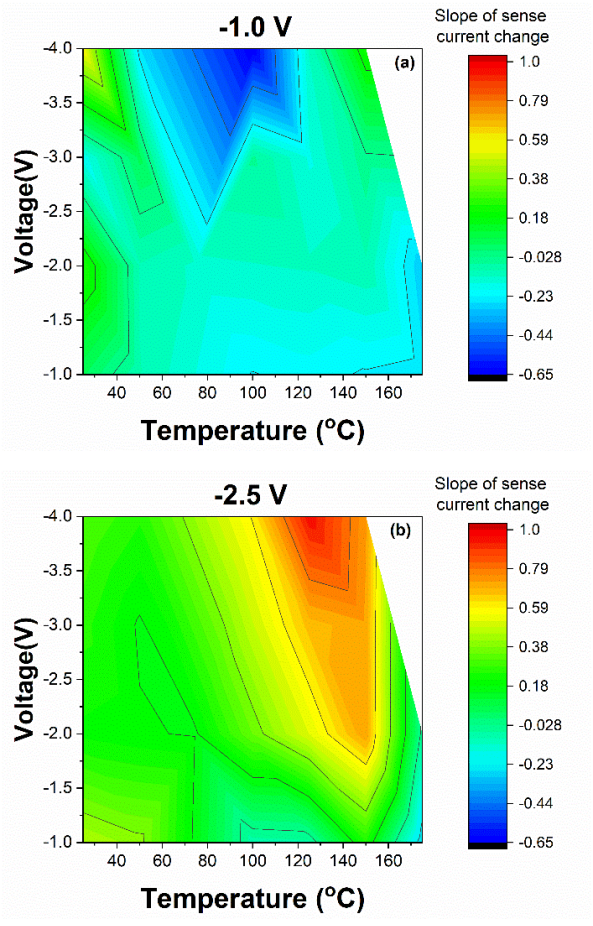

Figure 6. Sense current change rate for (a) -1V and (b) -2.5V. Both defect generation and filling influence the dark current changes.

Compared to the vertical p-i-n structures in [11], our EAM structures show a more pronounced filling of traps, which causes a significantly lower increase of the dark current during stress (Fig. 7). From this figure, we can also read that the increase of stress current at operating conditions (85°C/ -2V, marked by a star in the figure), is not expected to be significant for the stress durations applied during BTS.

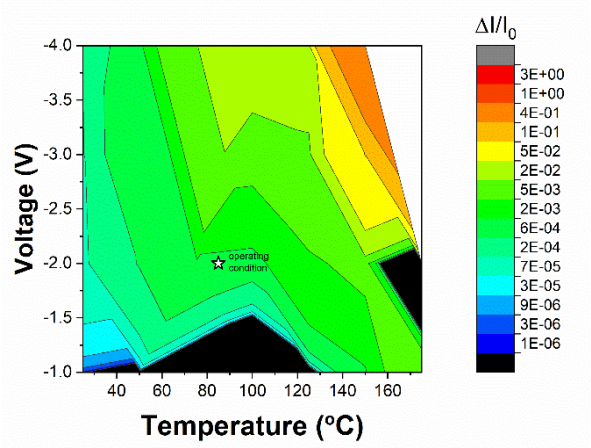

Figure 7. Stress current change illustrated by change of charge after stress with black area representing negative values. The change of stress current at operation conditions (85°C/-2V) is not expected to be significant ($\Delta I/I_0 \approx$ 1e-3).

C. *Long term voltage stress results*

After BTS tests with shorter testing times, we also performed accelerating aging tests on package level for much longer times period and at the 3 device geometries shown in Table I. From the t_0 wafer-level data, the influence of the Ge length on the dark current level at -2V appears significant (Fig. 8). With the interfaces of Ge/Si and Ge/Ox having the highest electric field values for this bias as shown before in Fig. 3, an expected higher I_{dark} for the longer device is observed. The more threading dislocations, due to the 4.2% lattice mismatch between Ge and Si after epitaxy, the higher the I_{dark}.

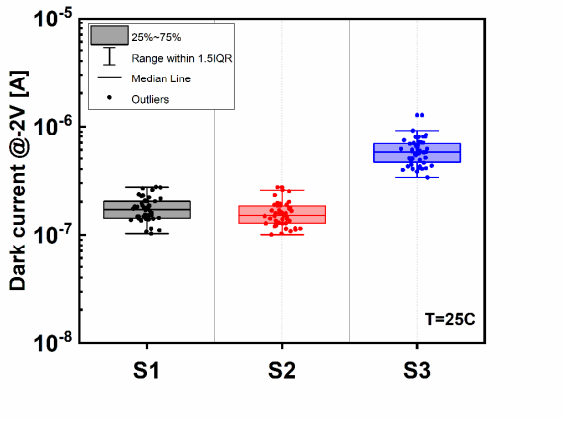

Figure 8. Length dependence on the obtained wafer-level dark current values at -2V is significant.

The same ΔI_{dark} trends w.r.t. stress time are observed, for all 3 geometries, suggesting that the initial dark current level is not actually impacting the overall observations. Therefore, only S1 is shown in Fig. 9.

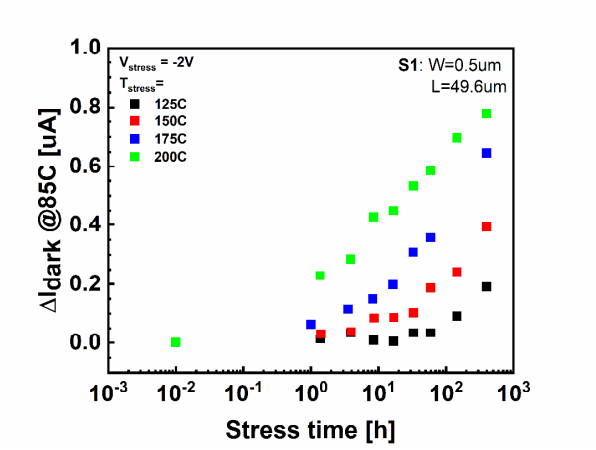

Figure 9. Dark current shift at Top=85°C, for all stress conditions, revealing the two-phase degradation that occurs similar to GeSi EAMs.

Similar to the GeSi EAMs [9] and the conclusions from Section III.B, two degradation mechanisms are evident and dependent on the applied temperature. For 125°C and 150°C there is a bimodal behavior, with the first part describing the trap filling, followed by a power-law increase that typically indicates creation of new defects. On the contrary, for 175°C and 200°C the defect creation takes place much faster denoting the impact of temperature on the I_{dark} degradation at a constant V_{stress} value (as can also be observed in Fig. 6). By fitting the linear part of the dark current shift at different T_{stress}, in Fig. 9, we determine the so called "incubation time". Plotting the values for all samples (Fig. 10), it becomes clear that the decrease is independent of the device length, despite the fact that the initial dark current level is higher for the S3 device.

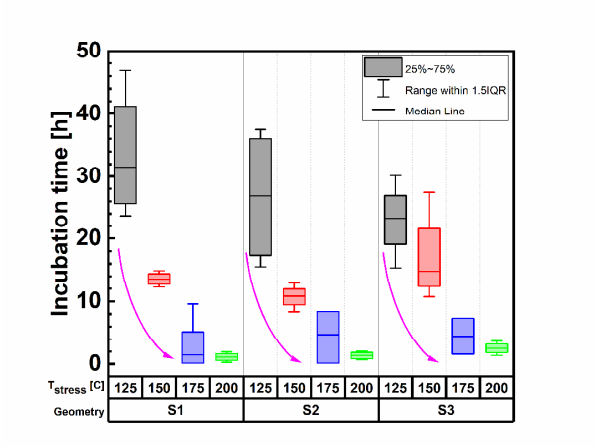

Figure 10. Incubation time for different device geometries and different stress temperatures suggest that the defect filling rate takes place faster as stress temperature increases and independently of the device length.

Normalizing the ΔI_{dark} with I_0, from S1 to S3, all data can be merged (Fig. 11) and even the highest stress temperatures can be fitted towards lifetime extraction using the semi-empirical model of Eq. 1-2. The proposed model follows an Arrhenius behavior over the measured temperature range, with some of the parameters fitted on the logarithmic scale, to automatically constrain them to positive values and to "steer" the optimizer algorithm, developed with the Wolfram Mathematica software package. The fitted activation energy of 1.15eV suggests that the failure mechanism could be a combination of slow charge trapping (~1.3eV) [16] and creation of new defects, that eventually lower the E_A value.

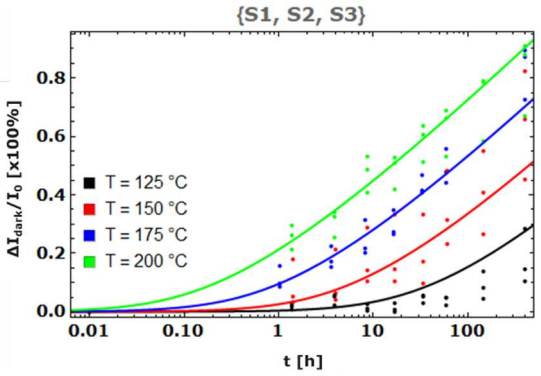

Figure 11. Fitted data of the relative I_{dark} shift w.r.t. stress time and T_{stress}, geometry independent, using Eq. 1.

$$\Delta I_{Drk}[t, \tau, \Delta I_{de}, m] == \Delta I_{de} \cdot \mathbf{W}\left[\left(\frac{t}{\tau}\right)^{m}\right] \quad (1)$$

with m being the exponent, τ the "incubation time" and **W** is the Lambert function.

Wherein

$$\tau[T_C] == A \cdot e^{\frac{E_a}{k_B \cdot (T_C + 273.15)}} \quad (2)$$

with E_a the activation energy of the degradation mechanism, k_B the Boltzmann constant and T_C the stress temperature.

In addition to the reliability study, Human Body Model (HBM) electrostatic discharge (ESD) measurements were performed on bare die level. HBM ESD stress in reverse with steps of 10V was applied and the devices were characterized with an I-V sweep (-2V to +1V) after every zap. The voltages at which we see a first change in I_{dark} and at which the device completely breaks scales with the device length (Fig. 12).

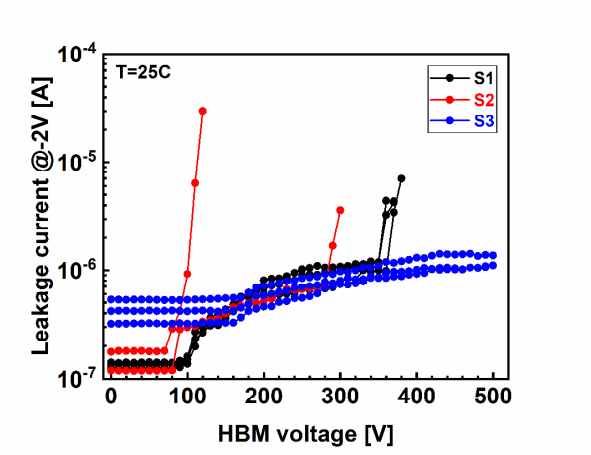

Figure 12. HBM data scaling with Ge device length, with S3 having the highest tolerance.

This could be related to the t_0 series resistance that reduces with increasing diode length (Fig. 13), similar to previously reported Transmission Line Pulse (TLP) results [17], increasing the robustness of the longer device. Nevertheless, the ≥100 V HBM robustness for device S1 and S3 is high enough to avoid damage during handling in facilities and processes that comply with the ANSI/ESD S20.20 standard [18]. However, device S2 requires ESD control measures beyond the S20.20 standard and ideally below 60 V HBM to ensure safe handling. This is a reasonable requirement for advanced fabrication and assembly processes.

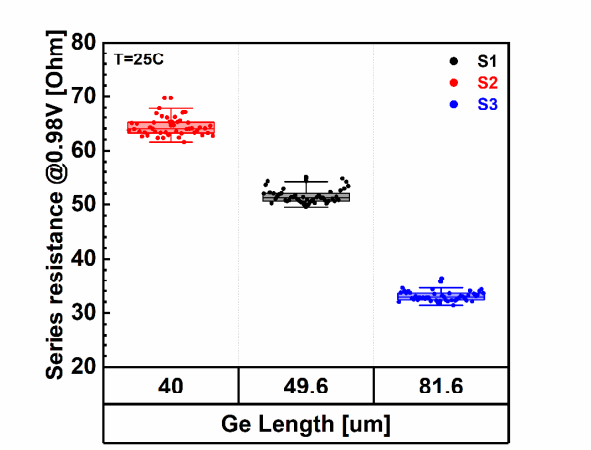

Figure 13. Ge length dependence of series resistance that impact the devices's HBM ESD robustness . Lower series resistance means that the device can conduct a higher current for a fixed IR voltage, therefore increasing the HBM ESD robustness.

D. Performance evaluation after stress

Electro-optical measurements, at different time intervals were performed at room temperature, on long term stressed devices. Each point in the following plots, represents the average of 4 samples per condition and the samples at zero stress time, the reference, non-stressed, devices. Fig. 14-15, demonstrate the electrical stability of our devices. The extracted value of the series resistance, at 0.98V of forward bias, remains constant for all stress conditions, up to 5000h of stress time and for all tested geometries.

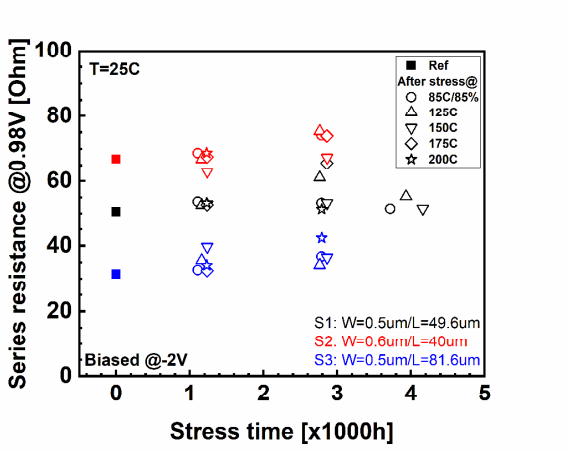

Figure 14. Extracted series resistance for all the tested temperatures, at biased and unbiased conditions. Series resistance remains unaffected after stress.

At the same time, the ideality factor, calculated from the I-V slope in the lower forward bias regime, from 0.05V to 0.35V, is showing no significant change after stress, ensuring the good quality of the diode.

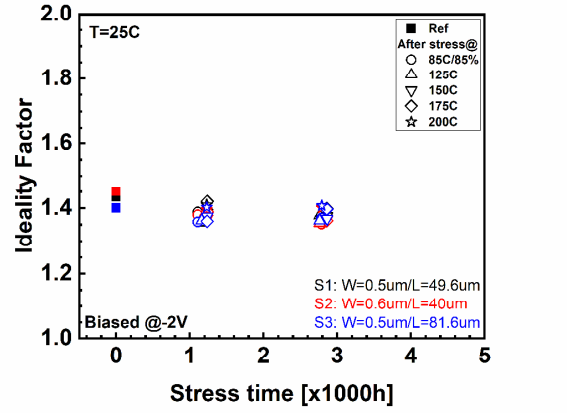

Figure 15. Ideality factor is not impacted by any stress condition staying at 1.4 for all stressed samples.

On the optical side, similar observations can be made. In Fig. 15, the Extinction Ratio (ER), for a max Figure Of Merit and for a voltage swing of 2xVpp, is shown. S1 and S2 were measured as modulators and for up to 4500h of electrical stress, no degradation of the reference value is observed.

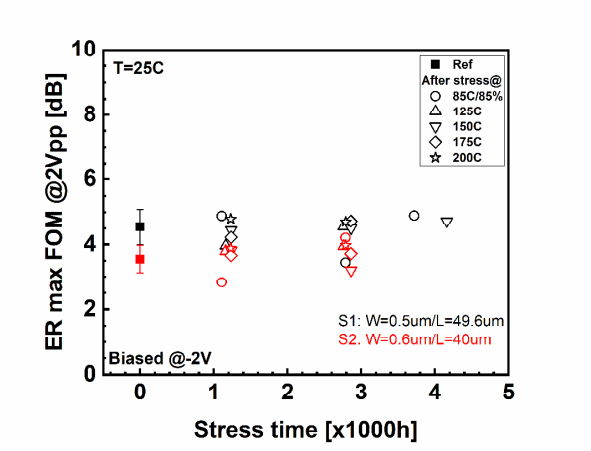

Figure 16. Extracted ER for all tested temperatures, at biased and unbiased conditions. The Extinction Ratio of the stressed samples remains on the same level as the reference ones.

At the same time, the modulation wavelength that is calculated for a max ER at 2xVpp (Fig. 17), remains stable at 1600 nm, which is the nominal value for these demonstrated EAMs. As a result, for the applied stress conditions and despite the dark current degradation that these components are exhibiting, their performance before and after stress has not been compromised.

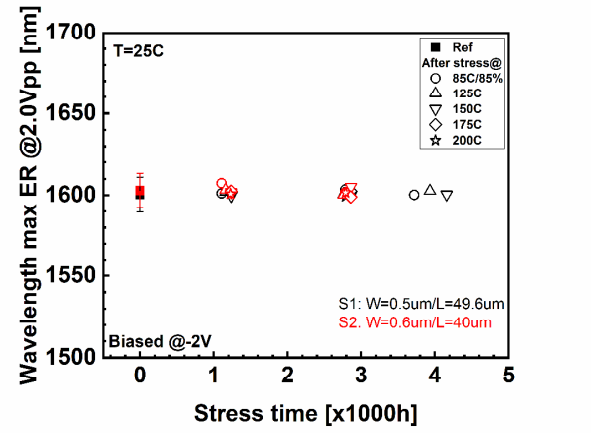

Figure 17. The wavelength of the modulators, at the maximum ER at 2Vpp, did not change after electrical stress.

IV. Conclusions

A detailed reliability study on Ge EAMs to investigate the degradation mechanisms of the dark current, was presented in this work. Filling of (pre-existing) defects and defect generation are taking place during electrical stress. While both are simultaneously present, depending on the applied stress conditions, one is more dominant. A semi-empirical model of the relative I_{dark} shift independent of the diode geometry, allows lifetime extrapolations to normal operating conditions. The extracted activation energy is indicating a combination of slow charge trapping and creation of new defects. Despite the I_{dark} degradation, at high temperatures, no failure is expected at operating conditions (85°C/ -2V). A conclusion confirmed as well, by performance evaluation after stress, that reveals no impact on the other electro-optical parameters.

Acknowledgments

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