Wafer-Level Aging of InGaAs/GaAs Nano-Ridge p-i-n Diodes Monolithically Integrated on Silicon

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For the first time, a reliability study on degradation of InGaAs/GaAs nano-ridge p-i-n diodes monolithically integrated on Si is reported. Wafer-level constant current stress in forward bias shows a gradual power law aging of both forward and dark current. The degradation mainly occurs near the p-contacts due to noticeable Joule heating. A sintering step lowers the series resistance hence improves the reliability. The aspect-ratio trapping layer efficiently blocks the threading dislocations, with no indication of dislocations penetrating the active region for the 5000s stress time used in this study.

Introduction **–** Monolithic integration manifests itself as the smallest form factor- and potentially lowest cost technology to implement light sources onto a silicon photonics (SiPho) platform. Quantum dot lasers using blanket layer growth demonstrate a promising lifetime [1]. However, the thick buffer layer hinders the integration with Si waveguides [2]. Apart from that, the research on degradation of fundamental diode properties has not yet been presented.

Leveraging aspect-ratio trapping (ART) and nano-ridge engineering (NRE), versatile III-V nano-ridges (NR) with reduced buffer layer have been grown on 300mm (001) Si substrates [3-6]. The structures showcase a fully relaxed, dislocation-free active layer and pronounced photoluminescence [4]. Nonetheless, threading dislocations (TDs) confined inside the ART trench pose one of the major reliability concerns for LEDs and lasers. The formation of dark line defects (DLD) through recombination-enhanced dislocation climb/glide are well-known to provoke rapid degradation [7]. For the first time, this early work presents a reliability study on multi-quantum well (MQW) InGaAs/GaAs NR p-i-n diodes under wafer-level constant current aging.

Design parameters **–** Schematics of the NR diode are depicted in Fig. 1. TABLE I describes the design of experiments. The trench width of 80nm ensures sufficient ART (AR~3.75), the TD density is below $4.5\times10^{5}cm^{-2}$ as claimed in [5]. Cross section TEM images in Fig. 2 show a high-quality active region with all TDs trapped inside the trench. Tungsten contact plugs atop the nano-ridge contribute to optical absorption loss, which can be mitigated by enlarging the distance between two metal plugs. The responsivity of nano-ridge waveguide photodetectors was found to be improved by using a sparse p-contact plug pitch [8]. The reliability of two p-contact plug pitch designs, dense (0.3µm) and sparse (4.8µm) pitch, were analyzed in this study. The copper interconnects and contact plugs are located 150µm from the irregular shaped end facets alleviate fringing effects [2]. The diode length is defined as the metal length where carriers are injected into the NR, and ranges from 250µm to 2000µm. The diode length of devices under tests is 1000µm, if not specified otherwise.

Characterization **–** The current-voltage (I-V) curves of the NR diode as a function of temperature are illustrated in Fig. 3. The activation energy (E_A) extracted at -2V is slightly lower than $E_g/2$ of GaAs (inset in Fig. 3), pointing to a Shockley-Read-Hall (SRH) process combined with other leakage mechanisms such as trap-assisted tunneling (TAT) [11]. TABLE II summarizes the parameter extraction methodology and learning according to prior reliability studies on III-V optoelectrical devices.

Fig. 4 presents the (a) forward and (b) dark current as a function of diode length. $J_{forward}$ is independent of diode length while J_{dark} decreases for longer NRs due to reduced fringing effects. Additionally, increasing the p-contact plug pitch reduces the contact plug densities, resulting in higher R_{series} (Fig. 4 (c)).

Stress results **–** Devices were stressed under constant current density of 2kA/cm^2 at 40°C, for 5000s. Intermittently, the stress was removed, and the device degradation was monitored by I-V sweeps. The drift of I-V curves during stress is displayed in Fig. 5. The decrease in R_{series} and increase in $I_{forward}$ point to annealing and/or metallic diffusion near contacts (Fig. 6). Moreover, higher I_{dark} indicates leakage current paths build up during stress. The gradual degradation of parameters in GaAs NR diodes follows a power law illustrated in Fig. 6. The exponents of $\Delta I_{forward}$ and ΔR_{series} are ~0.2 in contrast to ~0.33 of ΔI_{dark}, suggesting different mechanisms governing the stress- induced degradation.

Devices with sparse p-contact plug pitch suffer higher degradation in the forward bias region while the I_{dark} increment is comparable with dense pitch structures, see Fig. 6. Reduced contact plug densities induce current crowding and Joule heating, eventually lead to faster aging. An optional sintering process (420°C, 20mins) improves contact qualities thus R_{series} decreases for both sparse and dense pitch (Fig. 7(a)). Besides, R_{series} is positively correlated with the degradation coefficient of $\Delta I_{forward}$ (Fig. 7(b)). Due to the variability of R_{series}, devices were stressed at various voltages when applying constant current. As clearly demonstrated in the $\Delta I_{forward}$-V_{stress} plot in Fig. 8, the degradation near p-contacts governs the change in $I_{forward}$. $\Delta I_{forward}$ increases exponentially with the stress voltage and the two p-contact plug pitch designs obey separate trend lines. Conversely, ΔI_{dark} is independent of p-contact plug pitch and stress voltage (not shown), possibly caused by defect-enhanced leakage in the bulk or at the NR surface.

Fig. 9 shows the effect of diode length on stress-induced degradation. A longer diode length may be required in future laser devices, while having a greater risk of finding a TD into the GaAs volume, which serves as a latent defect. Nevertheless, degradation of both $I_{forward}$ and I_{dark} exhibit weak correlation with diode length up to 2000µm for two possible reasons: (a) insufficient stress time to initiate recombination enhanced dislocation motions, or (b) ART trench efficiently prevents TDs from penetrating into the quantum wells. Furthermore, the result denotes that degradation is dominated by the p-metal/nano-ridge cross section.

Conclusions **–** Wafer-level constant current aging discloses the reliability sensitive region of the NR diode: the tungsten/p-GaAs contacts. TDs at the ART trench do not seem to dominate the degradation behavior for the stress conditions explored in this early work. Their relative impact on long-term reliability needs further investigation.

References

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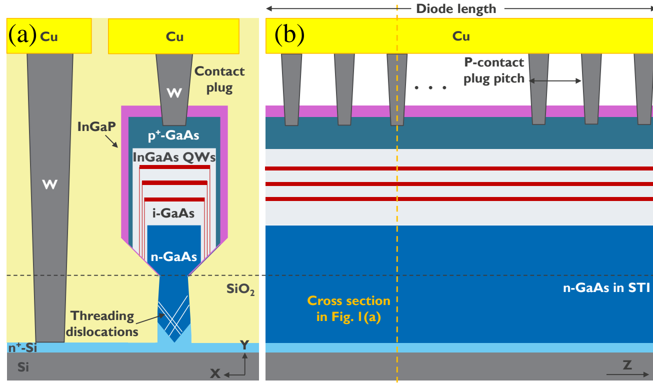

Figure 1. Schematics of InGaAs/GaAs nano-ridge p-i-n diode monolithically integrated on Si, leaveraging the aspect-ratio trapping (ART) and nano-ridge engineering (NRE) concepts. (a) cross section and (b) lateral cut.

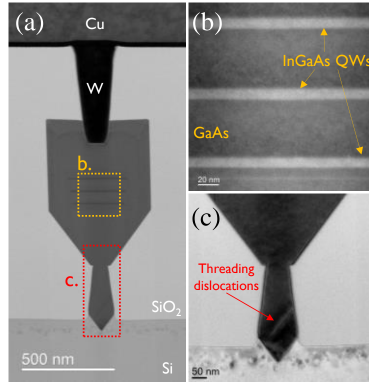

Figure 2. (a) ABF-STEM of the nano-ridge cross section. (b) zoomed-in HAADF-STEM of uniform multi-quantum wells. (c) zoomed-in (400)-BF TEM of the aspect-ratio trapping region.

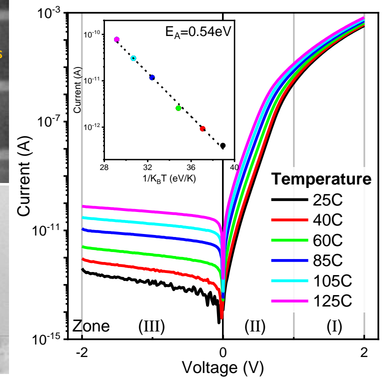

Figure 3. Current-Voltage (I-V) characteristics as a function of temperature, the activation energy (E_A) is 0.54eV extracted at -2V from the Arrhenius plot in the inset.

TABLE I. DESIGN OF EXPERIMENTS

Design parameter	Unit	Design
Process*	-	w/o sintering, sintering
Trench Width	nm	80
P-contact plug pitch	µm	0.3, 0.6, 1.2, 2.4, 4.8
Diode length	µm	250, 500, 1000, 2000

*An optional sintering process of 420°C, 20mins can be adopted to improve contact quality.

TABLE II. PARAMETER EXTRACTION AND LEARNNGS

Zone	Parameter	Method	Learnings from literature	Ref.
(I)	Forward current ($I_{forward}$)	Current at 2V	- Diode performance	[9]
(I)	Series resistance (R_{series})	1/slope at 2V	- Contact quality - Increase/decrease → metallic diffusion	[9]
(II)	Current at low forward bias	-	- Increase → reduction in non-radiative carrier lifetime	[9]
(III)	Dark current (I_{dark})	Current at -2V	- Crystal quality - Increase → defect diffusion/generation in the active zone/at surface	[10]
(III)	Activation energy (E_A)	Arrhenius plot	- Defect conductive mechanism	[11]

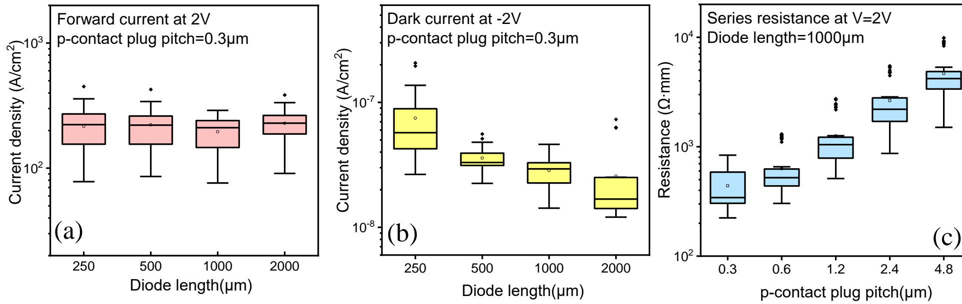

Figure 4. Characteristics of NR diodes. (a) forward current and (b) dark current as a function of diode length, p-contact plug; (c) Series resistance as a function of p-contact plug pitch.

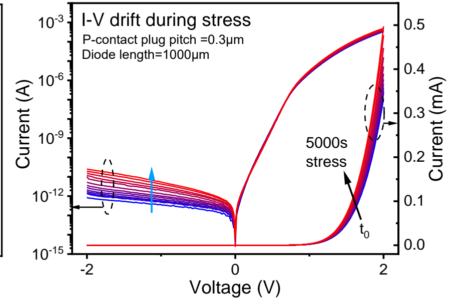

Figure 5. Semi-log (left) and linear (right) I-V curves at various stress time, T=40°C, J=2kA/cm².

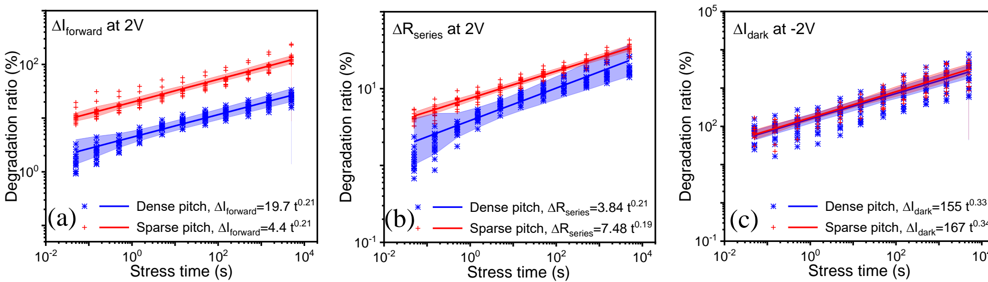

Figure 6. Degradation of parameters follows the power law, $\Delta P = \frac{P(t) - P_0}{P_0} = Ct^{\alpha}$. (a) forward current, (b) series resistance and (c) dark current. The filled areas indicate 95% confidence intervels of the weighted least-aquare fit.

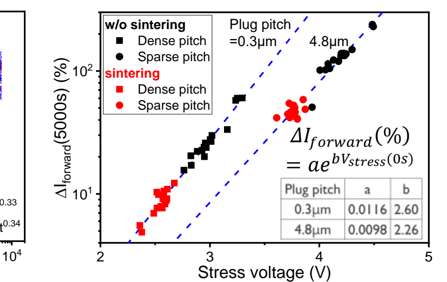

Figure 8. $I_{forward}$ degradation is a function of stress voltage and p-contact plug pitch.

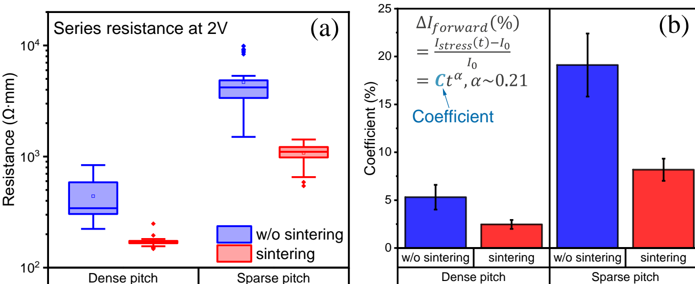

Figure 7. Sintering (420°C, 20mins) improves contacts and electrical stability. Both (a) Series resistance and (b) power law coefficient of $I_{forward}$ decrease.

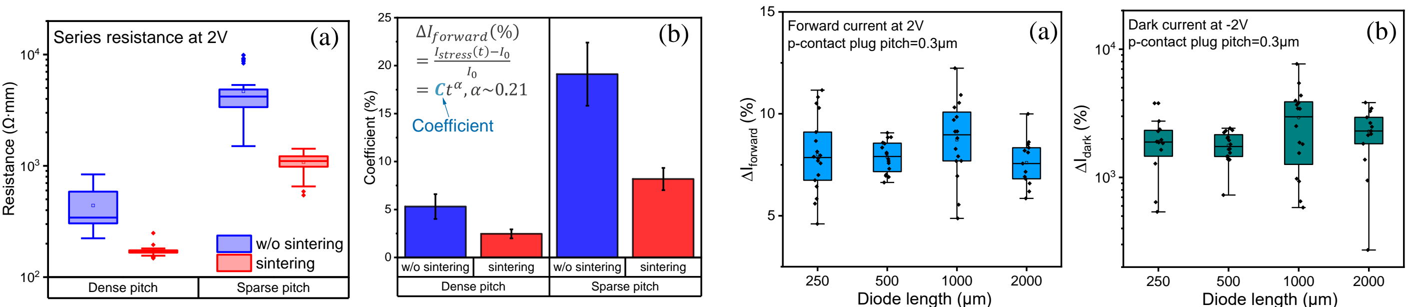

Figure 9. Effect of cavity length on stress-induced degradation. Degradation of (a) $I_{forward}$ and (b) I_{dark} after 5000s stress are independent of diode length.