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# Investigating metal oxide resists for patterning 28-nm pitch structures using single exposure extreme ultraviolet: defectivity, electrical test, and voltage contrast study

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## Abstract

**Background:** To keep up with the logic area scaling, back-end-of-line (BEOL) structures are reduced to smaller pitches, requiring faster and reliable metrology and defect detection solution.

**Aim:** Metrology and detailed defect inspection at the early phases of process optimization.

**Approach:** Single exposure (SE) 0.33NA extreme ultraviolet (EUV) lithography was used along with a bright field mask for patterning in a metal damascene process flow of BEOL structures. We also used a dual damascene process flow for voltage contrast (VC) metrology study.

**Results:** Scatterometry technique, together with machine learning (ML), allowed us to have fast and accurate measurements of line-space (LS) and tip-to-tip (T2T) critical dimension (CD), and prediction of electrical performance. We demonstrated characterization results of stochastic defects across various test structures of 28-nm pitch devices. We used a large-area electron beam (e-beam) tool for high-speed large-area inspection which provided us with the quick feedback on defect signatures and scope for further root cause analysis. On a separate dual damascene integration flow, we used VC metrology to capture different failure modes in the patterning process of metal trenches with tight T2T and corresponding overlapping vias.

**Conclusions:** We studied the impact of stochastic resist defects on electrical measurements of meander (MR) and fork-fork (FF) structures, and showed that large electrical test structures, built with a relatively simple patterning flow, can be used at the early stages of resist and patterning development, as the electrical failures are almost exclusively caused by the resist defects. In the dual damascene flow, we demonstrated that VC metrology is useful to determine the design rule parameters and capture different failure mechanisms.

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**Keywords:** Single exposure extreme ultraviolet lithography; bright field mask; 28 nm back-end-of-line pitch; scatterometry; Ruthenium Damascene metallization; electrical test; machine learning.

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## 1 Introduction

There is an everlasting drive and motivation among the integrated circuit (IC) manufacturers to continuously shrink the device features, increase drive current, and reduce voltage. Utilizing conventional 193i lithography, downsizing of semiconductor devices becomes challenging as well as economically less favorable because of the additional cost and intricacy of multi-patterning flows. As a solution, 0.33NA extreme ultraviolet (EUV) lithography has already been introduced from the 7 nm node in high-volume manufacturing (HVM). The most

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advanced generation of the 0.33NA EUV tool offers 28 nm resolution.[1] However, due to the formation of stochastic resist bridge and resist thinning (predominantly driven by the noise of EUV photon shot and the randomness of chemical reaction), printing a pitch below 30 nm turns out to be challenging and does not yet fulfill the low failure rates required for high volume production yield.[2]

The downsizing of structures is often associated with complex three-dimensional (3D) device architectures and increases the importance and role of metrology, which includes exploratory research, technology development, and process control.[3] Metrology methods such as scatterometry and critical dimension scanning electron microscope (CDSEM) are typically used for inline CD measurement. The measurement performance of an SEM tool is impacted by resist shrinkage and charging effect.[4] Scatterometry is known for its fast and nondestructive metrology method which provides complete profile information of the fins in front-end-of-line (FEOL) and the interconnect lines in back-end-of-line (BEOL).[5] However, traditional scatterometry model building requires a long time to solution, especially, research and development (R&D), and modeling of nonperiodic structures can take even longer time and be problematic. Additionally, strict process control budget might be compromised by model errors. For these reasons, direct measurement of all the essential parameters may not be possible which leads to the requirement for predictive statistical approaches such as machine learning (ML).[6]

Stochastic defect detection and characterization remain troublesome while printing very tight pitches, because of the sub-10 nm defect size. Optical broadband plasma (BBP) tools can offer large-area inspection quickly, but defect detection sensitivity is quite challenging due to the defect size.[7] Electron beam (e-beam) based inspection can provide the ultimate sensitivity, however, inspection is possible only for areas of a few $mm^2$ to keep inspection time reasonable.

To keep the stochastic defects under control, EUV double patterning can be used to print 28-nm pitch line-space (LS) structures. However, the ownership cost of EUV double patterning is much higher than that of a single exposure (SE) EUV.[8] Therefore, to diminish the manufacturing cost, SE EUV has received greater attention and there are ongoing studies to print aggressive pitches while keeping stochastic defects under control. de Simone et al.[9] demonstrated that for 28 nm pitch LS, printed using SE EUV, the stochastic nano-bridge and -break density depend on the size of resist CD, and the defectivity could be further pushed down by choosing optimum postexposure bake (PEB) temperature and appropriate filter during the resist coating process. Recently, in support of logic scaling below the 5 nm node, Meli et al.[10] reported an electrical yield of 28-nm pitch for devices longer than 1 cm.

In this study, we verified ML capabilities to correlate the scatterometry data of structures of 28 nm pitch. We used a large area e-beam tool with large field-of-view (FOV) inspection capability to obtain after development inspection (ADI) and after etch inspection (AEI) defectivity. We also explored the effect of stochastic defect on the electrical yield and performed voltage contrast (VC) study to understand the different failure modes.

## 2 Wafer Processing Details

### 2.1 *Single Ruthenium Damascene Flow*

The process starts with BEOL stack deposition on Si wafers, followed by coating the wafers with metal oxide resist (MOR) on top of amorphous carbon (APF) hard mask (HM) and spin-on-glass (SOG) (Fig. 1). Using the damascene approach, a minimum metal pitch of 28 nm (vertical LS structure) was patterned using a source mask optimization (SMO) dipole source (Fig. 1) in an ASML 3400B EUV scanner. EUV light (13.5 nm) exposure and negative tone development (NTD) process were used to print the structures using a bright field (BF) mask tonality. The patterns were transferred into a 15 nm TiN HM layer and subsequently into a 60 nm oxide dielectric layer using two different plasma etch chambers. Finally, the metallization steps involved filling the trenches with TiN liner (1.5 nm) and Ru (interconnect material), followed by chemical mechanical polishing (CMP) to form the electrically active Ru lines.



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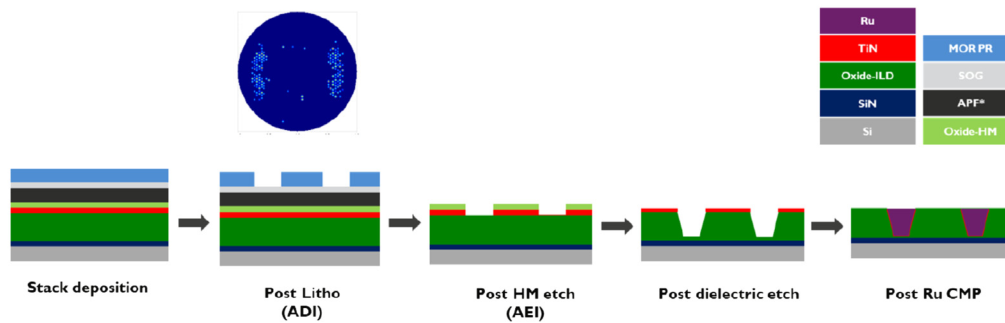


**Fig. 1** Schematic of the stack and simplified Ru damascene process flow including ADI and AEI steps, and source map used to pattern the LS structures.

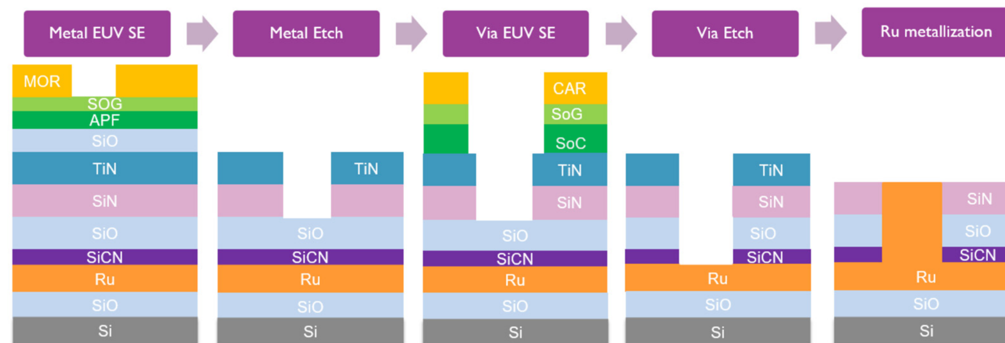


**Fig. 2** Schematic representation of a dual damascene VC-compatible process flow. Ruthenium metallization was used for the fill.

## 2.2 *Dual Ruthenium Damascene Flow*

A different process flow (Fig. 2) was specifically used for the VC[11] measurement. First, a blanket Ru layer was deposited on $SiO_x$-coated Si substrate, and then the dielectric layers (SiCN, $SiO_x$, and SiN) were deposited. Next, HM layers of $SiO_x$, TiN, and amorphous carbon (APF) were conformally deposited on top of the SiN. The Ru blanket layer was used as a virtual ground to enable VC measurement and the SiN layer was introduced to enable separate study on the impact of stress on overlay. SE EUV lithography, NTD process, and MOR were used to transfer the vertical metal trench (28 nm pitch) patterns into the SiN layer, stopping selectively on the $SiO_x$ layer using a plasma etch process with almost no litho to etch bias. A second SE EUV lithography along with positive tone development (PTD) process, and chemically amplified resist (CAR) were utilized to transfer the via pattern (56 nm pitch) into the bottom $SiO_x$/SiCN dielectric, stopping on the Ru layer. Then, the via-trench structures were metalized using a thin TiN adhesion layer followed by Ru deposition. Next, Ru/TiN CMP was performed to complete the devices. Notably, for these smaller features, Ru metallization was preferred over Cu metallization.[12]

# 3 Results and Discussion

## 3.1 *Line-Edge-Roughness (LER) Estimation*

The unbiased LER estimations were performed post HM etch at different focus conditions for three different pitches (28, 30, and 32 nm) by collecting 49 images and using the MetroLER software. CDSEM images of $2048 \times 2048$ pixels (pixel size of 0.8 nm) were acquired using a HITACHI 6300 tool and an example of such an image is shown in Fig. 3.



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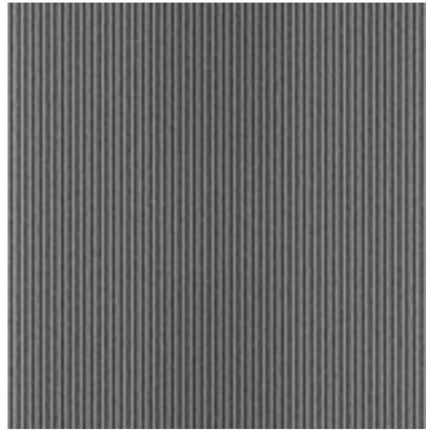

**Fig. 3** CDSEM image of $2048 \times 2048$ pixels.

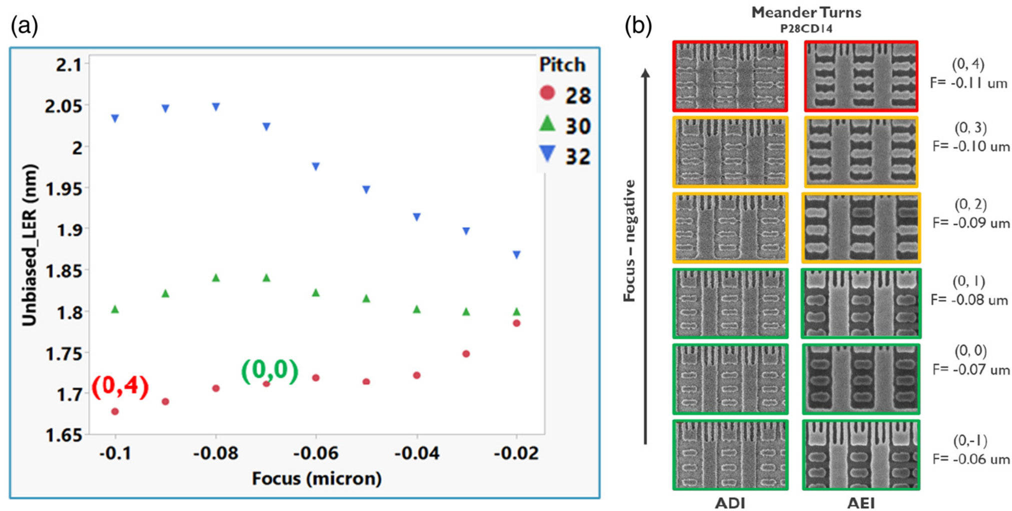


**Fig. 4** (a) Unbiased LER measurement versus focus for different pitches. (b) Meander turns (CD = 14 nm, pitch = 28 nm) at different focus conditions.

The unbiased LER values demonstrated that the 28 nm pitch has very different best focus condition compared to that of 32 nm pitch, e.g., at the focus of $-0.1$ $\mu$m, the LER value of 28 nm pitch was found to be the lowest, whereas it was very high for 32 nm pitch [Fig. 4(a)]. Moreover, while investigating the meander turns for the 28 nm pitch devices, we obtained the best focus condition at $-0.07$ $\mu$m [Fig. 4(b)].

The wafer maps, obtained at AEI of HM and oxide dielectric of meander (MR) and fork-fork (FF) devices, demonstrated that the mean CD is $\sim$14 nm with $3\sigma$ of $\sim$1.7 nm (Fig. 5). Notably, the center and edge of the wafers have a CD close to 13.5 and 15 nm, respectively. The CDSEM images showed that the turns were healthy for the wafers printed at the best-dose and best-focus conditions (Fig. 5).

## 3.2 *Large Area E-beam Inspection (ADI and AEI) of Tip-to-Tip (T2T) Structures*

In the case of SEM inspection tools, automatic defect detection plays an important role in correct defect isolation and subsequent classification. Traditionally, defect detection involves collecting images of a defective and a reference location, and then computing the difference. Classical or statistical algorithm is then used to extract defect signal location among the many noisy signals



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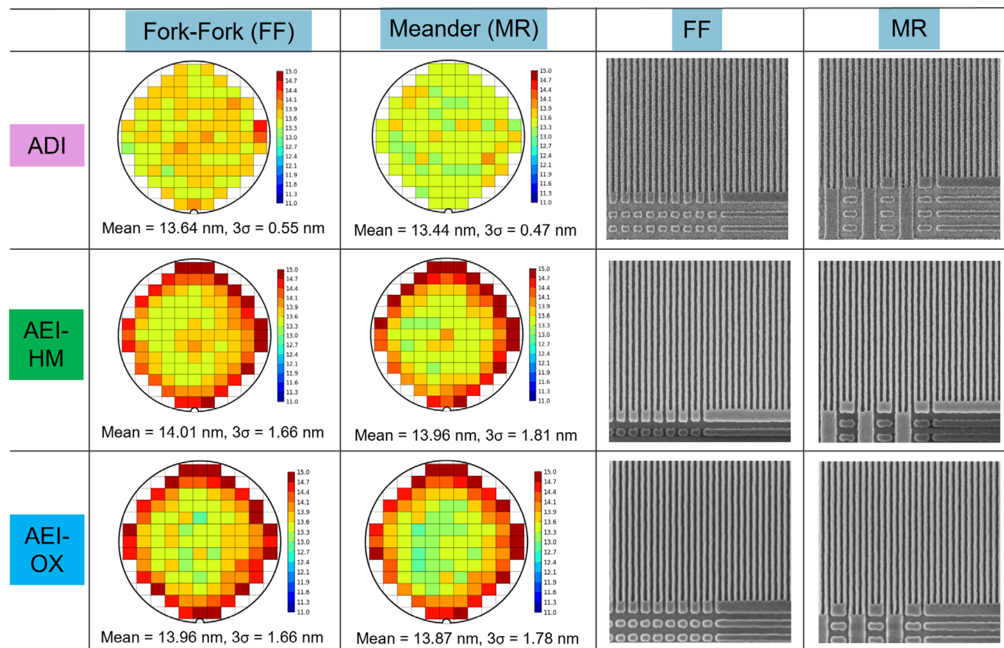


**Fig. 5** Wafer maps showing CD after etching of the HM and oxide dielectric trench for 28-nm pitch (design CD = 14 nm) MR and FF devices on a uniform-dose wafer, and their representative CDSEM images.

arising due to inevitable pattern variations. Several factors give rise to these pattern noise signals, e.g., LER (both low and high-frequency variations), poor pattern fidelity, grains, etc. Variations may not only be present on the top (current inspection) layer but may also be perceived from the previous layer when a higher landing energy is during SEM inspection. Such noise issues are becoming more predominant when we scale to tight pitches and defect sizes become smaller. One of the ways to deal with the noise during defect detection is to be able to distinguish the noisy and defect signal pixels accurately and robustly.

A new deep learning algorithm can help to increase the performance significantly in detection and classification. We implemented such a capability in a large-area e-beam tool, which provided enhanced detection sensitivity. Most frequently, deep learning applications rely on a very large number of training examples, which is not feasible in the semiconductor industry as the available library of a given defect type may be limited. The e-beam tool is explicitly designed to train on limited examples which is another key feature of the deep learning algorithm. Sometimes, a few tens of defect examples are sufficient for high detection accuracy. Often CD variation and roughness lead to high SEM inspection noise. Therefore, it is important to suppress this noise and increase the signal-to-noise ratio of the defect of interest (DOI) for better detection efficiency while maintaining high throughput for meaningful wafer coverage.

For T2T structure, we inspected 20 design rule combinations, characterized by their layout (regular = $R$ or staggered = $S$), slot length (60 or 80 nm), and T2T space (22 to 26 nm with step size = 1 nm) [Fig. 6(a)]. Since BF mask was used, the blue polygons indicate absorbers. We investigated blocks across multiple fields on the wafer and mainly observed horizontal and vertical shorts for the T2T structures [Fig. 6(c)]. Defect distribution across various design rules demonstrated that short-staggered trenches (S60) fail at a much higher rate compared with longer trenches (S80) or regular structure (R60 and R80), and moreover, the fail rate was found to follow the T2T vertical design CD [Fig. 6(b)].

In the case of the AEI T2T structures, we observed S60 trenches again dominating the defect pareto (Figs. 7 and 8). We found that the fail rate of the S60 vertical shorts (S60 V) follows vertical design CDs as expected, i.e., decreasing failures with increasing T2T CDs [Fig. 7(d)]. We also observed a strong center-to-edge wafer signature [Figs. 7(a) and 7(b)]. To study the defect signatures, quick T2T metrology measurements were done. Wafer maps were obtained for defect counts of vertical shorts on S60 patterns [Fig. 7(a)] and average T2T of all S60 pattern



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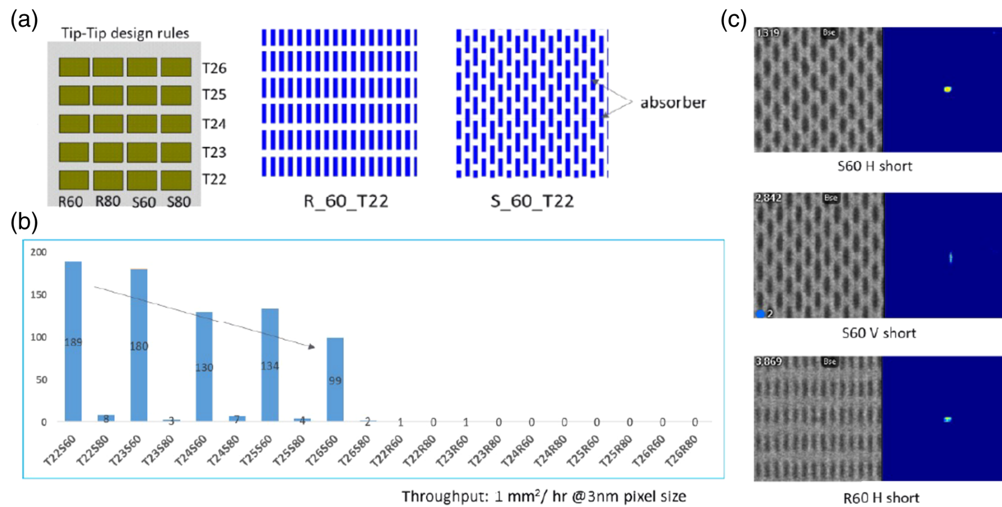


**Fig. 6** (a) 28 nm pitch LS and different T2T design rule structures. (b) Inspection of T2T structures showing higher failure in short-staggered trenches (S60) and is dependent on the T2T vertical design CDs. (c) Defect and patch images.

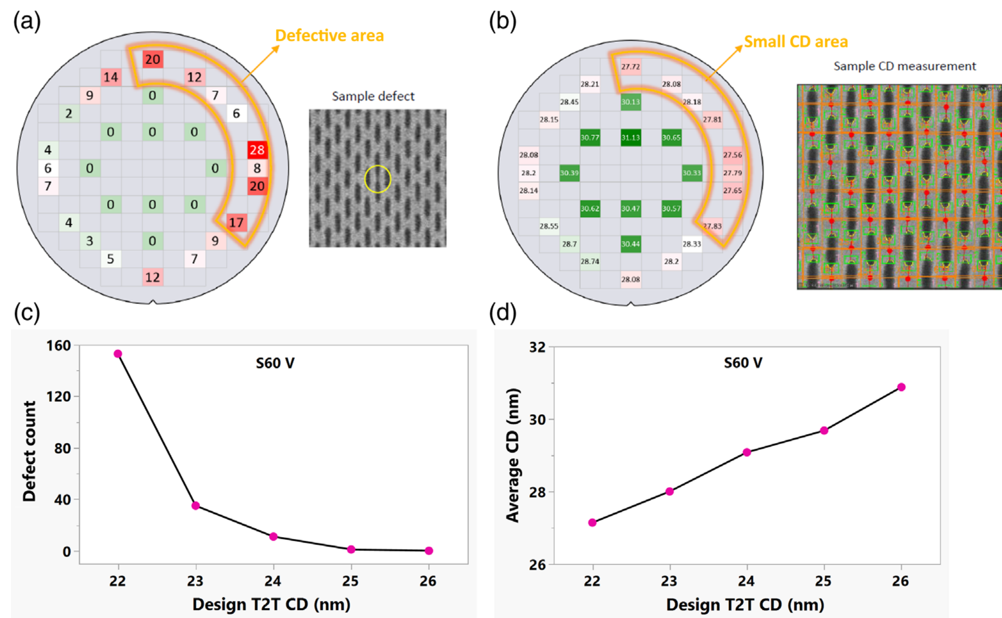


**Fig. 7** Defect count (a) and average CD distribution, (b) shown in a wafer map for verticals shorts of S60 pattern. Plots of (c) total defect count and (d) average CD split by T2T design rules.

[Fig. 7(b)], and it was clearly observed that the average CD decreases with increasing defect density [Fig. 7(d)]. Since the trends agree on an average, it can be concluded that the signature is most likely to be caused by the etch process. Interestingly, in the case of the S60 horizontal (S60 H) shorts, we observed that the effect of T2T design rules is less on both defect count and average CD, compared with the S60 V (Fig. 8).

### 3.3 *Scatterometry and ML: Space CD Measurement of 1D Feature*

ML solution, an attractive tool for process control, monitoring purposes, and electrical-test (e-test) prediction, involves cross-combining the inline scatterometry spectra with reference data.[5,13,14] Then a mathematical estimator is generated using a set of ML algorithm. The data used to create the mathematical estimator is called the training set, and once the training is



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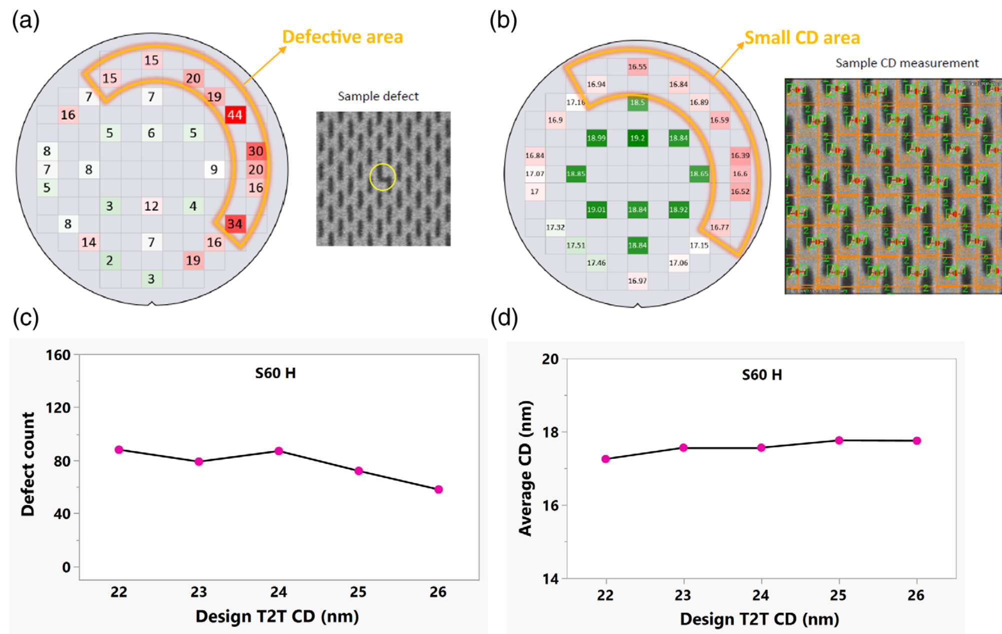


**Fig. 8** (a) Defect count and (b) average CD distribution is shown in a wafer map for horizontal shorts of S60 H pattern. Plots of (c) total defect count and (d) average CD split by T2T design rules.

completed and shows a good correlation to the reference data, the scatterometry spectra are used to measure and predict the parameters of interest. ML capabilities have been successfully demonstrated for inline CDs[15] and end-of-line e-test for HVM.[5] Furthermore, the ML technique is less dependent on the measured patterns' structural complexity and can also measure the non-periodic targets. The model optimization is done by the design of experiment (DOE) methodology. Extreme process window corners can be used during training of the data set to ensure ML can measure any process variation. ML-based inline scatterometry measurements allow early awareness of the electrical performance and variability, and thus significantly reduce the costs for both R&D and HVM by taking proactive action to either scrap or rework the wafer, improving the process robustness and monitoring accuracy.

To produce a robust dataset for training the ML model, we varied process parameters and conditions for different wafers at the lithography and etch step (Table 1). Lithography

**Table 1** Wafer processing conditions at various steps.

| Wafer ID | Litho | Etch |
|---|---|---|
| D10 | FEM | POR |
| D13 | Dose meander | POR |
| D14 | CDU | POR |
| D15 | CDU | POR |
| D16 | CDU | POR |
| D17 | CDU | POR |
| D18 | CDU | POR |
| D19 | CDU | POR |
| D20 | CDU | DOE |
| D21 | CDU | DOE |

POR, process on record; DOE, design of experiment; CDU, critical dimension uniformity.



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**Fig. 9** AEI measurement sites for FF, MR, and LS structures.

FEM (focus-energy matrix) and dose meander wafers were fabricated to obtain wide variation in the CD fingerprint. To enable successful ML training with good training scores, possible outliers were filtered out from the reference data set which is an essential aspect of the ML solution.

To eliminate the measurement errors, arising from line breaks and bridges of post HM etch, inline CDSEM data outliers were filtered out. Scatterometry spectra for the AEI ML training were collected from three different structures: MR, FF, and bulk LS region. All the structure and location of the optical CD (OCD) and CDSEM reference measurements are presented in Fig. 9. The width of the FF structure of the electrically active area is only 17 $\mu$m, which is smaller than the scatterometry spot size (30 $\mu m^2$), whereas, in the MR and LS structures, the scatterometry spot size is comparable to the width of the device structures (Fig. 9).

A single ML model was created for all the sites using the wafers labeled as D10 (FEM), D13 (dose meander), and D14 (CDU), and then tested on all the other CDU wafers (Table 1). We separated all the features to highlight ML's capability to measure small targets and comparison of the $R^2$ values, obtained from the correlation plots, demonstrated FF to be the best (Fig. 10). This also provides evidence that ML is capable of accurately measuring targets much smaller than the OCD spot size (Fig. 9). Wafer D21 with much smaller trench CD (due to modified etch process) was also measured accurately by the ML solution, showing its capability of covering even an unexpected process variation. The reference and ML solution for two CDU wafers showed expected radial etch distribution of CD for both the etch conditions (Fig. 10).

### 3.4 *Scatterometry and ML: T2T CD Measurement of 2D Feature*

The ability to directly print 2D features is a significant advantage of the SE EUV compared to multipatterning schemes and allows to simplify of the process flow by eliminating block

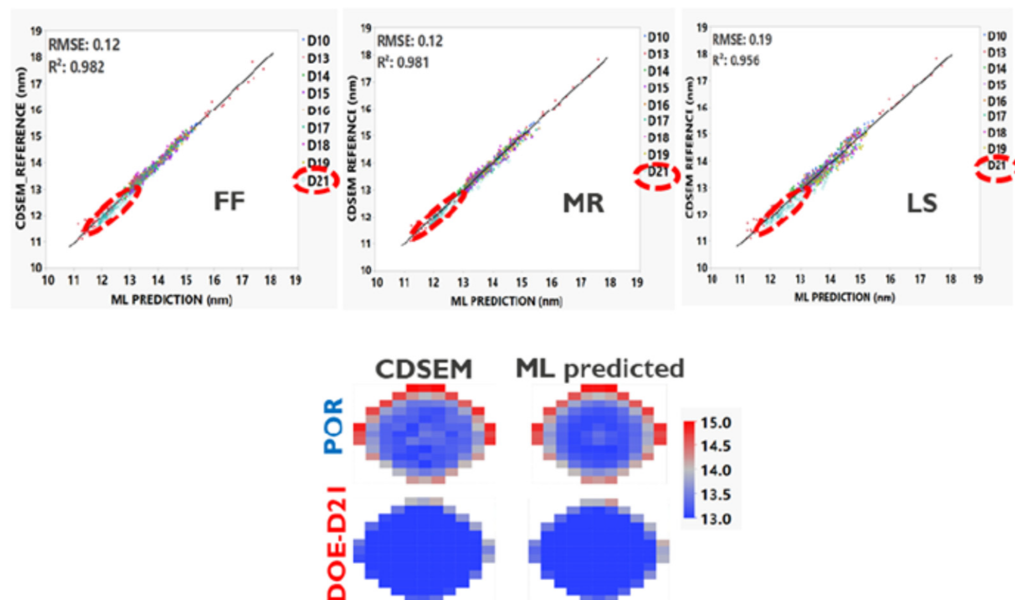


**Fig. 10** AEI correlation plots of CDSEM reference and ML-predicted data, and AEI wafer maps for two CDU wafers with different etch conditions.



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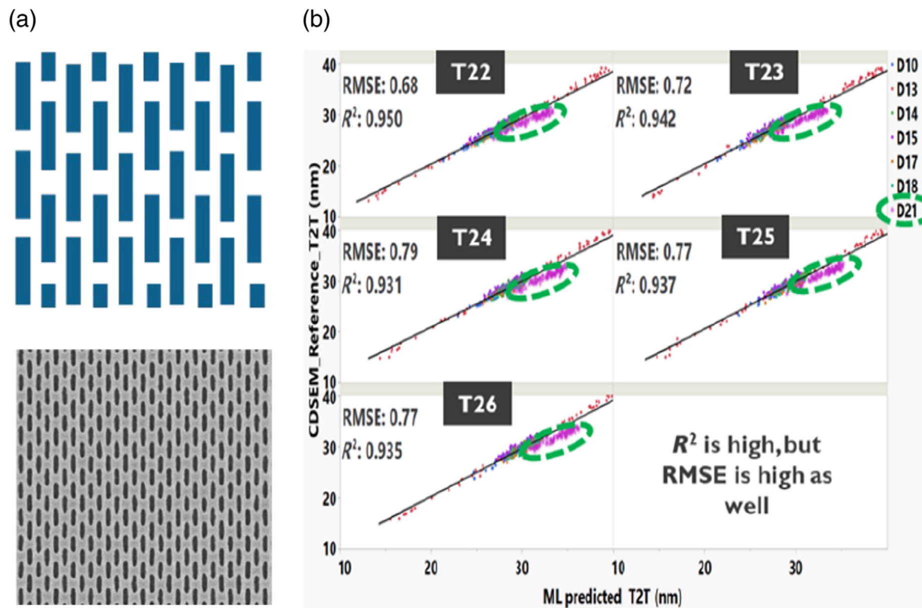


**Fig. 11** (a) Schematic of staggered block arrays and AEI pattern etched into HM. (b) Correlation of ML-predicted and reference AEI T2T CD values.

patterning, at least at some metal layers.[16] Generally, T2T measurements are done using CDSEM, which measures multiple single T2T structures to exclude measurement noise and capture variations of the T2T structures.[16] Unique test sites with different T2T structures were created to test OCD capabilities, including the T2T variations and pitch. Structures with five different T2T dimensions (22 to 26 nm, step size = 1 nm) between S60 long islands were studied. The schematic of the test design and CDSEM image of HM pattern are shown in Fig. 11(a). The CDSEM measurement consisted of averaging 50 different T2Ts within one FOV for each location of a die, and the average value was used to train the ML algorithm.

The ML training was performed on AEI FEM, dose meander, and CDU wafers for the five different feature sizes, and the ML solution was then used to verify each feature on the whole lot. Correlation plots of the ML-predicted and AEI reference data for the different T2T dimensions showed high $R^2$ values [Fig. 11(b)]. It suggests that the OCD spectra signal could discern the slight variation, especially considering the low T2T pattern density. Thus, OCD ML provided a fast and accurate inline monitoring of the T2T metal line average values in AEI step. The higher root mean square error (RMSE) values [Figs. 11(b)] could be explained by wafer D21, which was etched with a non-POR recipe and therefore was flagged in the correlation plots with different slopes [Fig. 11(b), areas marked with green dashed lines].

## 3.5 *E-test Prediction: Capacitance*

In the case of FF structures, the scatterometry spot size was found to be bigger than the width of the active device area (Fig. 12), as also mentioned before (Fig. 9). After Ru filling and CMP, the wafers were tested electrically, and the FF structures were used for the capacitance measurement. ML training was done separately for the 28 (14P28; design CD = 14 nm) and 30 nm pitch (15P30; design CD = 15 nm) structures.

Comparison of the reference capacitance data and the ML-predicted data showed good correlation score for both the 14P28 and 15P30 FF structures [Fig. 12(b)]. The $R^2$ value for the 15P30 structure was found to be better compared with that of 14P28 structure. One of the plausible explanations could be the significant variability of 14P28 capacitance measurements due to defectivity. Interestingly, for the 14P28 structures, an unusual capacitance value was observed for a die at the center of wafer, compared with its neighboring dies [Fig. 12(c), area marked with a red line]. This suggests a defective die and a detailed defect inspection study is required to analyze the exceptionally high capacitance value. However, the ML-predicted wafermap did not



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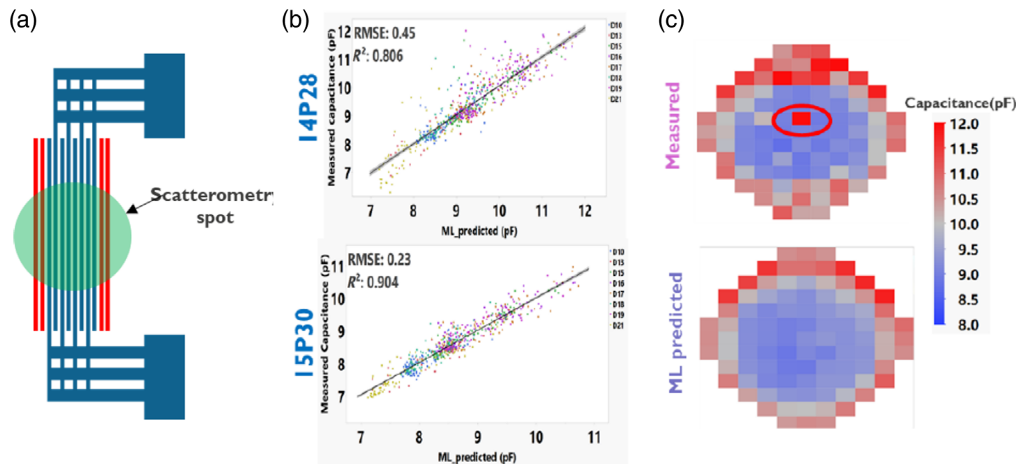


**Fig. 12** (a) Schematic of size comparison of FF structure and scatterometry spot. (b) Correlation plots between measured e-test and ML-predicted capacitance values for 14P28 and 15P30 structures. (c) Wafer maps of measured and ML-predicted capacitance for 14P28 in a CDU wafer.

show the unusual data. Therefore, the relatively low $R^2$ value for 14P28 structure and the mismatch points are mostly arising from the defective die. It also indicates that the scatterometry spectra are not sensitive enough to the small defects, which can cause incorrect capacitance measurement, providing an overview of a wide area with much less impact from defectivity.

### 3.6 *E-test Prediction: Resistance*

Resistance measurements were performed on the MR structures, which consist of very long lines with multiple turns and dummy lines (continuous = MR1 or segmented = MR6) of the same CD [Fig. 13(a)]. ML solution was trained for the three structures: 14P28 (MR1), 14P28 (MR6), and 15P30 (MR1). Prediction for the wafers showed good correlations ($R^2 > 0.93$) with the measured resistance values [Fig. 13(b)]. After HM etch, lower trench CD observed at the center of the wafer showed a higher resistance value [Figs. 13(c) and 13(d)]. It is noteworthy that an extremely high resistance value was measured at the center of a wafer [Fig. 13(c), black circle] and was filtered out during the ML training. On the other hand, ML solution predicted the Ru lines'

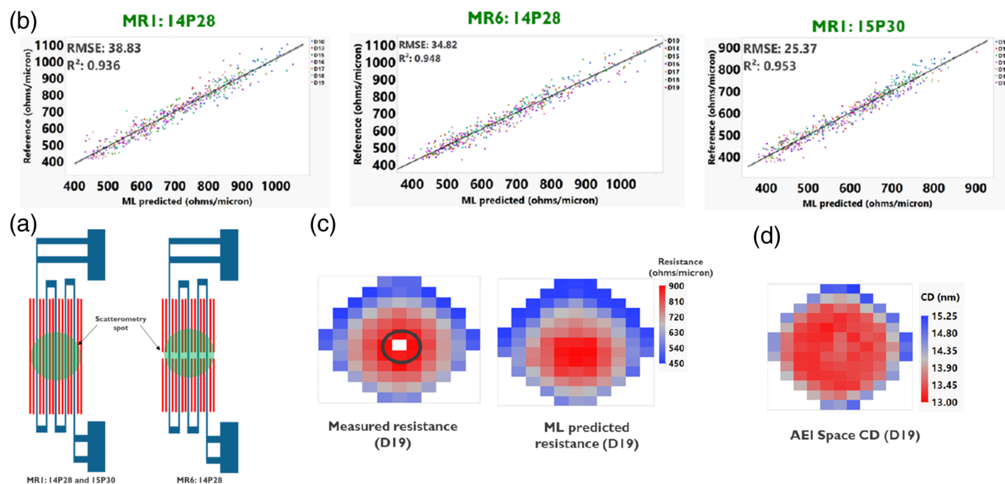


**Fig. 13** (a) Schematic of different meander structures and the scatterometry spot size. (b) Correlation between measured and predicted resistance values for three different devices. Wafer maps of (c) measured and predicted resistance of 14P28 (MR1) structure in a CDU wafer and (d) space CD of the same wafer at AEI.



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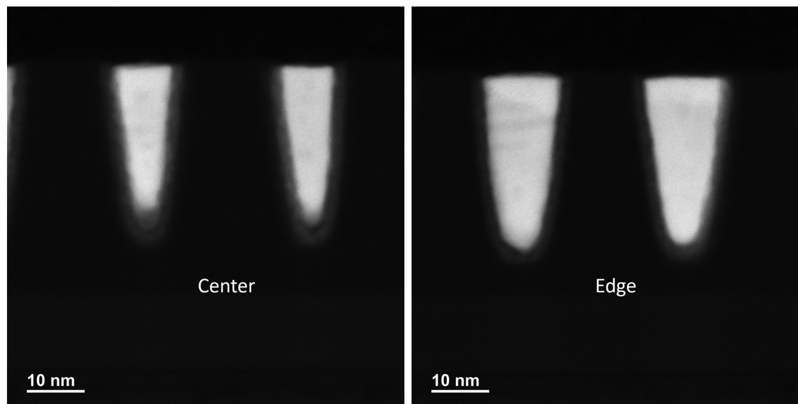


**Fig. 14** Comparison of cross-sectional transmission electron microscopy (TEM) HAADF images in a center and edge die.

electrical performance as if there were no defects, indicating no sensitivity of the scatterometry spectra to the defects.

Transmission electron microscope (TEM) along with high angle annular dark field (HAADF) detector was used to obtain the cross-sectional view of the structures in a center and edge die. The images demonstrated that in a center die, the top-CD and height of Ru lines are ∼9.5 and ∼28.0 nm, respectively, whereas, in an edge die, the top-CD and height of Ru lines were found to be ∼12.8 and ∼30.0 nm, respectively (Fig. 14). The results suggest that there is clear center to edge variation in structural size and shape which leads to the changes in the resistance value. Moreover, we obtained elemental mapping images which are shown in Fig. 15.

## 3.7 *Electrical Yield*

Common defects emerging from the litho processes are (i) resist nano-bridge, which can lead to metal break in the damascene process and (ii) resist thinning or pinching, which can cause patterning hard mask breaks, leading to metal bridges between nano-interconnects. At the end of

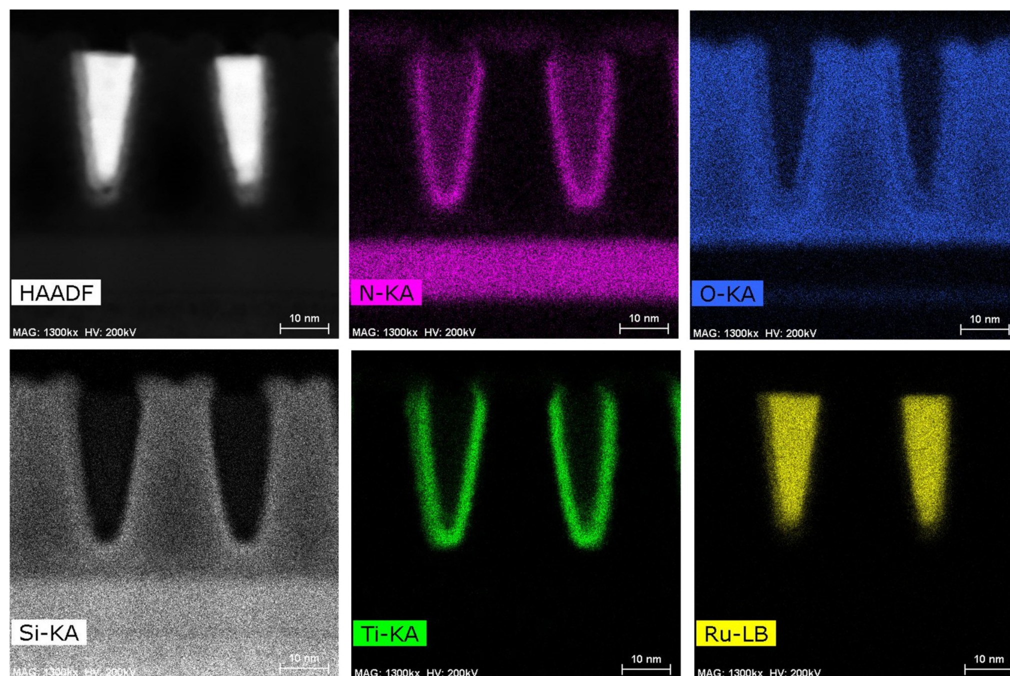


**Fig. 15** Cross-sectional HAADF and energy-dispersive X-ray spectroscopy (EDS) elemental mapping images in a center die.



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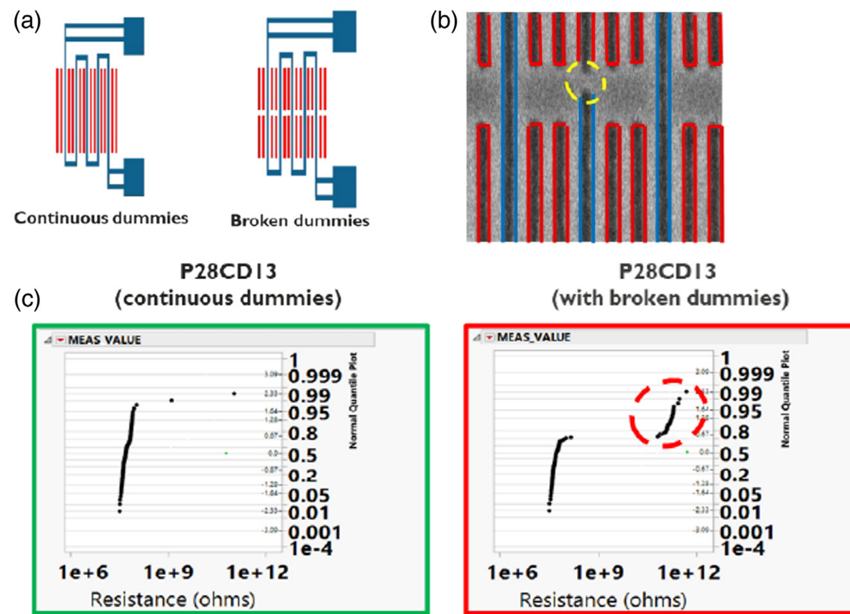


**Fig. 16** (a) Schematic of meander devices. (b) SEM image of MR devices with segmented dummy lines showing a typical HM bridge defect. The red lines are the dummies, and the blue lines are active and connected to the electrical test pads. (c) Quantile plots showing MR resistance data for design CD = 13 nm, pitch = 28 nm with continuous and segmented dummy line designs.

the process, MR and FF structures of different sizes and pitches were tested electrically and inspected using a large FOV e-beam microscope (to perform physical defect inspection). After large area e-beam analysis of the electrically failed structures, we observed failures consistent with defects originating from the resist. Therefore, conclusions on resist stochastics (through CD, pitch, dose, and focus) can be drawn from the reported electrical data and correlated with large-area physical defect inspection.

A schematic of MR structure with continuous and segmented dummy line are shown in Fig. 16(a). In an MR structure with segmented dummy lines (red lines), the SEM image showed a typical HM bridge defect [Fig. 16(b), yellow circle]. We expect the bridging to occur more often adjacent to the end-to-end spaces of the segmented dummy lines, because the active line is isolated at this location, resulting in lower contrast. The quantile plots showed better meander yield for the devices with continuous dummies, while segmented dummy lines suffered a 20% yield loss [Fig. 16(c)]. All the dies marked within the red dashed line [Fig. 16(c)] are defective, because HM bridging defects lead to metal breaks in the damascene process.

Figure 17 demonstrates the quantile plots of MR resistance data for the other 28 nm pitch devices with different active line CDs (13, 14, and 15 nm) and T2T distances of segmented dummy lines (T2T CD = 30, 40, and 50 nm). It was observed that the MR devices with only segmented dummy lines and design CD of 13 nm had significant yield loss. Contrarily, devices with design CDs of 14 and 15 nm showed very high yields, and the dummy T2T CDs seemed to have little impact on the yield (Fig. 17).

In the case of FF devices, the hard mask break causes metal bridging in the damascene process, resulting in high FF leakage. To differentiate the good dies from bad ones, we set a threshold current of $1 \times 10^{-7}$ A. For a 28-nm pitch FF device, the quantile plot demonstrated excellent yield (~95%) for the active line CD of 13 nm (Fig. 18). Interestingly, the yield was found to drop as the metal lines trend toward higher CDs (Fig. 18). The reason for this behavior is associated with the increasing chance of bridging as the metal lines widen to larger CDs of 14 and 15 nm.

Finally, the combo yields were obtained by multiplying the FF yield with the MR yield. Across the wafer, the yield was calculated for each die based on the data from 20 devices per die. It was found that large devices (a longer meander length) showed lower yield than the medium size (a shorter meander length) devices (Fig. 19). The combo yield for the large devices with CD = 14 nm was found to be 91%, which is higher than that of CD = 13 and 15 nm (Fig. 19).



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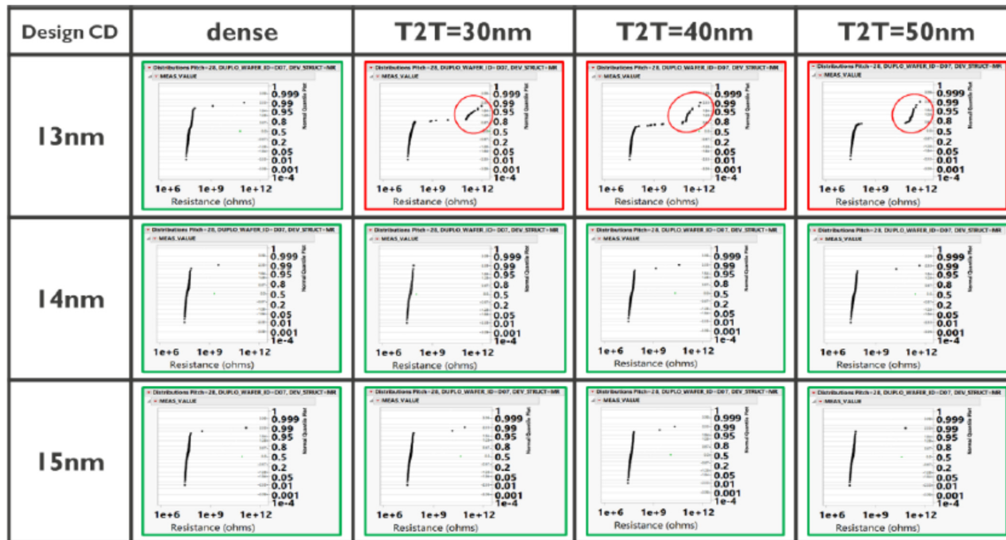


**Fig. 17** Quantile plots showing MR resistance data for 28-nm pitch MR devices with different active line CDs (13, 14, and 15 nm) and T2T distance of the segmented dummy lines (T2T CD = 30, 40, and 50 nm).

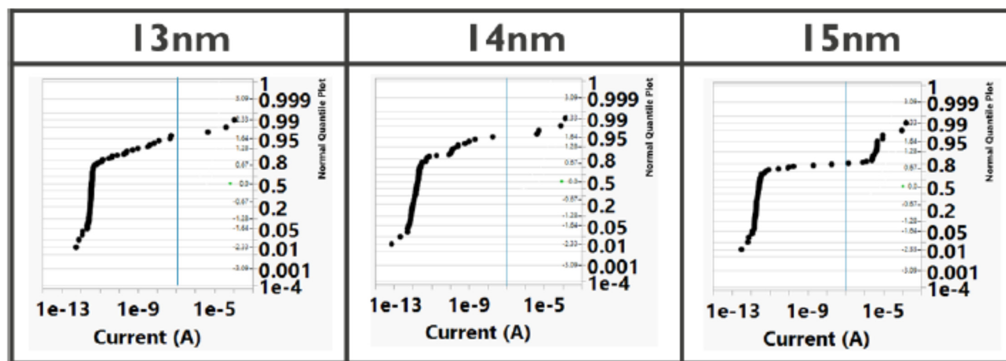


**Fig. 18** Quantile plots showing leakage current for 28-nm pitch FF devices with different active line CDs (13, 14, and 15 nm).

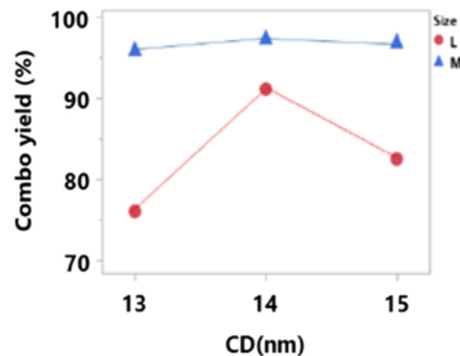


**Fig. 19** Combo yield for 28-nm pitch devices for different design CDs and sizes. L = longer meander length, M = shorter meander length.

## 3.8 *Voltage Contrast (VC) Characterization*

VC[11] is another e-beam metrology technique suitable to perform defect analysis on a large area at high speed. VC characterization was used on structures fabricated using a 28-nm metal pitch



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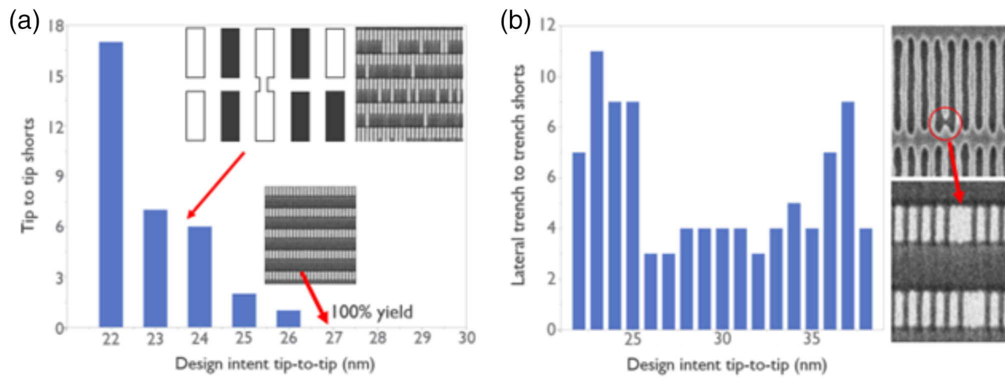


**Fig. 20** (a) Number of T2T short defects as a function of T2T design CD and (b) stochastic lateral short defects and corresponding SEM (after etching) and VC (after metallization) images.

dual damascene flow as depicted in Fig. 2. After CMP, VC inspection is expected to show a clear bright signal for metal trenches properly connected to the ground (through the via) and dark signal for floating metal. This high image contrast helps to differentiate yielding from nonyielding structures and identify different failing mechanisms.

We observed three failure modes: (i) T2T shorts, (ii) trench-to-trench shorts, and (iii) open vias. In the VC signal images, each of the failure modes showed a different signature: (i) double-length vertical white bars for T2T shorts, (ii) triple-width (or more) white bars for lateral stochastic bridges, and (iii) missing white bars for metal-via failures. Therefore, the distinct images corresponding to the failure modes facilitated yield analysis. Although typical VC metrology allows for large FOV inspection ($32\ \mu m \times 32\ \mu m$), >1500 images were acquired to cover the full DOE area. The collected images were processed by ML, and the yield and defect rates were extracted per failing mechanism. The yield and defect rates were based on 800 vias or T2T per DOE.

For T2T design CD higher than 26 nm, no T2T shorting defects were observed and 100% yield could be achieved [Fig. 20(a)]. Interestingly, stochastic side bridges were discovered close

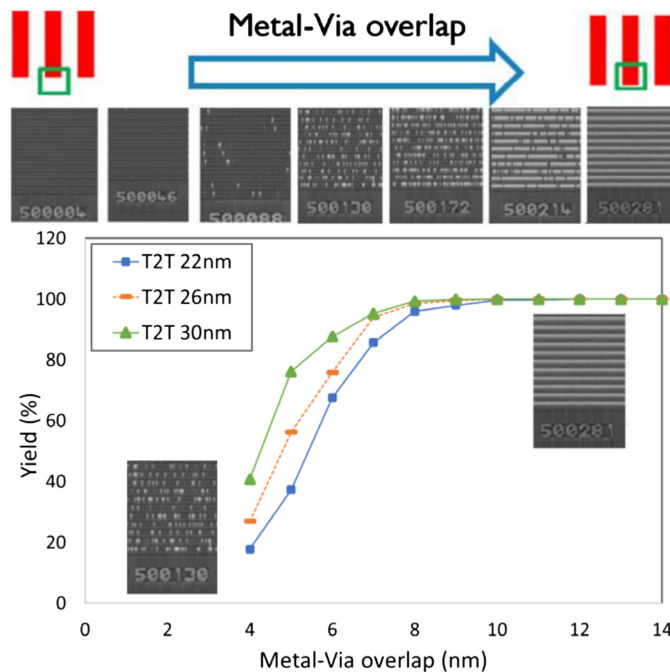


**Fig. 21** Metal-via VC yield as a function of metal-via overlap and T2T design CD.



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to the T2T location, and this defect could not be correlated to the T2T dimensions [Fig. 20(b)]. Further optical proximity correction (OPC), process, and illumination improvements are expected to reduce the number of defects for the failure mechanisms.

The metal-via contact yield, obtained for three T2T design CD, increased with increasing metal-via overlap (Fig. 21, bottom). This trend could also be discerned visually as the number of bright trenches increased with increasing metal-via overlap (Fig. 21, top). Notably, a 100% yield was achieved at metal-via overlap of ∼10 nm. In the smaller overlap region, a higher yield was achieved for a more relaxed T2T CD, because a larger T2T CD target implies an improved lithographic image contrast at the line end and therefore, a smaller variation in line-end placement.

## 4 Conclusion

We investigated the patterning of 28 nm pitch structures and used different metrology techniques combined with ML modeling to evaluate defect levels. For a Ru single damascene flow, the inspection of different T2T structures showed a higher failure rate for the short-staggered trenches. The deep learning-based defect detection was shown to suppress various noises, enabling good sensitivity when optimizing for inspection throughput. Metrology on the same platform provided field and wafer-level CD signatures for defect correlation. With a wide operating space, a large area SEM tool provides ultimate sensitivity with high coverage, leveraging on multiple unique core technologies and large FOV. Scatterometry spectra together with ML solution, demonstrated speedy measurement and good capability for inline process monitoring after HM etch (AEI) for various targets (LS and T2T, including T2T variations) and parameters. It was shown that targets smaller than the OCD spot size could also be trained and verified accurately by the ML solution. Beyond dimensional metrology, post-CMP resistance and capacitance measurements were trained and validated on multiple MR and FF structures. Since scatterometry is not sensitive to small stochastic defects, the ML training set needed to be filtered carefully due to their considerable impact on the referencing technique reading.

Investigation of the impact of resists stochastic defects showed that devices with segmented dummy lines have significant yield loss, which could be restricted by a further pupil and OPC model optimization. Electrical measurements, performed on FF and MR structures, showed failures that could be correlated with stochastic resist defects. Combined MR and FF yields were also presented for different design CDs. We demonstrated that large e-test structures can be used at the early stages of resist and patterning process development, as the electrical failures are mostly caused by resist defects, thanks to the simplicity of the short-loop process.

For a dual damascene process, we showed that VC metrology is useful to determine the design rule parameters and capture different failure mechanisms. The VC results indicated that a T2T design CD higher than 26 nm and metal-via overlap of ∼8 to 10 nm are recommended to obtain higher T2T and metal-via yield, respectively.

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defectivity issues when first immersion hoods were implemented. He contributed to more than 60 publications in SPIE.

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