Impact of Seed Annealing on the Reliability of Monolithic GaAs/Si p-n Diode Optical Phase Shifters

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Abstract *We report the reliability assessment of carrier-depletion p-n diode GaAs/Si optical modulators monolithically integrated on a 300-mm Si wafer. Dark current remains stable under long accelerating aging tests. Devices without seed annealing experience a shift of $V_{\pi}.L_{\pi}$ with no stress temperature dependence.*

Introduction

Over the past decades, the ongoing demand for optical transceivers has transitioned Silicon Photonics (SiPho) from an early research development [1] to a mature technology [2]. Leveraging its compatibility with the existing complementary metal oxide semiconductor (CMOS) platforms, it enables dense [3] and high-yield manufacturing, providing an extended library of components, both on the transmitter and receiver side [4], [5].

Even though the majority of devices are monolithically integrated using Silicon (Si) and Germanium (Ge) on a Si wafer [6], the increasing interest of light generation and amplification [3] paved the way for the integration of III-V direct bandgap materials. Going beyond laser fabrication, features like lower effective mass and higher carrier mobility are making III-V materials more suitable for high-speed electronic devices than bulk Si [7]. Recent works [8]–[10] have demonstrated a highly efficient carrier-depletion optical phase modulator, with direct growth of GaAs on Si, benefiting from the above characteristics.

Besides the many advantages, direct growth of III-V materials on Si comes with a price. Large mismatches in lattice constant and the coefficient of thermal expansion (CTE) between III-V materials and Si are some of the challenges to overcome for a high-quality monolithic integration. Threading dislocations, {111} defects and misfit dislocations formed during process, can significantly impact the dark current of those components, which eventually affects the specifications for the signal-to-noise ratio. Different approaches to reduce the defect density have been established by various groups [11]–[17] with the majority of them being based on high-temperature annealing (600 °C to 1000 °C). An alternative method is to grow the III-V material in trenches with a V-shaped bottom consisting of two {111} facets, a very beneficial approach since no specific high-temperature surface treatment is required [17]. In this paper, we report the impact of seed annealing on the performance and reliability of GaAs/Si V-groove depletion-type modulators.

Devices and experiments

The III-V/Si optical phase shifters were fabricated in imec's 300-mm CMOS pilot line, using a Silicon-On-Insulator (SOI) wafer with a 215 nm top Si layer on a 2 µm thick Buried Oxide. N-type doped GaAs was grown using a two-step Selective-area Epitaxial Growth on V-groove Si trenches, with an optional seed annealing step at 530 °C between them, followed by a p-type and n-type Si implantation to form the near-vertical p-n junction. Details on the GaAs growth and all implant conditions can be found in [18] and [10], respectively. Finally, after Chemical Mechanical Polishing, a GaAs thickness of 70-90 nm above the Si rib is reached. A detailed cross-section is shown in Fig. 1 and Tab. 1 describes the different dimensions.

Tab. 1: List of parameters and dimensions used in this work for a 500 µm-long device.

Parameter	Value [nm]
III-V thickness on Si rib (*tIIIV*)	70~90
III-V width (*wIIIV*)	240
III-V depth (*dIIIV*)	170
Distance between center to p-n junction (*wJt*)	100

For this study, 500 µm-long devices with and without seed annealing have been selected. Package-level accelerating aging tests were with T_{stress} conditions of 150 °C, 175 °C and 85 °C/85 % Relative Humidity (RH), biased at V_{stress} of -5 V. During these stress conditions, we monitored

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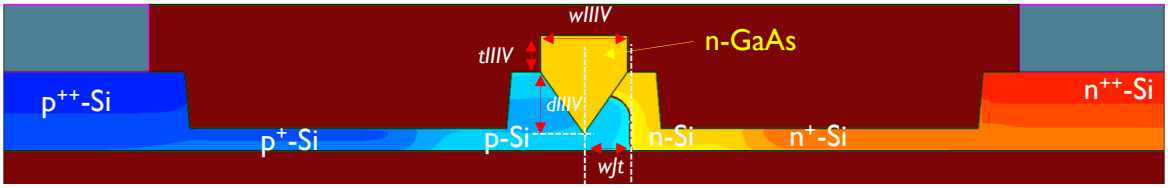

Fig. 1: Cross-section of the GaAs/Si optical phase shifter.

the dark current shift for up to 5000 h of stress time, while the electro-optical performance of the components was evaluated at room temperature and at different time intervals.

Stress results

Accelerated aging tests are performed at high temperatures for long stress times, while the stress sequence is interrupted at regular intervals for dark current and electro-optical measurements at lower conditions. Selecting the highest applied T_{stress} = 175 °C and plotting the dark current at 85 °C and -5 V, it is clear from Fig. 2, that there is no significant impact of the seed annealing step on both the initial dark current and its degradation. Hence, the devices are considered as electrically reliable components.

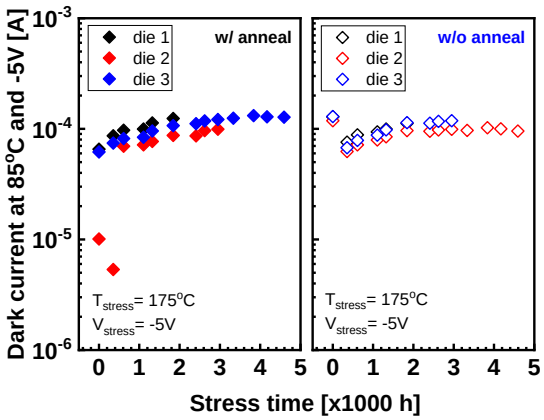

Fig. 2: Dark current evolution at operating conditions, for stress at 175 °C and -5 V, indicating no impact of seed annealing step.

Failure analysis was carried out on two identical stressed samples (175 °C and -5 V for 5000 h), from each process condition, using dark-field scanning transmission electron microscopy (DF-STEM). From the zoomed-in cross-sections shown in Fig. 3, the presence of threading dislocations is evident in the GaAs, while misfit dislocations are appearing at the GaAs/Si interface of the V-groove, as very bright contrast lines. Additionally, {111} defects are highlighted in the figure, but are more clearly detectable in a different imaging condition, the two-beam bright-field (BF) TEM, that is not presented here. Even though the seed annealing step reduces the threading dislocations inside the bulk GaAs, the

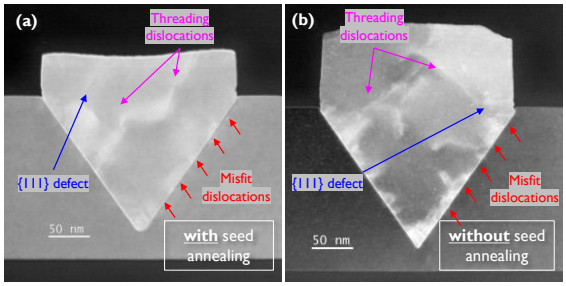

Fig. 3: DF-STEM of the GaAs/Si cross-sections on stressed devices (a) with and (b) without seed annealing, both with observable threading dislocations in the GaAs and misfit dislocations at the III-V/Si interface.

fact that I_{dark} is similar between the two types of components, could be attributed mainly to the contribution of GaAs/Si interface defects.

This assumption is further confirmed by using the strain TEM nano-beam diffraction technique (NBD) on a 'fresh' and electrically stressed device (150 °C and -5 V for 5000 h), without the seed annealing step. From Fig. 4, it can be depicted that there's no observable difference between the two samples. Some local strain is revealed, particularly in proximity of the defects, but the measured mismatch w.r.t. the reference (taken at the top GaAs) is very low and close to the sensitivity limit of the NDB method, for both.

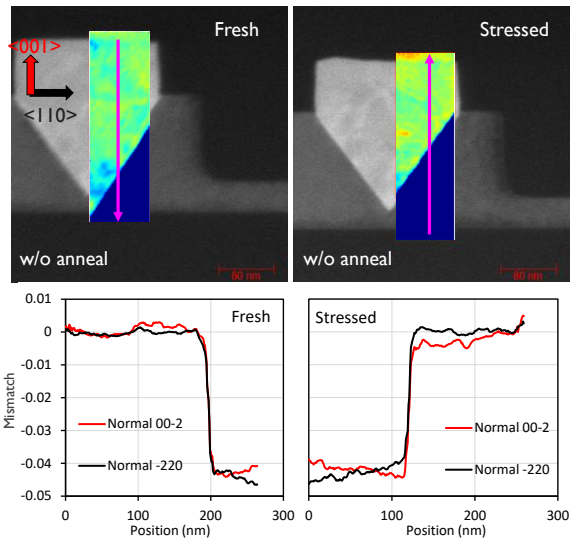

Fig. 4: Comparison between an untreated and electrically stressed optical phase shifter, using strain TEM NBD technique, having similar trends without any difference manifesting in the strain.

Electro-optical performance after stress

At different time intervals, the performance of stressed optical phase shifters was evaluated. Specifically, the monitored parameter is one that indicates the modulation efficiency, $V_\pi.L_\pi$ which is the product of the voltage and the phase-shifter length for a π-phase shift. All measurements were performed at room temperature and the extracted values are compared with the wafer-level t_0 data in Fig. 5.

Data points at zero stress time, represent the reference, un-stressed devices in each case, that have been measured on wafer-level (in black) and on package-level (in red). For the phase shifters subjected to the additional seed annealing step, $V_\pi.L_\pi$ values appear to be already very low before stress, while they remain unaffected for up to 5000 h of electrical stress. On the other hand, the components without this extra process step, are gradually degrading w.r.t. the applied stress time. The fact that different temperatures lead to similar degradation trends indicates that the observed degradation is a more bias-driven effect than a temperature related one.

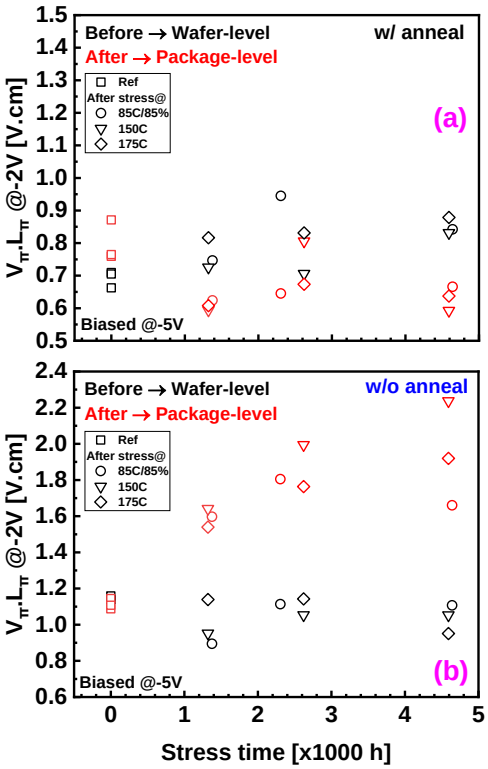

Fig. 5: $V_\pi.L_\pi$ values shift .w.r.t. t_{stress} for different stress conditions. Devices with (a) seed anneal appear to have an improved performance, while the ones without (b) are gradually degrading.

It is known that the $V_\pi.L_\pi$ is inversely proportional to the change of the effective refractive index (Δn_{eff}) that is directly correlated to the depletion width of the junction and therefore, with the junction capacitance. From Fig. 6, we can see that the higher reverse bias is applied, the wider the depletion region becomes, covering completely the GaAs/Si interface.

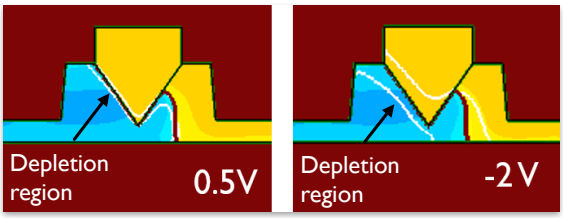

Fig. 6: Depletion width of the vertical p-n junction becoming wider with increasing reverse bias, pointing out to the contribution of the interface quality to the junction capacitance.

One possible explanation for the optical stability of the annealed devices, is the passivation, due to high temperature, of the pre-existing dangling bonds. On the other hand, the phase shifters, not being subjected to the seed annealing step, are potentially experiencing an increase of the dangling bonds with longer stress times, that eventually leads to the measured $V_\pi.L_\pi$ increase.

Conclusions

A detailed reliability study on GaAs/Si p-n diode optical phase shifters was presented in this work. The long-term stability of the modulators was evaluated w.r.t. an optional seed annealing process step between the two-step epitaxy process. Dark current remains stable after up to 5000 h of electrical stress, at different conditions. Finally, the seed annealing step at 530 °C, can be used to revoke the modulation efficiency ($V_\pi.L_\pi$) degradation before and after stress.

Acknowledgements

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