

Opto-Electronic Advances

ISSN 2096-4579

CN 51-1781/TN

Low-loss chip-scale programmable silicon photonic processor

Yiwei Xie, Shihan Hong, Hao Yan, Changping Zhang, Long Zhang, Leimeng Zhuang and Daoxin Dai

Citation: Xie YW, Hong SH, Yan H, Zhang CP, Zhang L et al. Low-loss chip-scale programmable silicon photonic processor. *Opto-Electron Adv*, 6, 220030(2023).

<https://doi.org/10.29026/oea.2023.220030>

Received: 8 February 2022; Accepted: 4 May 2022; Published online: 31 October 2022

Related articles

All-optical computing based on convolutional neural networks

Kun Liao, Ye Chen, Zhongcheng Yu, Xiaoyong Hu, Xingyuan Wang, Cuicui Lu, Hongtao Lin, Qingyang Du, Juejun Hu, Qihuang Gong
Opto-Electronic Advances 2021 4, 200060 doi: [10.29026/oea.2021.200060](https://doi.org/10.29026/oea.2021.200060)

An advanced III-V-on-silicon photonic integration platform

Yingtao Hu, Di Liang, Raymond G. Beausoleil
Opto-Electronic Advances 2021 4, 200094 doi: [10.29026/oea.2021.200094](https://doi.org/10.29026/oea.2021.200094)

Optical multiplexing techniques and their marriage for on-chip and optical fiber communication: a review

Svetlana Nikolaevna Khonina, Nikolay Lvovich Kazanskiy, Muhammad Ali Butt, Sergei Vladimirovich Karpeev
Opto-Electronic Advances 2022 5, 210127 doi: [10.29026/oea.2022.210127](https://doi.org/10.29026/oea.2022.210127)

Ultrahigh-resolution on-chip spectrometer with silicon photonic resonators

Long Zhang, Ming Zhang, Tangnan Chen, Dajian Liu, Shihan Hong, Daoxin Dai
Opto-Electronic Advances 2022 5, 210100 doi: [10.29026/oea.2022.210100](https://doi.org/10.29026/oea.2022.210100)

More related article in Opto-Electron Journals Group website 



<http://www.oejournal.org/oea>



 OE_Journal



 @OptoElectronAdv

DOI: [10.29026/oea.2023.220030](https://doi.org/10.29026/oea.2023.220030)

Low-loss chip-scale programmable silicon photonic processor

Yiwei Xie^{1†}, Shihan Hong^{1†}, Hao Yan¹, Changping Zhang¹, Long Zhang¹,
Leimeng Zhuang² and Daoxin Dai^{1,3*}

Chip-scale programmable optical signal processors are often used to flexibly manipulate the optical signals for satisfying the demands in various applications, such as lidar, radar, and artificial intelligence. Silicon photonics has unique advantages of ultra-high integration density as well as CMOS compatibility, and thus makes it possible to develop large-scale programmable optical signal processors. The challenge is the high silicon waveguides propagation losses and the high calibration complexity for all tuning elements due to the random phase errors. In this paper, we propose and demonstrate a programmable silicon photonic processor for the first time by introducing low-loss multimode photonic waveguide spirals and low-random-phase-error Mach-Zehnder switches. The present chip-scale programmable silicon photonic processor comprises a 1×4 variable power splitter based on cascaded Mach-Zehnder couplers (MZCs), four Ge/Si photodetectors, four channels of thermally-tunable optical delaylines. Each channel consists of a continuously-tuning phase shifter based on a waveguide spiral with a micro-heater and a digitally-tuning delayline realized with cascaded waveguide-spiral delaylines and MZSs for 5.68 ps time-delay step. Particularly, these waveguide spirals used here are designed to be as wide as 2 μm, enabling an ultralow propagation loss of 0.28 dB/cm. Meanwhile, these MZCs and MZSs are designed with 2-μm-wide arm waveguides, and thus the random phase errors in the MZC/MZS arms are negligible, in which case the calibration for these MZSs/MZCs becomes easy and furthermore the power consumption for compensating the phase errors can be reduced greatly. Finally, this programmable silicon photonic processor is demonstrated successfully to verify a number of distinctively different functionalities, including tunable time-delay, microwave photonic beamforming, arbitrary optical signal filtering, and arbitrary waveform generation.

Keywords: silicon photonics; programmable; photonic integrated circuit; waveguide; delay lines; Mach-Zehnder interferometer

Xie YW, Hong SH, Yan H, Zhang CP, Zhang L et al. Low-loss chip-scale programmable silicon photonic processor. *Opto-Electron Adv* 6, 220030 (2023).

Introduction

Chip-scale programmable optical signal processing is a new paradigm that aims at designing common integrated photonic configurations for implementing a variety of functionalities. Basically, it can be elaborated flex-

ibly for basic or more complex operations across different fields such as telecommunications, radar, lidar, quantum and artificial intelligence^{1–8}. Although showing a great range of functionalities, implementing programmable optical processor usually requires a large-scale

¹Centre for Optical and Electromagnetic Research, State Key Laboratory for Modern Optical Instrumentation, Zhejiang Provincial Key Laboratory for Sensing Technologies, Zhejiang University, Zijingang Campus, Hangzhou 310058, China; ²Imec USA, Nanoelectronics Design Center, Inc., 194 Neocity Way, Kissimmee, FL34744, USA; ³Ningbo Research Institute, Zhejiang University, Ningbo 315100, China.

[†]These authors contributed equally to this work.

*Correspondence: DX Dai, E-mail: dxdai@zju.edu.cn

Received: 8 February 2022; Accepted: 4 May 2022; Published online: 31 October 2022



Open Access This article is licensed under a Creative Commons Attribution 4.0 International License.

To view a copy of this license, visit <http://creativecommons.org/licenses/by/4.0/>.

© The Author(s) 2023. Published by Institute of Optics and Electronics, Chinese Academy of Sciences.

optical system that comprises a combination of many basic building elements. Silicon photonics have been considered as one of the most promising options for realizing large-scale programmable optical processors because of its complementary metal-oxide semiconductor (CMOS) compatibility, high integrated density as well as high thermal-tuning efficiency^{9–12}. In addition, it is very convenient to integrate passive and active silicon photonic devices monolithically.

To date, a variety of photonic integrated circuit (PIC) topologies for programmable silicon photonic processors have been demonstrated, including finite impulse response filters (FIR) with delayline arm⁸, Mach-Zehnder interferometers (MZIs) cascaded with delaylines^{13–18}, subwavelength grating waveguides^{17–18}, arrayed waveguide gratings¹⁹, cascaded ring resonators^{20–24}, and MZI-based squared/hexagonal/triangular mesh networks⁶. Among them, the topology comprising switches and delaylines offers high design flexibility and easy incorporation of tuning elements. These features support custom-synthesis of processing responses in both time- and frequency-domains, i.e., impulse responses and spectral responses. Although a number of programmable silicon photonic processors based on delaylines/switches have been demonstrated^{13–18}, it is still very challenging to develop large-scale programmable PICs with a large number of tuning elements.

The first challenge is how to significantly lower the loss of silicon photonic waveguides^{25–29}, regarding that regular silicon photonic waveguides usually have a propagation loss of ~ 2 dB/cm. As it is well known, the loss of optical waveguides mainly comes from the material loss, the scattering loss at surfaces, the substrate leakage loss as well as the bending loss. For silicon photonic waveguides, the scattering loss due to the surface roughness is the dominant. In the past decades, tremendous efforts have been devoted to reduce the propagation loss by using the following two typical approaches. One is to smoothen the waveguide sidewalls with some special fabrication processes, and the other is to reduce the light-matter interaction at the rough sidewalls by manipulating the mode distribution. Griffith et al. fabricated a silicon photonic waveguide with a propagation loss of 0.9 dB/cm using etchless processes³⁰. Alternatively, one can also reduce the scattering loss by decreasing the sidewall area. Zhou et al. demonstrated a 60-nm-thick silicon photonic waveguide with a lowered loss of 0.6 dB/cm¹⁵, which is owing to reduced sidewall areas. This type of

low-loss waveguide was then used for developing a tunable real-time delayline¹⁴, which can perform the time delay of 0 to 1.27 ns with a step of 10 ps. Moreover, a delayline array has also been proposed by integrating multiple channels^{3,31}. In addition, a shallowly-etched silicon photonic ridge waveguide has also shown a low loss of around 0.3 dB/cm, which is due to less overlap between the mode field and the side walls. Later, Dong et al. presented a silicon photonic ridge waveguide with a large cross section of $2.0 \mu\text{m} \times 0.25 \mu\text{m}$, showing a low loss of 0.27 dB/cm³². For these optical waveguides, however, the bending radius is usually quite large because of the weak mode confinement. Furthermore, their fabrication is not fully compatible with current multi-project-wafer (MPW) foundry processes. Therefore, it is still challenging to achieve low-loss silicon photonic devices that can be fabricated with standard MPW processes.

In addition, complex programmable optical processors usually require hundreds or even thousands of tuning elements, like Mach-Zehnder switches (MZSs). There might be some significant random phase errors caused by the fabrication imperfection for the phase shifters of those MZS elements. These phase errors can be compensated through some complicated and careful calibration. Currently some special approaches for auto-routing and self-configuration have been proposed and attracted intensive attention^{33,34}. Unfortunately, the calibration is still quite complicated because it usually entails additional on-chip feedback control schemes with the help of many additional elements (such as tap couplers and power monitors) and sophisticated characterization procedures^{8,14,35}. Furthermore, the compensation requires extra power consumption^{8,14}.

In this work, we present a fully-integrated programmable silicon photonic processor by integrating a 1×4 variable power splitter based on Mach-Zehnder couplers (MZCs), four photodetectors, as well as four channels of tunable delaylines with MZSs. Particularly, for the optical delaylines, ultra-low-loss waveguide spirals with a cross section of $2.0 \times 0.22 \mu\text{m}^2$ are used, while a tapered Euler-curve S-bend is introduced at the center of the spiral to minimize the loss and suppress the generation of higher-order modes. Meanwhile, the width of the phase shifters in the arms of the MZSs and MZCs is widened to $2 \mu\text{m}$ for achieving low random phase errors due to the fabrication imperfection. For the present silicon photonic processor, the chip area is about 4.9 mm^2 ,

and each channel of tunable delayline has a continuously tuning range up to 176 ps while the waveguide propagation loss is about 0.28 dB/cm. The present silicon photonic processor chip exhibits some unique advantages compared to those existing delayline technologies, including the wide tuning range, the reconfigurability, the high resolution, and the low loss. In addition, the chip can also be configured for distinctively different functionalities of signal processing, including tunable delays, beam steering/forming, arbitrary optical signal filtering, and arbitrary waveform generation.

Structure and design

Figure 1 shows the schematic of the present programmable silicon photonic processor, which consists of a $1 \times N$ tunable optical power splitter based on MZCs, N channels of optical delaylines with MZSs, N channels of PDs and a $N-1$ coupler array. There are P input ports (i.e., $\#I_1, \#I_2, \dots, \#I_P$) at the left side for inputting optical signals, while there are P output ports (i.e., $\#O_1, \#O_2, \dots, \#O_P$) at the right side for outputting optical signals, where P is $2 \cdot \log_2(N)$. Alternatively, optical signals at the output side can also be converted to electrical signals and read from the PDs integrated on the same chip. Here each MZC works as a photonic processing unit to enable programmable path-selecting, as well as power splitting/combining. Each channel of optical delayline comprises a continuously fine-tuning waveguide spiral delayline with a micro-heater and a M -bit digitally-tuning delayline with $(M+1)$ thermo-optic MZSs.

This topology allows to tune the time delay difference between adjacent channels for achieving high flexibility. The MZSs labeled by V_{nm} ($m=1, \dots, M$) are used to

tune the time delay of the N -th channel from 0 to $(2^M-1)\Delta t$ with a step of Δt . Such an architecture using spirals in cascade and binary-tree-structured MZCs minimizes the chip footprint and the circuit complexity, and also guarantees the flexible control of the amplitude and delay for each channel. MZCs on the same stage are connected to previous stage of MZCs with equally-long waveguides, so that the delay difference between any two channels is determined by the corresponding delay lines. Meanwhile, the 1% : 99% power splitters are introduced at each stage for monitoring the MZS state. Besides, there are multiple additional testing ports allowing to independently access to different sections of the chip, simplifying the device characterization and increasing the operation flexibility. By means of programming the tunable elements, this chip is able to provide distinct functionalities of signal processing. For example, the present chip can be modelled as N -channel optical true time delayline with PDs for beam steering, or a 2×2 tapped delayline filter for arbitrary filtering and arbitrary waveform generation.

For all MZCs and MZSs on the chip, the concept of low-phase-error 2×2 thermo-optic MZSs proposed in our previous work³⁶ is utilized here, as shown in Fig. 2(a). The MZS consists of two 2×2 3-dB multimode interference (MMI) couplers and two symmetric MZS arms. Here a micro-heater is introduced on the upper arm, as shown in Fig. 2(b), where the SiO_2 upper-cladding layer between the silicon core and the micro-heater is designed to be $1 \mu\text{m}$, to balance the absorption loss from the TiN heater and the heating efficiency as well as the heating response time. Particularly, the core-width of the phase shifter in the arms is broadened to be $2 \mu\text{m}$, so

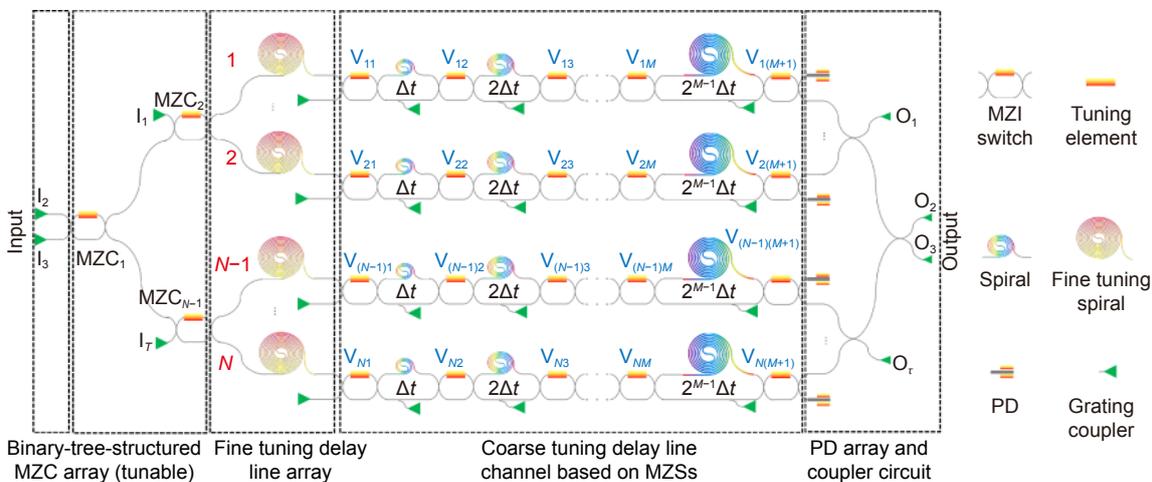


Fig. 1 | Schematic of an on-chip optical signal processor.

that the random phase errors due to the fabrication imperfection can be reduced significantly, compared to the conventional MZS with 0.45- μm -wide singlemode phase shifters. This feature could notably reduce the calibration complexity and the power consumption, and thus possibly paves the way for large-scale silicon photonic processor.

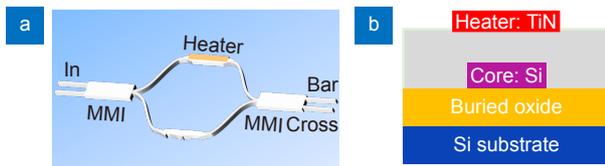


Fig. 2 | Schematic configuration of the present 2×2 thermo-optic MZS incorporating widened phase-shifter waveguides. (a) Top view. **(b)** Cross section of the MZS arm with a micro-heater.

On the other hand, loss reduction is always considered as one of the most fundamental and critical issues in the development of large-scale photonic chip. In order to achieve low-loss and compact waveguide structures, we use a silicon photonic waveguide consisting of a multimode-waveguide Archimedean spiral and a tapered Euler-curve S-bend, as shown in Fig. 3(a). Here the input section consists of a bent adiabatic taper waveguide, which is used to connect the 500-nm-wide singlemode section to the multimode section. Figure 3(b) shows the calculated result for the scattering loss in a silicon photonic waveguide as the core width w_{co} varies. Here, a three-dimensional volume current method^{35,37–39} was used for evaluating the loss due to the scattering at the waveguide interfaces. For the loss calculation, we assume that the mean square deviation of the sidewall roughness σ_{sidewall} is about 4 nm and the top/bottom surface roughness σ_{surface} is fixed as 0.4 nm, as estimated from the fabrication samples. From Fig. 3(b), it can be

seen that the total transmission loss becomes reduced significantly when the core width increases. Ultimately, here we choose the waveguide core width as $w_{\text{co}} = 2 \mu\text{m}$.

The tapered Euler-curve S-bend locating at the center of the spiral is defined as^{39,40}:

$$\frac{d\theta}{dL} = \frac{1}{R} = \frac{L}{A^2} + \frac{1}{R_{\text{max}}}, \quad (1)$$

where L is the curve length, $A = [L_{\text{max}} / (1/R_{\text{min}} - 1/R_{\text{max}})]^{1/2}$, L_{max} is the total length of the waveguide bend. In the designed modified-Euler bend, the bending radii (varied gradually from the maximum R_{max} to the minimum R_{min} and back to R_{max}) and the core widths (varied gradually from the maximum W_m to the minimum W_s) should be designed carefully in order to avoid higher-order mode excitation^{39,40}. The excess loss and the crosstalk for the cases with different bending radii and core widths are simulated by Lumerical finite difference time-domain (FDTD). Ultimately, the curvature radii R_{max} and R_{min} for the S-bend are respectively chosen as 25 μm and 10 μm , while the waveguide widths W_s and W_m are chosen as 0.6 μm and 2 μm , respectively.

Results

We design a proof-of-concept chip by using silicon photonic waveguides with 220-nm-thick silicon core and a 2- μm -thick buried oxide (BOX) layer. As shown in Fig. 4(a), this configuration comprises four channels (i.e., $N = 4$), each of which has five stages of waveguide spirals integrated with six 2×2 MZSs (i.e., $M = 5$). These five stages of waveguide spirals have time delays of $2^0\Delta t$, $2^1\Delta t$, $2^2\Delta t$, $2^3\Delta t$, and $2^4\Delta t$, respectively, where $\Delta t = 5.68$ ps. The reason for such a time delay design is to achieve microwave photonic processing covering Ku and K bands (see more details in Section *Tunable delay line and microwave*

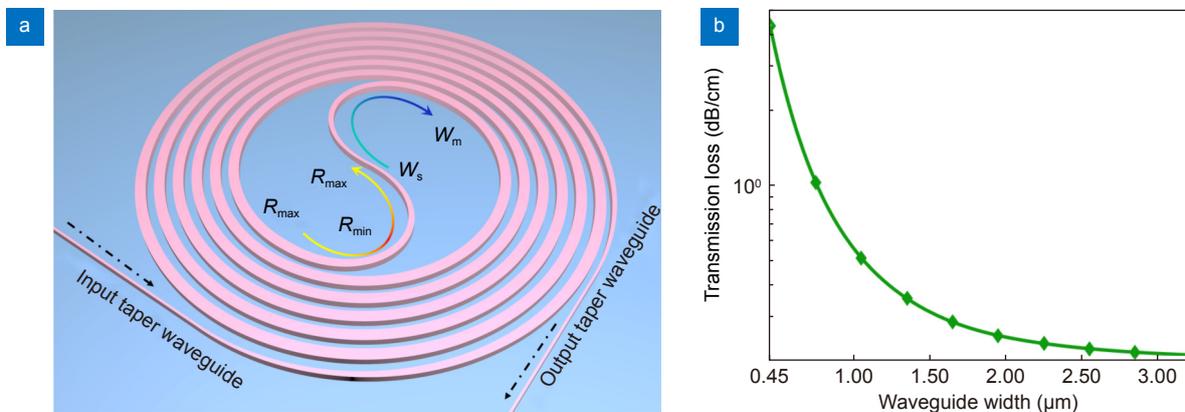


Fig. 3 | (a) 3D-view of the low-loss waveguide spiral. **(b)** Calculated scattering loss as the waveguide core width increases at the wavelength of 1550 nm.

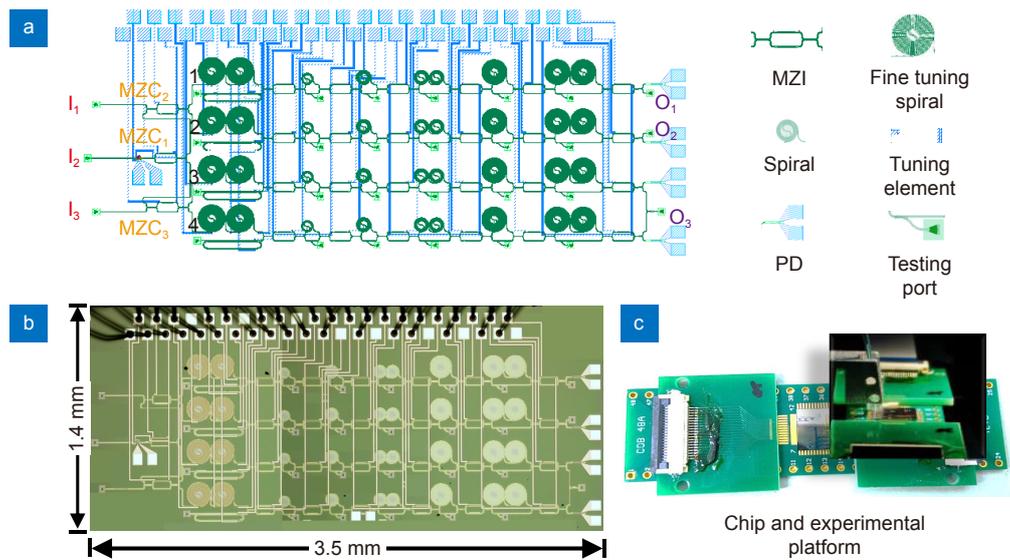


Fig. 4 | (a) Layout of the chip and the basic building blocks. (b) A photo of the fabricated chip. (c) A photo of the packaged chip.

photonic beamformer). Figure 4(b) shows the fabricated chip, which has a footprint of 4.9 mm². As shown in Fig. 4(c), the chip was packaged by wire-bonding all heater pads to a printed-circuit-board carrier while the fiber arrays were used for optical coupling.

Characterization of key elements

Low-phase-error MZSs

Figure 5(a) and 5(b) show the microscopy picture of the fabricated low-phase-error MZS with 2- μ m-wide phase shifters. The transmissions at the cross- and bar-ports of this MZS were then measured by sweeping the heating power from 0 to 60 mW when it operates at 1550 nm, as shown in Fig. 5(c). It can be seen that a heating power of 21 mW is needed to generate a phase shifting of π . We also measure the transmission spectra at the cross and bar-ports in the wavelength range from 1520 nm to 1580 nm when it is OFF and ON respectively, as shown in Fig. 5(d). It can be seen that the excess losses are low (\sim 0.4 dB) and the extinction ratios are $>$ 20 dB in a large bandwidth of $>$ 60 nm. The switch speed was also characterized, as shown in Fig. 5(e). It can be seen that the rise/fall time of the optical switching is about 20 μ s/14 μ s. For the present MZS, the applied power Q_0 for the OFF state is almost zero, owing to the low phase errors in the widened phase shifters, as proposed in our previous paper³⁶. Figure 5(f) shows the measured results for the ratio Q_0/Q_π for all MZSs on the same chip, where Q_π is the power to generate an additional phase shifting of π needed for the ON state. It can be seen that the ratios Q_0/Q_π for all MZSs are smaller than 0.05, which is much

lower than those conventional MZS with 0.45- μ m-wide singlemode phase-shifters. This further validates the excellent fabrication tolerance for the present MZS, which is nearly calibration-free. Such a property can help reduce the calibration complexity and the power consumption greatly, particularly for a system with a large number of MZS elements.

Digitally-tuning delay line

Figure 6(a) shows the picture of a single channel of 5-bit digitally-tuning delay line. The MZSs are switched thermally by heating the micro-heaters controlled by a multichannel voltage source (XPOW40AX-CCvCV-U, Nicslab). Figure 6(b) shows the zoom-in picture of the waveguide-spiral delayline at Stage #5. Figure 6(c) shows the measured optical output waveforms of the 5-bit digitally-tuning delay line as the time delay varies from 5.68 ps (i.e., Δt) to 90.88 ps (i.e., $2^4\Delta t$). The total length of the waveguide spirals used for a single channel is about 1.4 cm. The measured propagation loss of the waveguide spiral with the cross section of 2000 \times 220 nm² is about 0.28 dB/cm, which is much lower than that of those regular 450 \times 220 nm² silicon photonic waveguides. When the present 5-bit digitally-tuning delay line is switched from the shortest path to the longest path, the measured total loss from port I_1 to port O_1 increases from 3.0 dB to 3.4 dB, which includes the losses from the fine-tuning waveguide spirals, the MZCs, the MZSs, and the digitally-tuning spirals. In addition, the measurement shows that the loss of each MZS is lower than 0.4 dB by subtracting the excess loss of the delay lines from the total loss.

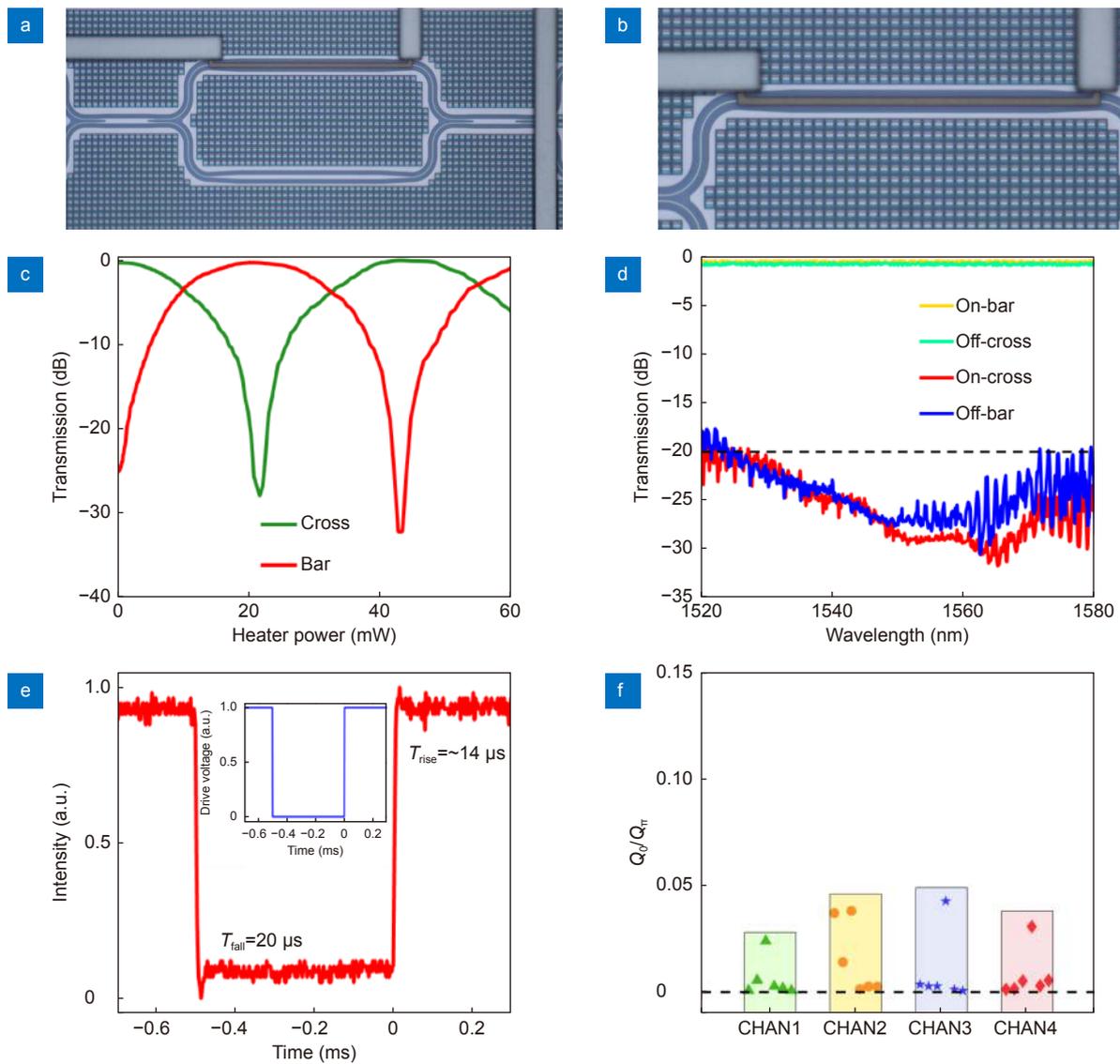


Fig. 5 | Measurement results of a representative MZS device with 2- μm -wide phase shifters. (a) Optical microscope image. (b) Zoom-in picture of the heater on the MZS's arm. (c) Transmissions at the cross and bar-ports for the central wavelength as a function of the heating power. (d) Transmission spectra for the off-state and the on-state. (e) The switching time of the MZS. (f) Normalized power consumption for compensating the phase error in MZSs for different channels.

Continuously-tuning delay line

Figure 7(a) shows the waveguide spirals with a heater used for continuously-tuning delay line. Here the delay line is designed with two waveguide spirals in order to reduce the overall footprint as well as the maximal voltage required. When the waveguide spirals are heated, the group index of the fundamental mode is modified and thus the time delay Δt_{CT} is changed accordingly by⁴¹

$$\Delta t_{\text{CT}} = \frac{L}{c} \kappa \Delta T, \quad (2)$$

where L is the length of the delay line, c is the speed of light, κ is the thermo-optic coefficient of silicon photonic waveguide mode and ΔT is the temperature change. In

the present case, the length of the heater is chosen as 9.5 mm according to the heater requirement.

Figure 7(b) shows the measured waveforms when different heating powers are applied to one of the spirals. It can be seen that the time delay change is about 3.15 ps when the heating power of 0.42 W is applied. Definitely, the time delay change is doubled to be 6.3 ps when both spirals are heated. Figure 7(c) gives the measured continuously-tuning time delay as the heating power increases. The delay time changes almost linearly as respect to the applied power, showing that the heating efficiency is about 12.05 ps/W for one heating spiral. In order to avoid any thermal crosstalk, the separation

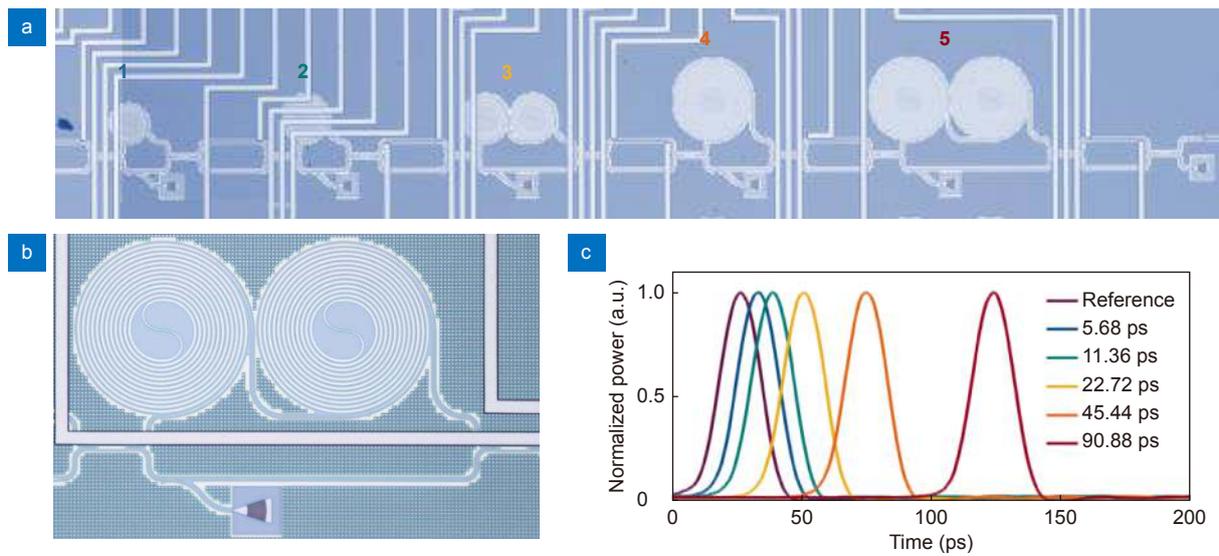


Fig. 6 | (a) A single channel of 5-bit delay line. (b) Zoom in picture of the waveguide spiral for stage 5. (c) measured optical output waveforms of the 5-bit digitally-tuning delay line as the time delay varies from 5.68 ps (i.e., Δt) to 90.88 ps (i.e., $2^4\Delta t$).

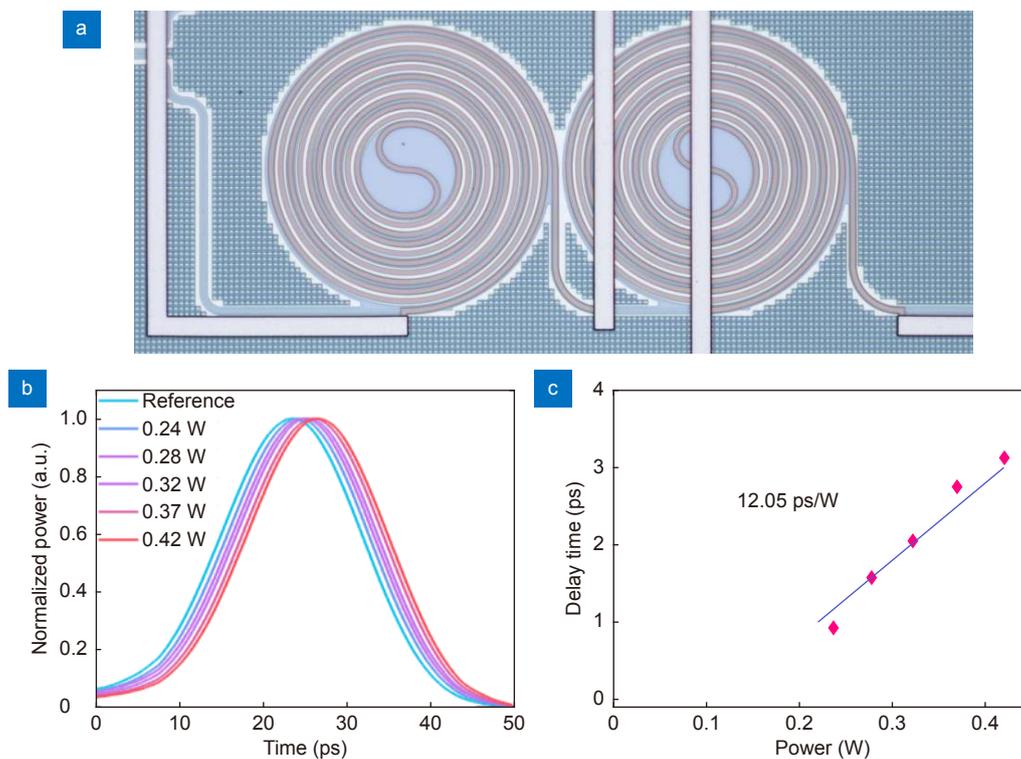


Fig. 7 | (a) Waveguide spiral carpeted with a heater for continuously-tuning delay line. (b) Time-domain impulse responses for the cases with different heating powers for one heating spiral. (c) The delay time as the heating power increases for one heating spiral.

between the heaters on the fine-tuning waveguide spiral and the subsequent digitally-tuning delay line is as large as >0.2 mm. In our experiments, no obvious thermal crosstalk was observed. What's more, this power consumption can be reduced by shortening the delay difference, Δt , or adding air-trenches at the sides/bottom of the waveguides^{42,43}.

Ge/Si waveguide photodetectors

Ge/Si waveguide photodetectors are used for the present programmable silicon photonic processor, as shown in Fig. 8(a). Here the design with lateral doped-silicon regions is introduced. Figure 8(b) shows the measured dark current of the PD as a function of the reverse bias voltage. It can be seen that the dark current is about ~ 36 nA

when operating at 1 V and the corresponding responsivity is about 0.80 A/W. Figure 8(c) shows the measured spectral responses of the fabricated Ge/Si PD when operating with different bias voltages. It can be seen that the 3-dB bandwidth is over 30 GHz when the bias voltage is set as -3 V. Furthermore, we also measured the eye-diagrams for receiving 40 Gb/s OOK signals with the present waveguide PDs at each channel, as shown in Fig. 8(d), respectively. The measured extinction ratio of these 40-Gbps eye diagrams is around 6 dB. In this experiment, the power of the modulated optical signal is 8.8 dBm, and a reverse bias voltage of 2 V was applied to the PD via a bias-tee. These measurement results show that the present Ge/Si waveguide photodetectors work with high performances and satisfy the demands of developing programmable silicon photonic processors.

Tunable delay line and microwave photonic beamformer

In modern radar systems, microwave phased array antennas usually play an important role. The traditional electronic phased array radar is bulky and has a limited bandwidth, which causes beam squinting. To solve this issue, optical true time delay line (OTTDL) has been in-

troduced as an effective solution by steering the beam at a same angle for a wide bandwidth to solve the bandwidth limitation of traditional electronic phased array antennas. By controlling the phases and the amplitudes of OTTDL transmissions, it is possible to achieve beam steering and beam forming^{14–16,31,42,44,45}, and satellite navigation communications and automotive ranging radars for Ku and K band have attracted people's attention. The present chip-scale programmable silicon photonic processor can be configured as 4-channel OTTDL for 18 GHz microwave signal and demonstrate the beamformer covering the Ku and K band.

As shown by the blue solid lines in Fig. 9(a), the optical signal launched from port I_2 was split into four channels with any desired power ratios controlled by the 1×4 tunable MZCs, and finally received by the corresponding Ge/Si PDs at the end. Since each channel of the 4-channel OTTDL has 5-bit delay states, there are 2^5 delay states available flexibly by controlling the MZCs. For the 18 GHz microwave photonic beamformer, the minimum delay time $\Delta\tau$ is given by¹⁶

$$\Delta\tau = \frac{2d\sin\theta_m}{cN_\theta}, \quad (3)$$

where d is the distance between the adjacent antenna

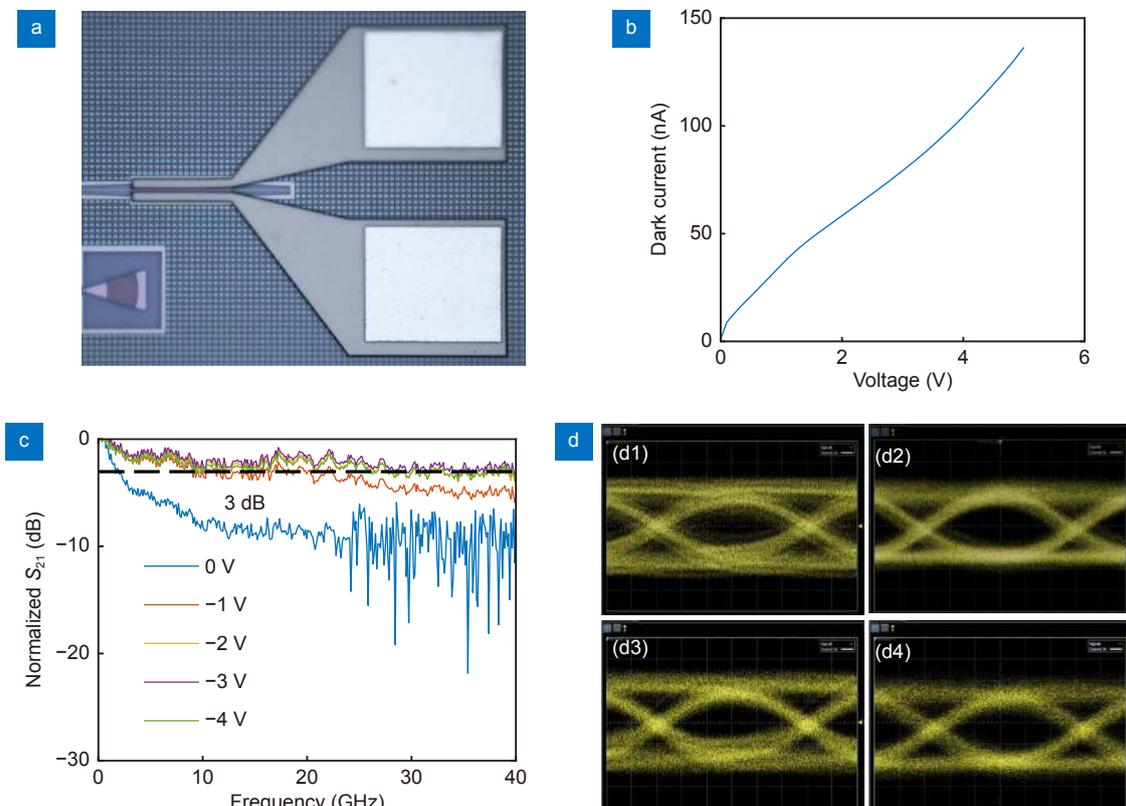


Fig. 8 | Ge/Si waveguide photodetector. (a) Chip picture. (b) Dark current. (c) Bandwidth. (d) Eye diagram at 40 Gbps at each channel.

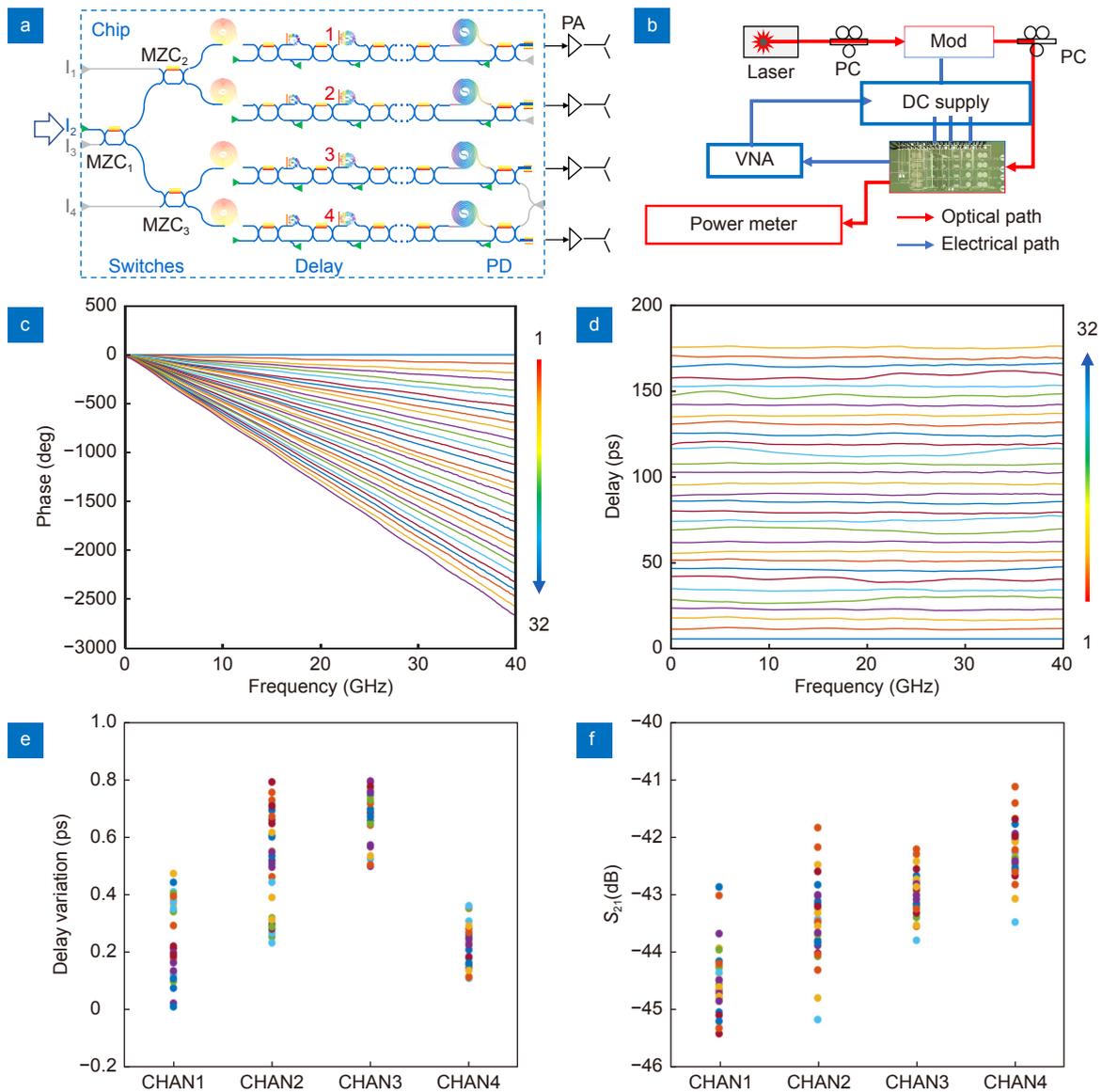


Fig. 9 | (a) Realization of 4-channel OTTDL based photonic beamformer (Input from port I_2 , and output from four PDs). Here light goes along the blue paths, and there is no light in the grey paths. (b) Experimental setup. Measured phase response (c) and group delay response (d) of the microwave signals for all 32 delay states of the first channel of delay line. The delay variations (e) and the measured S_{21} (f) for all four channels at 18 GHz. PC: polarization controller, Mod: modulator, VNA: vector network analyzer.

elements and is usually set as half of the wavelength of the target frequency (i.e., $d=\lambda/2$), θ_m is the maximal steering angle (e.g., here $\theta_m=90^\circ$), N_θ is the number of the formed beam for steering and one has $N_\theta = [2^M/(N-1) + 1]$. Hence, for the 18 GHz microwave signal in our case, the minimum delay time is determined as $\Delta\tau = \Delta t = 5.68$ ps without using the fine-tuning delay. As a result, the formed beam corresponding to the 1st and 32nd states are overlapped almost, indicating that eleven distinguishable beams can be formed for steering.

Figure 9(b) shows the experimental setup for measur-

ing the amplitude/phase responses of the microwave signals. Here light with an optical power of 15 dBm was launched from a tunable CW laser and modulated by using a commercial modulator, which was driven by the RF signal from the VNA. The modulated optical signal is then coupled to port I_1 of the chip. The time delays for the four channels are controlled by setting the optical switches on the chip to the desired states with a multi-channel programmable voltage source. Finally, the four channels of optical signals were converted to RF signals by using the corresponding on-chip PDs and received by the VNA one-by-one in the experiment. As a

representative, the measured phase response for all the 32 states of the first channel is shown in Fig. 9(c), where the phase delay is normalized to the state with the shortest delay. Figure 9(d) shows the group delay derived from the frequency derivative of the measured phase. The delay line provides a delay tuning range from 0 to 176 ps with a step of 5.68 ps in the 0–40 GHz frequency range (limited by the PD bandwidth).

Furthermore, the delay responses of all the four channels were measured at the frequency of 18 GHz, including the delay variations and the microwave transmissions (S_{21}), as shown in Fig. 9(e–f). Here the delay variation ΔT is defined as the measured delay of each state in four channels compared to the designed time delay T_0 . From Fig. 9(e), one sees that all four channels have relatively small time delay errors of <0.8 ps, owing to the insensitivity to the width variation of multimode photonic waveguides used here. Besides, the microwave loss for all the states in different channels varies within 5 dB, as revealed in Fig. 9(f). Here channel #1 has the largest microwave loss because there are most metal conductors placed over the waveguides of channel #1 to connect the pads on the chip side [see the layout design given in Fig. 4(b)]. Fortunately, the microwave loss can be compensated by introducing a microwave power amplifier.

Then the beam patterns formed by the present 18 GHz microwave photonic beamformer can be calculated by the sum of the individual antenna^{46,47}, i.e.,

$$F(\theta) = \sum_{n=0}^N A_n e^{j[(n-1)\frac{2\pi}{\lambda} d \sin\theta - \phi_n]}, \quad (4)$$

where θ is the steering angle, A_n and ϕ_n are the amplitude and phase of the microwave signal emitted from the n -th antenna element.

Figure 10(a) shows the calculated beam patterns corresponding to the eleven steering angles enabled by the digitally-tuning delay line ($f=18$ GHz). It can be seen that

the beam angle can be tuned from -63.76° to 69.11° with a step of 12° . Since the present 4-channel OTTDL is amplitude-controllable, the amplitudes for the four channels of signals are optimized to reduce the pattern sidelobe greatly. For example, when the amplitude ratio for Channels #1–4 is set as 1:0.4:0.4:1, the formed beam patterns are shown in Fig. 10(b). From this figure, it can be seen that the sidelobe has been suppressed effectively compared to that in Fig. 10(a) for the case when the four channels have uniform amplitudes.

In addition, the continuously-tuning delay in the present chip can be utilized so that the delay difference between adjacent channels can be tuned precisely, indicating that the beam-steering angle can be tuned finely. Figure 11(a) shows the beam pattern with different steering angles at the frequency of 18 GHz when $\Delta\tau = 2.84$ ps with the help of fine-tuning delay, in which case the steering angle was tuned from -71.09° to 73.24° with a step of $\sim 7^\circ$. In this case, the device offers 21 distinguishable steering angles. Furthermore, the steering angle for the beam formed by the present on-chip processor can be varied continuously. Figure 11(b) presents the steering angle varying as a function of the delay difference between adjacent emitters. Furthermore, with the assistance of the amplitude-controlled MZCs, the extinction ratio (ER) between the side lobe and the major lobe of the beam pattern can be reduced to ~ 0.1 . The extinction ratio is defined as the ratio between the intensities of the sidelobe maximum (within the steering angle tuning range) and the main lobe peak.

The dependence of the steering angle and the ER on the frequency is then verified. Figure 12(a) shows the calculated beam patterns at the microwave frequency of 12–21 GHz, which covers a majority of the Ku and K band. Here the steering angle around $\theta = -21.07^\circ$ is considered as an example. It can be seen that the beam can be formed very well with low sidelobes and the pattern is

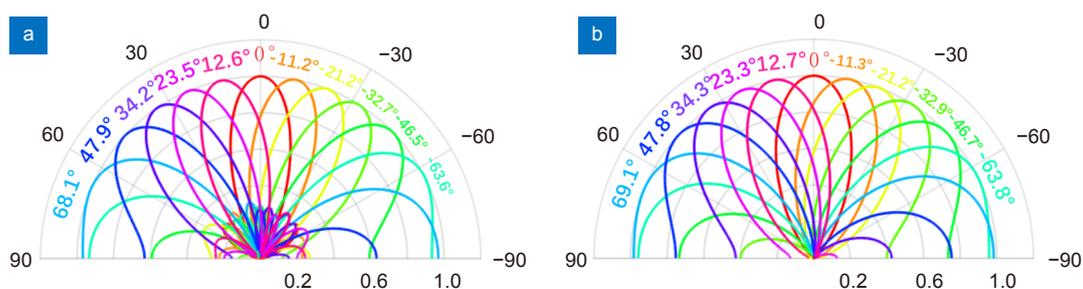


Fig. 10 | Calculated beam patterns corresponding to the 11 steering angles enabled by the digitally-tuning delay line ($f=18$ GHz). (a) Four channels have uniform amplitudes. (b) Four channels have the optimized amplitudes.

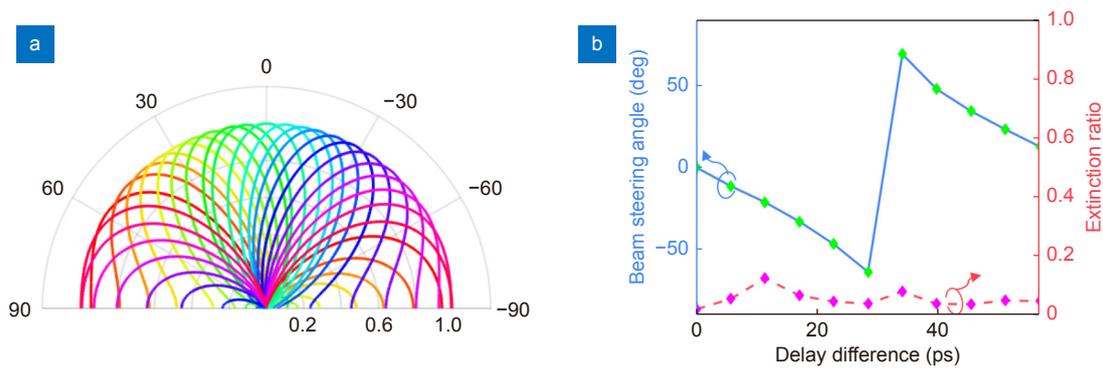


Fig. 11 | (a) Calculated beam patterns corresponding to the 21 steering angles enabled with the fine-tuning delay. (b) Beam steering angle and extinction ratio as the delay difference between adjacent emitters increases from 0 to 56.8 ps.

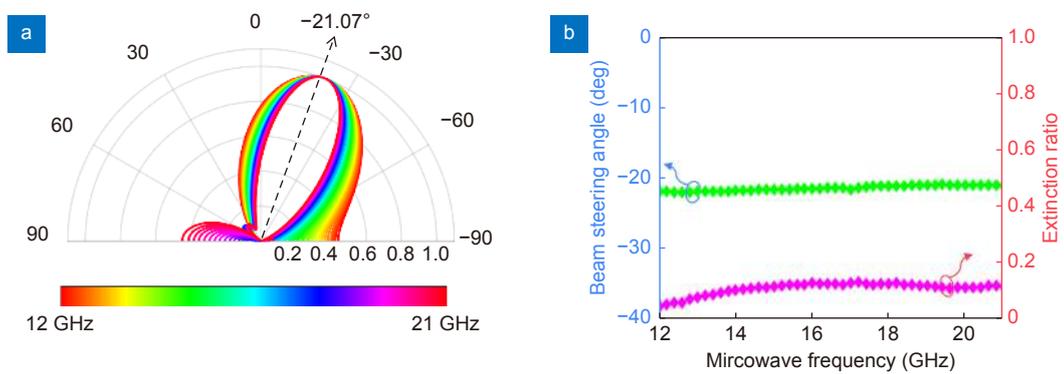


Fig. 12 | (a) Calculated beam patterns when operating at different RF frequencies. (b) Calculated steering angle and extinction ratio as the steering angle varies. Here the frequency is from 12 GHz to 21 GHz.

not sensitive to the frequency. Figure 12(b) shows the steering angle θ and the extinction ratio ER for the beam pattern as the frequency varies. It can be seen that the beam steering angle is frequency insensitive and the extinction ratio is below 0.2.

Table 1 gives a summary of the representative delay lines for beam steering in terms of the scale, the performance of waveguides and MZSs, the overall power consumption and the footprints^{3,14–16,31,44,45}. As shown in Table 1, most of these delay lines were demonstrated with a single channel^{14–16}. There are a few chips with multiple channels, as demonstrated in ref.^{3,31,44,45}, where the delay line is routed in either snake-shape^{3,31} or S-shape⁴⁵, resulting in large footprints. Furthermore, the waveguides have some high propagation loss, which prevents further improvement of the chip scale. In contrast, the present chip has the lowest on-chip loss, owing to the ultralow-loss silicon photonic waveguides developed here, which enables a relatively large range of delay. Moreover, a continuously-tuning delay line is firstly introduced to replace the conventional microrings³ for large-bandwidth delay. Note that some recent works have shown that microrings also have the potential to realize large-delay-

bandwidth continuously-tunable delay lines^{22–24}.

In addition, the waveguide spirals for the present chip are very compact, which is realized by introducing a tapered Euler-curve S-bend whose minimal bending radius is as compact as 10 μm . As a result, the present chip has a compact footprint of $\sim 4.9 \text{ mm}^2$. Furthermore, the power consumption is also a key parameter for evaluating the performance of a microwave photonic beamformer. For the present chip, low-phase-error MZSs, which not only relieve the calibration complexity but also reduce the total power consumption, were introduced. In the experiments, the overall power consumption of the chip is about 540 mW, which can be further reduced by introducing air-trenches⁴².

Tunable optical signal filtering

Optical filters are another essential component in optical communications and microwave photonics. The main parameters for designing optical filters include the free spectral range (FSR), the central wavelength, the pass-band bandwidth and the response shape. For practical applications, a universal processor could be configured for optical signal filtering with continuous tunability in

Table 1 | Comparison of various on-chip microwave photonic beamformers (B.W.: Bandwidth).

Year	Integrated components	Bit×N _{ch}	Total delay (ps)	Delay step (ps)	WG loss (dB/cm)	On-chip loss (dB)	Optical bandwidth (nm)	MZI power consumption (mW/π)	Total power consumption (mW)	MZS speed (μs)	Size (mm ²)
2010 ⁴⁴	Delay lines	5×4	200	36	/	/	0.016	/	862	/	4.6×0.8
2014 ¹⁴	Delay lines	7×1	1270	10	0.9	6.2	20	18	1.09×1270	/	11.84
2017 ¹⁵	Delay lines	7×1	1280	10	0.35	8.5	0.48	12	12.24×8	18.97	28.62
2019 ¹⁶	Delay lines	7×1	191.37	1.42	2.472	15.64	35	38	178.77	33.7	13.32
2019 ³¹	Delay lines	5×4	155	3	2.472	7.2	35	/	200	/	/
2019 ⁴⁵	Delay lines	4×4	50	/	/	/	/	0.2 V/π	/	/	17.58
2020 ³	Delay lines, Modulator and PD	5×8	496	2 (w/o ring)	1.3	3.5-7	30 (w/o ring)	20	1450	56	11.03×3.88
				Small (with ring)			0.108 (with ring)				
Our work	Delay lines and PD	5×4	176	5.68 (w/o fine-tuning delay)	0.28	3-3.4	60	22	540 (w/o fine-tuning delay)	20	4.9
				Small (with fine-tuning delay)					2140 (with fine-tuning delay)		

terms of the parameters mentioned above.

As shown in the blue lines of Fig. 13(a), the present silicon photonic processor can be configured as a tapped-delay-line filter by activating channels #3 and #4. Meanwhile, each of these two channels can work with several taps by engineering the coupling ratio of the MZSs. For the signal launched from port I₄, the configured structure can be modelled as a tapped-delay line filter with the following transfer function⁸

$$H(f) = \sqrt{\frac{\Gamma}{K}} \left[\sum_{k=0}^{K-1} a_k e^{-j\varphi_k} e^{-j2\pi f k \tau} \right], \quad (5)$$

where f is the optical frequency, Γ is an amplitude normalization constant, K is the number of taps introduced, $k\tau$ is the delay of the k -th tap, a_k and φ_k are the amplitude- and phase-coefficients for the k -th tap. The FSR of the optical filter is inversely proportional to the delay difference τ between adjacent taps. For the present processor design, these coefficients a_k and φ_k can be varied by controlling the tunable MZSs and enables the response shaping as well as the frequency tuning. Figure 13(b–e) shows the measured filtering responses with different delay-differences τ . In the experiment, a tunable laser (Agilent 81600B) was used as the source, and a power meter (Agilent 81618A) was used to monitor the transmissions at the output port. The measured transmissions were normalized with respect to the transmission of an adjacent straight singlemode waveguide connected with grating couplers on the same chip. A stopband suppression of >20 dB was achieved across the entire bandwidth of interest (e.g., ~30 nm). Figures 13(b–d)

show the filtering responses of a 2-tapped-delay-line filter realized by making MZC₃ work as a 3-dB coupler and setting the delay-difference between channels #3 and #4 (2 taps) to be $\tau=22.72, 45.44,$ and 90.88 ps, respectively. Moreover, as mentioned above, more taps can be implemented by tuning the splitting ratios of the MZSs in the channels. Here, Fig. 13(e) gives a comparison of the 2-tap (orange) and 4-tap (blue) filter shaping. The 4-tapped passband filter is realized by tuning V_{34} and V_{44} to achieve splitting ratios of 50 : 50 while the other MZSs are in the ON or OFF states. As a result, both channels #3 and #4 have 2 taps, resulting in 4 taps in total and $\tau=2^3\Delta t$. These results verify the tunability for the FSRs and the passband repetition bandwidth between the stopband notches of the corresponding filter coefficient configurations, which is the key for implementing optical clock rate multiplication.

We also evaluate the thermal crosstalk of the device by measuring the stopband notch depth variation of the spectral response when tuning the neighboring heaters, as shown in Fig. 13(f). In this example, the processor is configured as a 2-tapped-delay-line filter with $\tau = 5.68$ ps. The crosstalk from the nearest heaters (i.e., V_{21} and V_{22}) is negligible and the notch-depth variations are less than 1.8 dB. Moreover, as shown in Fig. 13(g), the notch depth is insensitive to the thermal crosstalk from the neighboring channel (e.g., channel #2) when all the MZSs in channel #2 are turned on with the heating power of 40 mW. The filter configuration to achieve different spectral responses are summarized in the inset table. With the help of the low-phase-error MZS technique, the

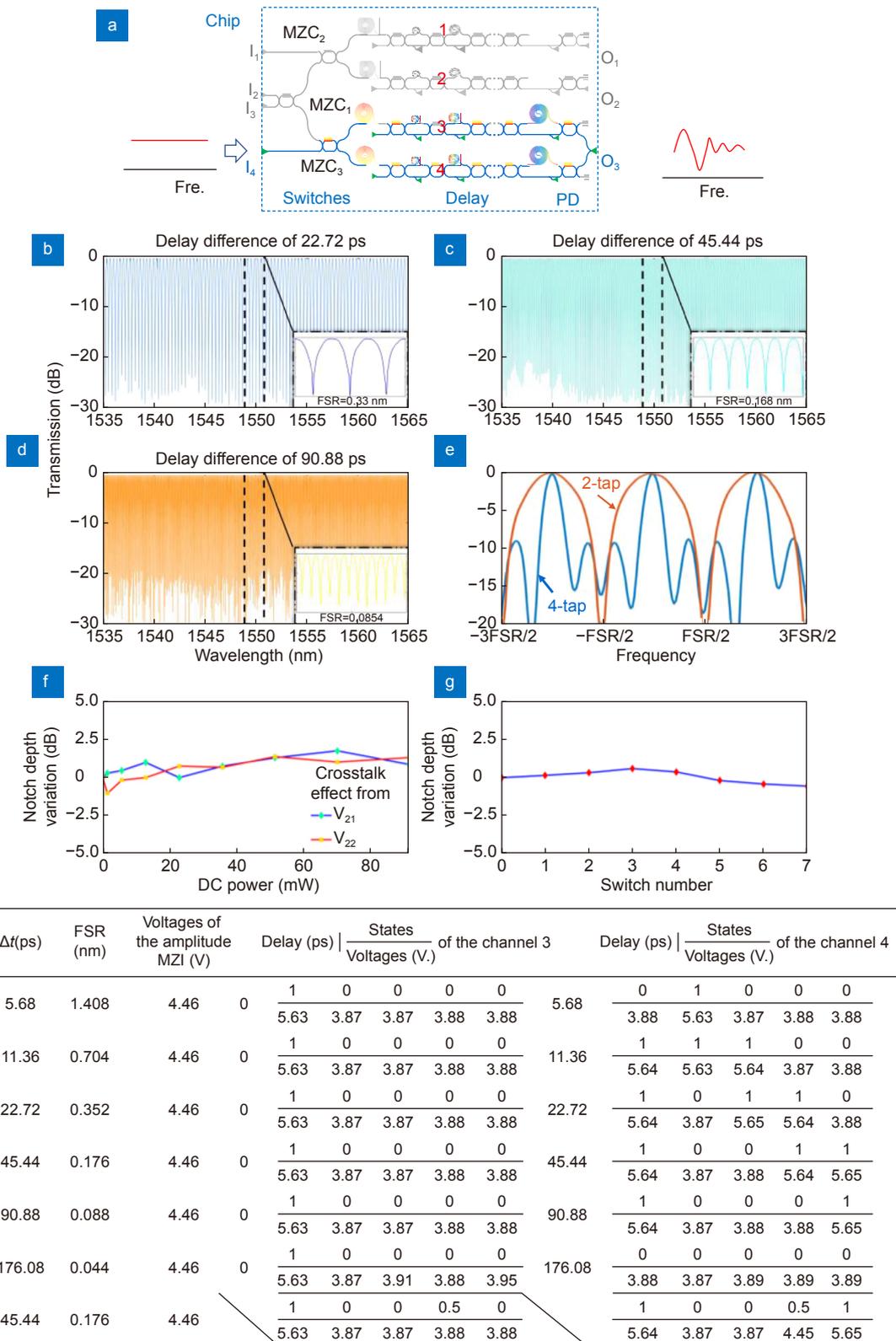


Fig. 13 | (a) Principle of arbitrary filtering operation (Input from port I_4 , and output from port O_3). Measurements of filter spectral responses: (b–d) demonstrations of the FSR tunability for the filter. (e) Demonstrations of passband shaping for the filter. (f) Notch-depth variation due to thermal crosstalk from neighboring heaters (e.g., V_{21} and V_{22} in channel #2). (g) Notch-depth variation due to thermal crosstalk from the neighboring channel (e.g., channel #2) when all the MZSs in channel #2 are turned on with the power of 40 mW. Inset table: filter configuration for achieving the desired FSRs by setting the power splitting ratios of the MZSs in channels #3 and #4.

voltages on all MZSs for achieving the same splitting ratio are almost the same. As a result, the optical filter can be easily configured to achieve the central wavelength, the FSR, the passband bandwidth and the response shape as desired.

In practical, the repetition rates of the pulse sources are fixed by using an optical cavity which usually has a fixed cavity length. When using the present processor, the repetition rate of optical pulse train sources can be switched flexibly, and this is particularly useful in radar systems for detecting the distances of the targets.

Arbitrary waveform generation

Defining signal waveforms at high speeds is essential for modern telecommunications/radar systems with high signal bandwidths⁴⁵. Conventional implementations of high-speed arbitrary waveform generators (AWGs) require fast and power-hungry digital-to-analog converters. A state-of-the-art commercial AWC with a sampling rate about 100 GSa/s and an electrical bandwidth about 40 GHz is still too expensive for applications out of the laboratory. Alternatively, photonic approaches open a promising path for high-speed AWCs potentially with low cost and low power consumption⁸.

Here the present silicon photonic processor can be configured as a tapped-delay line, indicated by the blue lines in Fig. 14(a). Here the signal launched from port I_1 is switched to channel #1 by MZC₂. Then the signal is split to several sub-pulses with different time delays by appropriately controlling the splitting ratios of the MZSs. Figure 14(b–e) shows the synthesis of several types of representative waveform generation from an input pulse with a pulse width of 15 ps, including the rectangular, Gaussian, falling-triangular and rising-triangular types. The processor is configured to a 4-tapped-delay line with a time-domain impulse response resolution of 45.44 ps. In this case, MZSs V_{11} , V_{12} and V_{13} are tuned so that the pulse goes through the path without spirals, while MZSs V_{14} , V_{15} and V_{16} are tuned to receive four taps with appropriate amplitudes and delays. Theoretically, the splitting ratios of MZSs V_{14} , V_{15} and V_{16} in channel #1 should be designed as [1:1, 1:1, 1:1], [1:1, 1:3, 1:1], [2:1, 1:1, 2:1], and [1:2, 1:1, 1:2] for generating a square waveform, a Gaussian waveform, a rising ramp, and a falling ramp, respectively. In experiments, the splitting ratios of these MZSs are modified optimally to compensate the excess losses of the spiral waveguide as well as the MZSs themselves. The table in the inset shows the intensities

(A_1 , A_2 , A_3 , and A_4) of the sub-pulses, and the corresponding voltages V_{14} , V_{15} and V_{16} applied to the MZSs in channel #1.

These results provide a successful demonstration of the AWC with the waveforms directly synthesized in the time domain. Note that the generated waveforms are slight deviations from the ideal one, which is mainly caused by the limited extinction ratio (ER) of the MZSs, the limited bandwidths of PDs and oscilloscopes, the limited noise floor of an optical amplifier, the limited ER of the MZSs. In order to solve this problem, one should improve the MZSs with ultra-low losses and ultra-high ERs, reduce the excess losses of the waveguide spirals, improve the electrical bandwidth, and use ultra-short input pulse⁴⁸. Besides, according to the tuning range and the delay resolution of the digitally-tuning delay line, the present processor can be programmed to be a 32-tap delay-line filter with a time-domain impulse response resolution of 5.68 ps, corresponding to an AWC sample rate of 176 GSa/s.

Conclusions

As a summary, a chip-scale programmable silicon photonic processor has been demonstrated successfully by comprising a 1×4 variable power splitter based on cascaded MZCs, four Ge/Si photodetectors, four channels of thermally-tunable optical delaylines. The present programmable silicon photonic processor has been configured for realizing versatile functionalities, including tunable time-delay, microwave photonic beamforming, arbitrary optical signal filtering, and arbitrary waveform generation. On one hand, 2- μm -wide waveguide spirals have been introduced to enable an ultralow propagation loss of 0.28 dB/cm, which is much lower than the waveguide loss of 2–3 dB/cm for conventional 450×220 nm² silicon photonic waveguides used popularly. Even though the total length of the waveguide spirals is about 1.4 cm only for the present case, there is a notable loss reduction of 2.4–3.8 dB for the total chip loss. The total loss from the waveguide spirals might be even more dominant if longer waveguide spirals are introduced for longer time delay. For example, in order to achieve nanosecond-scale time delay, the total length of the waveguide spirals is as long as ~10 cm, in which case the loss is as high as 20–30 dB when using traditional silicon photonic waveguides with a loss of 2–3 dB/cm. Therefore, it is crucial to introduce low-loss waveguides when it is desired to continue up the scale of the PIC. On the

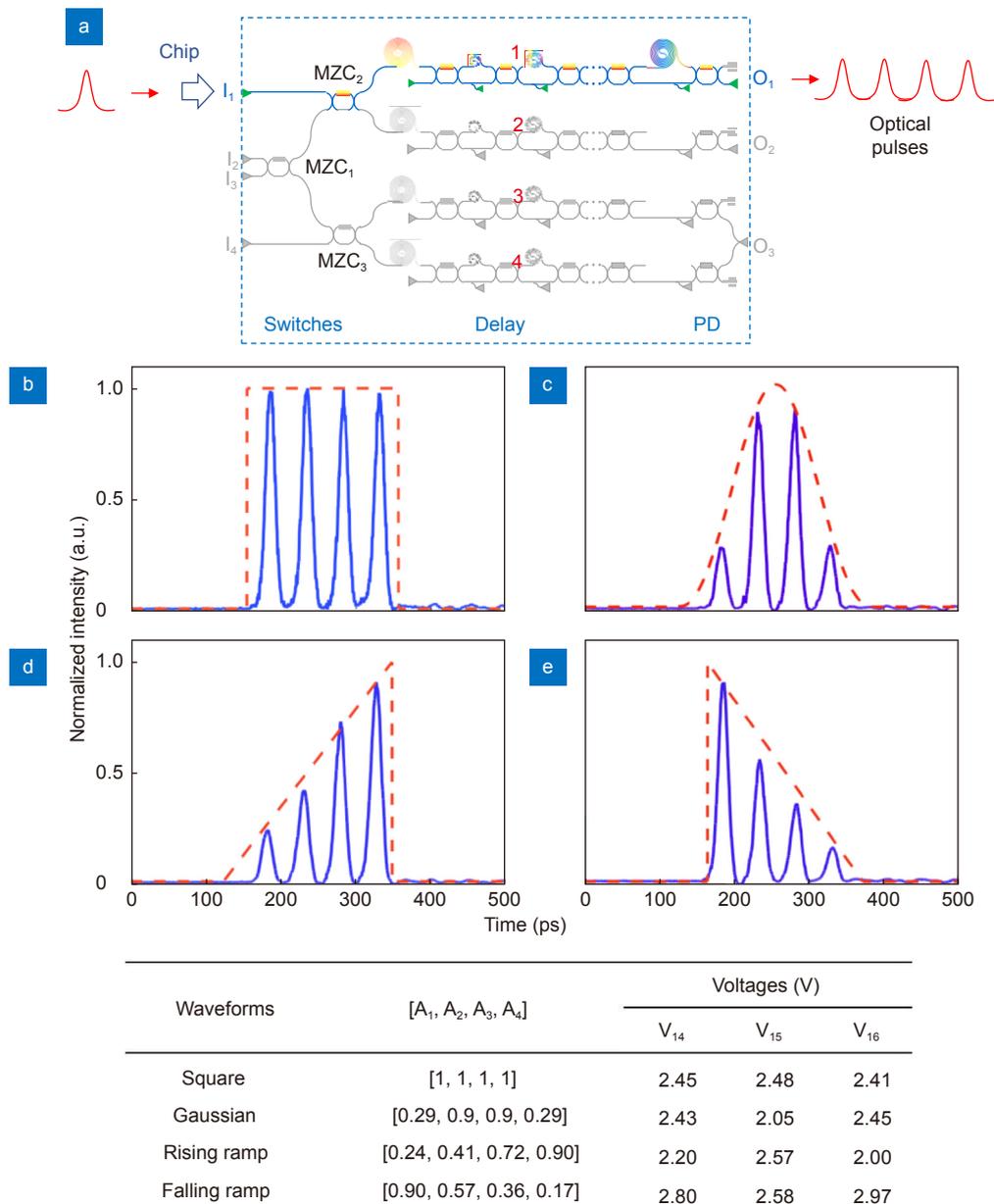


Fig. 14 | (a) Arbitrary waveform generation configuration. Here light inputs from port I_1 , goes through channel #1, and finally outputs from port O_1 . The measured waveforms (see the blue solid line), which are normalized to the peak intensity. (b) Square waveform. (c) Gaussian waveform. (d) Rising ramp. (e) Falling ramp. The red dashed lines outline the envelopes of the ideal waveforms. Inset table shows the intensities (A_1 , A_2 , A_3 , and A_4) for the four taps.

other hand, all the MZCs and MZSs are designed with 2- μm -wide arm waveguides to be nearly calibration-free. This design can be easily configured to achieve the designed functions as desired with low power consumption. This work paves the way for the realization of large-scale reconfigurable silicon photonic chips, owing to the high-performance basic building blocks techniques. It also provides the evidence to feasibly realize large-scale silicon photonic chips for more applications, e.g., quantum photonics, optical computing, lidar, etc. In the

future it is also possible to further reduce the other key elements' loss, and utilize the mechanisms of the electro-optic effect to further lower the power consumption and improve the tuning speed.

References

1. Chang WSC. *RF Photonic Technology in Optical Fiber Links* (Cambridge University Press, Cambridge, 2002).
2. Gauthier D. Slow light brings faster communications. *Phys World* **18**, 30–32 (2005).
3. Zhu C, Lu LJ, Shan WS, Xu WH, Zhou GQ et al. Silicon integrated microwave photonic beamformer. *Optica* **7**, 1162–1170

- (2020).
4. Khonina SN, Kazanskiy NL, Butt MA, Karpeev SV. Optical multiplexing techniques and their marriage for on-chip and optical fiber communication: a review. *Opto-Electron Adv* 5, 210127 (2022).
 5. Lvovsky AI, Sanders BC, Tittel W. Optical quantum memory. *Nat Photonics* 3, 706–714 (2009).
 6. Vandoorne K, Mechet P, Van Vaerenbergh T, Fiers M, Morthier G et al. Experimental demonstration of reservoir computing on a silicon photonics chip. *Nat Commun* 5, 3541 (2014).
 7. Yang L, Nie JS, Duan LZ. Dynamic optical sampling by cavity tuning and its application in lidar. *Opt Express* 21, 3850–3860 (2013).
 8. Xie YW, Zhuang LM, Lowery AJ. Picosecond optical pulse processing using a terahertz-bandwidth reconfigurable photonic integrated circuit. *Nanophotonics* 7, 837–852 (2018).
 9. Thomson D, Zilkie A, Bowers JE, Komljenovic T, Reed GT et al. Roadmap on silicon photonics. *J Opt* 18, 073003 (2016).
 10. Bogaerts W, Chrostowski L. Silicon photonics circuit design: methods, tools and challenges. *Laser Photonics Rev* 12, 1700237 (2018).
 11. Dai DX. Advanced passive silicon photonic devices with asymmetric waveguide structures. *Proc IEEE* 106, 2117–2143 (2018).
 12. Soref R. The past, present, and future of silicon photonics. *IEEE J Sel Top Quantum Electron* 12, 1678–1687 (2006).
 13. Moreira RL, Garcia J, Li WZ, Bauters J, Barton JS et al. Integrated ultra-low-loss 4-bit tunable delay for broadband phased array antenna applications. *IEEE Photonics Technol Lett* 25, 1165–1168 (2013).
 14. Xie JY, Zhou LJ, Li ZX, Wang JT, Chen JP. Seven-bit reconfigurable optical true time delay line based on silicon integration. *Opt Express* 22, 22707–22715 (2014).
 15. Wang XY, Zhou LJ, Li RF, Xie JY, Lu LJ et al. Continuously tunable ultra-thin silicon waveguide optical delay line. *Optica* 4, 507–515 (2017).
 16. Zheng PF, Wang CQ, Xu XM, Li J, Lin DD et al. A seven bit silicon optical true time delay line for Ka-band phased array antenna. *IEEE Photonics J* 11, 5501809 (2019).
 17. Wang Y, Sun H, Khalil M, Dong W, Gasulla I et al. On-chip optical true time delay lines based on subwavelength grating waveguides. *Opt Lett* 46, 1405–1408 (2021).
 18. Sun H, Wang Y, Chen LR. Integrated discretely tunable optical delay line based on step-chirped subwavelength grating waveguide bragg gratings. *J Lightwave Technol* 38, 5551–5560 (2020).
 19. Cvetojevic N, Jovanovic N, Lawrence J, Withford M, Bland-Hawthorn J. Developing arrayed waveguide grating spectrographs for multi-object astronomical spectroscopy. *Opt Express* 20, 2062–2072 (2012).
 20. Yariv A, Xu Y, Lee RK, Scherer A. Coupled-resonator optical waveguide: a proposal and analysis. *Opt Lett* 24, 711–713 (1999).
 21. Scheuer J, Poon JKS, Paloczi GT, Yariv A. Coupled resonator optical waveguides (CROW). *Proc SPIE* 5735, 52–59 (2005).
 22. Cardenas J, Foster MA, Sherwood-Droz N, Poitras CB, Lira HLR et al. Wide-bandwidth continuously tunable optical delay line using silicon microring resonators. *Opt Express* 18, 26525–26534 (2010).
 23. Shan WS, Lu LJ, Wang XY, Zhou GQ, Liu YB et al. Broadband continuously tunable microwave photonic delay line based on cascaded silicon microrings. *Opt Express* 29, 3375–3385 (2021).
 24. Xie JY, Zhou LJ, Zou Z, Wang JT, Li XW et al. Continuously tunable reflective-type optical delay lines using microring resonators. *Opt Express* 22, 817–823 (2014).
 25. Wu BB, Yu Y, Xiong JB, Zhang XL. Silicon integrated interferometric optical gyroscope. *Sci Rep* 8, 8766 (2018).
 26. Gundavarapu S, Belt M, Huffman TA, Tran MA, Komljenovic T et al. Interferometric optical gyroscope based on an integrated Si₃N₄ low-loss waveguide coil. *J Lightwave Technol* 36, 1185–1191 (2018).
 27. Lowell JR, Parra E. Application of slow light: a DARPA perspective. *Proc SPIE* 5735, 80–86 (2005).
 28. Mok JT, Eggleton BJ. Photonics: expect more delays. *Nature* 433, 811–812 (2005).
 29. Zhang L, Jie LL, Zhang M, Wang Y, Xie YW et al. Ultrahigh-Q silicon racetrack resonators. *Photonics Res* 8, 684–689 (2020).
 30. Griffith A, Cardenas J, Poitras CB, Lipson M. High quality factor and high confinement silicon resonators using etchless process. *Opt Express* 20, 21341–21345 (2012).
 31. Zheng PF, Xu XM, Lin DD, Liu PC, Hu GH et al. A wideband 1×4 optical beam-forming chip based on switchable optical delay lines for Ka-band phased array. *Opt Commun* 488, 126842 (2021).
 32. Dong P, Qian W, Liao SR, Liang H, Kung CC et al. Low loss shallow-ridge silicon waveguides. *Opt Express* 18, 14474–14479 (2010).
 33. Pérez-López D, López A, DasMahapatra P, Capmany J. Multipurpose self-configuration of programmable photonic circuits. *Nat Commun* 11, 6359 (2020).
 34. Zhou HL, Zhao YH, Wang X, Gao DS, Dong JJ et al. Self-configuring and reconfigurable silicon photonic signal processor. *ACS Photonics* 7, 792–799 (2020).
 35. Barwicz T, Haus HA. Three-dimensional analysis of scattering losses due to sidewall roughness in microphotonic waveguides. *J Lightwave Technol* 23, 2719–2732 (2005).
 36. Song LJ, Li H, Dai DX. Mach-Zehnder silicon-photonic switch with low random phase errors. *Opt Lett* 46, 78–81 (2021).
 37. Ciminelli C, Passaro VMN, Dell'Olio F, Armenise MN. Three-dimensional modelling of scattering loss in InGaAsP/InP and silica-on-silicon bent waveguides. *J Eur Opt Soc Rapid Publ* 4, 09015 (2009).
 38. Bauters JF, Heck MJR, John D, Dai DX, Tien MC et al. Ultra-low-loss high-aspect-ratio Si₃N₄ waveguides. *Opt Express* 19, 3163–3174 (2011).
 39. Hong SH, Zhang L, Wang Y, Zhang M, Xie YW et al. Ultralow-loss compact silicon photonic waveguide spirals and delay lines. *Photonics Res* 10, 1–7 (2022).
 40. Jiang XH, Wu H, Dai DX. Low-loss and low-crosstalk multimode waveguide bend on silicon. *Opt Express* 26, 17680–17689 (2018).
 41. Souza MCMM, Grieco A, Frateschi NC, Fainman Y. Fourier transform spectrometer on silicon with thermo-optic non-linearity and dispersion correction. *Nat Commun* 9, 665 (2018).
 42. Dong P, Qian W, Liang H, Shafiqi R, Feng DZ et al. Thermally tunable silicon racetrack resonators with ultralow tuning power. *Opt Express* 18, 20298–20304 (2010).
 43. Masood A, Pantouvaki M, Lepage G, Verheyen P, Van Campenhout J et al. Comparison of heater architectures for

thermal control of silicon photonic circuits. In *10th International Conference on Group IV Photonics* 83–84 (IEEE, 2013); <http://doi.org/10.1109/Group4.2013.6644437>.

44. Choo G, Madsen CK, Palermo S, Entesari K. Automatic monitor-based tuning of an RF silicon photonic 1X4 asymmetric binary tree true-time-delay beamforming network. *J Lightwave Technol* **36**, 5263–5275 (2018).
45. Duarte VC, Prata JG, Ribeiro CF, Nogueira RN, Winzer G et al. Modular coherent photonic-aided payload receiver for communications satellites. *Nat Commun* **10**, 1984 (2019).
46. Volakis JL. *Antenna Engineering Handbook* 4th ed (McGraw-Hill Education, New York, 2007).
47. Balanis CA. *Modern Antenna Handbook* (John Wiley & Sons, Inc., Hoboken, 2008).
48. Krylov AA, Sazonkin SG, Lazarev VA, Dvoretzkiy DA, Leonov SO et al. Ultra-short pulse generation in the hybridly mode-locked erbium-doped all-fiber ring laser with a distributed polarizer. *Laser Phys Lett* **12**, 065001 (2015).

Acknowledgements

We are grateful for financial supports from National Major Research and Development Program (No. 2018YFB2200200); National Science Fund for Distinguished Young Scholars (61725503); Zhejiang Provincial Natural Science Foundation (LZ18F050001, LGF21F050003); National Natural Science Foundation of China (NSFC) (91950205, 6191101294, 11861121002, 61905209, 62175214, 62111530147).

Author contributions

Y. W. Xie and D. X. Dai proposed the original idea of the work. Y. W. Xie and S. H. Hong carried out the experiments and wrote the paper. H. Yan analyzed the experimental data. C. P. Zhang designed the layout of the chip. L. M. Zhuang participated the discussion of the research. D. X. Dai supervised the research and wrote the paper. All authors discussed the results and commented on the manuscript.

Competing interests

The authors declare no competing financial interests.