NPN SiGe Hetero Junction Transistor latch-up memory selector

Gaspard Hiblot, Taras Ravsher, Roger Loo, Bhuvaneshwari Yengula Venkata Ramana, Yann Canvel, Nathali Franchina Vergel, Andrea Fantini, Shamin Houshmand Sharifi, Nina Bazzazian, Mustafa Ayyad, Alex Merkulov, Gouri Sankar Kar, Sebastien Couet

***Abstract*— NPN latch-up memory selector devices featuring SiGe hetero-junctions are fabricated and measured electrically. 25% Ge is introduced into the floating base layer by epitaxy. The performance of this device is compared against an implanted Si stack. It is observed that the addition of 25% Ge in the floating base layer of these latch-up selector devices boosts the non-linearity by more than x100 and enables abrupt latch-up below 2V. TCAD simulations comparing drift-diffusion and hydro-dynamic models are used to validate our understanding of the device.**

***Index Terms*— Selector, SiGe, NPN, HBT**

I. Introduction

In order to enable cross-point array and maximize Magnetic RAM (MRAM) density, two-terminal selectors are required [1], [2]. By suppressing 'sneak path' currents thanks to the non-linearity of the selector, a memory cell can be selected through partial biasing of the neighbouring cells, hence achieving minimum bitcell area ($4F^2$) [3]. Recent industrial announcements demonstrating the feasibility of scaling down the Magnetic Tunnel Junction (MTJ) pitch down to 50 nm [4] have further underlined the need for a two-terminal selector that can surpass the density limitations of the 1 Transistor 1 MTJ (1T1MTJ) architecture.

It was noted in [5] that an open-base Bipolar Junction Transistor (BJT) could exhibit bistable behavior. This structure can be very simply built by alternating N-type and P-type dopings so as to form an NPN pattern, where the two N-doped regions are contacted by electrodes while the middle P-type region is floating. The P-type region of this device is not completely depleted, in contrast to punchthrough diodes [6], [7]. This results in an undesirable hysteresis, but simultaneously provides an abrupt switching behaviour leading to high Non-Linearity (NL, defined as the ratio between ON-current and OFF-current) [8]. Several experimental realizations have demonstrated this bistable operation in lateral [9], [10] and vertical [11] nanowires. Recently, it has been suggested that this device could also be used as a memory selector [8], owing to its very abrupt transition.

However, the high turn-on voltage of this device (typically >4V) remains an obstacle for its application to STT-MRAM devices, which generally switch below 1.2V [12], [13]. A lower turn-on voltage is thus required to avoid damaging the Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM) devices, reduce the energy consumption and ensure compatibility with CMOS periphery. Although it has been demonstrated that impact ionization can occur below 0.5V [14], [15], triggering latch-up requires the combined effect of avalanche and bipolar gain which has not been observed at such low voltages. It was hinted in [8] that adding Ge content in the base would help to reduce the turn-on voltage of the NPN selector, however it seems that selector devices built with this approach have not been reported yet. This is the topic of this study. First, the fabrication process is detailed. Second, the electrical results are reported. Third, the device simulations results are presented.

Gaspard Hiblot is with IMEC, B3001 Leuven, Belgium (e-mail: gaspard.hiblot@imec.be).

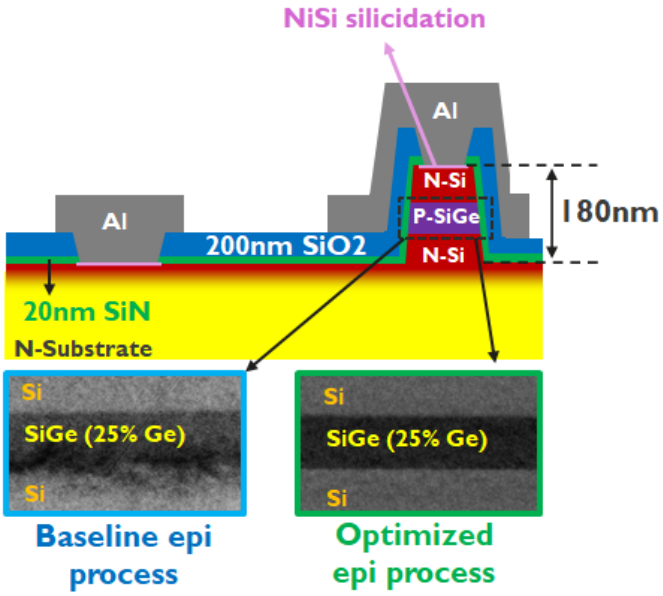


Fig. 1: Device structure and TEM views of the epitaxy stacks.

II. Device fabrication

The device structure is represented in Fig. 1. The stack is epitaxially grown by chemical vapor deposition, patterned (180nm stack height) and encapsulated with 20nm SiN and 200nm SiO2. The contacts are later processed with NiPt silicidation and Aluminum pads.

During epitaxial SiGe growth, a problem of Phosphorus segregation at the surface was encountered and caused a spreading of the Phosphorus profile into the Boron-doped

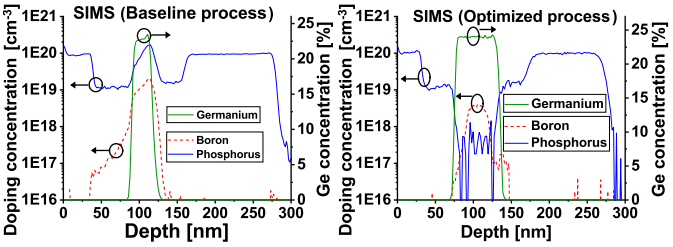


Fig. 2: SIMS profile obtained on blanket wafers with baseline epitaxy process (a) and optimized 2-steps epitaxy process (b).

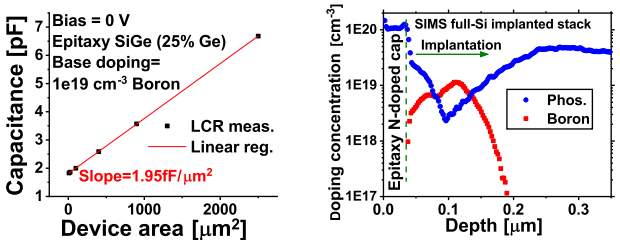


Fig. 3: (a) Depletion thickness for epi-SiGe stack extracted through capacitance measurements. (b) SIMS of implanted Si wafers.

base region, as shown in Fig. 2a. To circumvent this issue, a two-steps epitaxy approach was employed. Between the two epitaxy steps, the Phosphorus segregated at the surface is removed with a clean, so that the SiGe base Boron-doped layer can be grown without excessive Phosphorus contamination. With this approach, the doping profile has been improved as shown in Fig. 2b, where the Phosphorus-concentration in the base is considerably reduced. The SiGe layer has also been extended by ∼15 nm on each side to completely wrap around the Boron doping. The peaks in the SIMS measurements of the Phosphorus profile in the base are due to noise and the actual concentration is estimated to be below 2e17 cm^{-3}. As can be seen in the TEM of Fig. 1, the new epitaxy process also improved the SiGe layer quality. The total depletion thickness of the stack is evaluated through capacitance measurements, which are carried out on test structures with surface area ranging from 9 to 2500 μm^2. The results are reported in Fig. 3a. The intrinsic capacitance of the stack ($1.95\mathrm{fF}/\mu\mathrm{m}^2$) is extracted by linear regression to eliminate the contribution of parasitic capacitances. The resulting depletion thickness is evaluated as 57.2nm (28.6nm per side assuming symmetry). For the sake of comparison, full Silicon devices defined by implantation and capped with N-doped epitaxy layer (SIMS profile in Fig. 3b) are also processed.

III. Electrical Characterization

The electrical characteristics of these devices with the optimized stack are represented in Fig. 4. Due to their undepleted floating base, a hysteresis is observed in the characteristics of

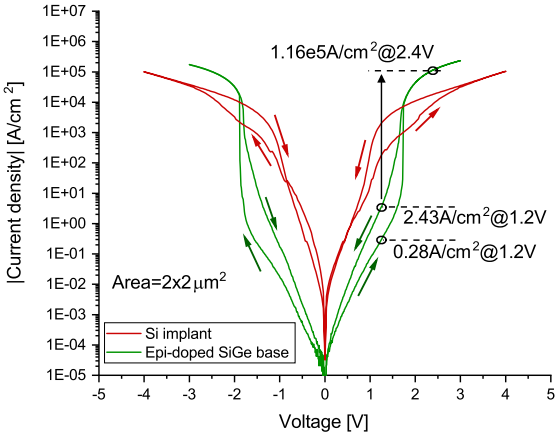
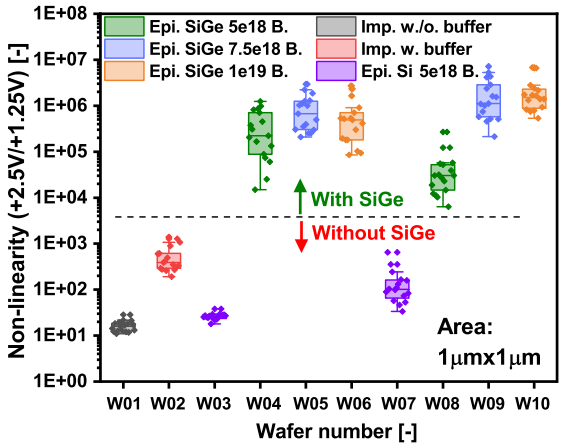


Fig. 4: Electrical measurements on implanted Silicon wafers and epitaxially grown stack with SiGe in the base.

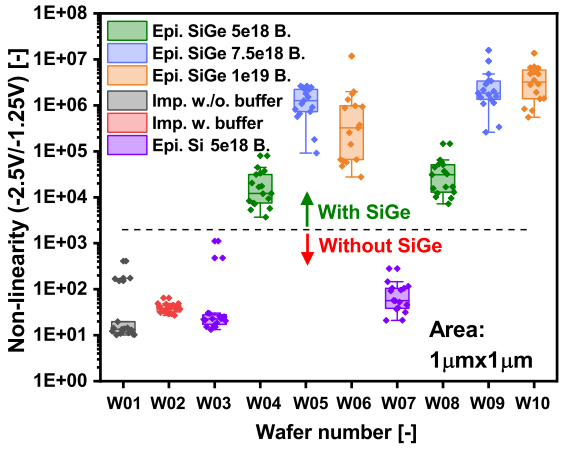
these devices both in negative and positive directions, which distinguishes these devices from punch-through diodes [6], [7]. This floating base stores excess carriers during latch-up which can contribute to a long time constant [16] hence further work is required to evaluate the speed of this device. In contrast to the implanted Si devices (labelled "Si implant" in Fig. 4), epi-doped SiGe devices exhibit abrupt latch-up behaviour with a subthreshold slope below 60mV/dec. This is attributed to the lower bandgap of SiGe compared to Si, which is further reduced thanks to compressive lattice strain [17]. Reducing the bandgap in the base increases the device gain (β) [18] and also increases the impact ionization multiplication factor (M) [19] which govern the latch-up turn-on voltage according to the instability criterion $\beta(M-1) \geq 1$ [5].

At operating voltages of 2.4V/1.2V, the selector achieves a NL coefficient of $4.1 \cdot 10^5$ in the forward branch. In the backward branch, the NL reduces to $4.7{\cdot}10^4$ due to the hysteresis. On the other hand, the ON-current (I_{on}=$1.16 \cdot 10^5 \mathrm{A/cm}^2$) is insufficient to switch a typical STT-MRAM, whose write currents are generally above $1\mathrm{MA/cm}^2$ [20]. It should be noted that I_{on} is probably artificially reduced by parasitic resistances such as horizontal current flow in the substrate. The large dimensions of the device translate into high absolute current values >4mA which makes it very sensitive to parasitic resistances. Further reduction of the stack thickness should enable higher ON-current. By reducing the stack height below ∼50nm, the electron velocity should reach saturation (∼1e7cm/s). Considering that the electron concentration in the base after latch-up is typically higher than $10^{19} cm^{-3}$, this should theoretically lead to current values above $16\mathrm{MA/cm}^2$.

The non-linearity at 2.5V/1.25V in the forward branch is reported in Fig. 5a for the positive voltage sweep and in Fig. 5b for the negative voltage sweep. Six process conditions are compared: implantation without doped epitaxy buffer below the stack ("imp. w./o. buffer"), implantation with doped epitaxy buffer ("imp. w. buffer"), full-Si epitaxy process ("Epi. Si") with $5e18\,cm^{-3}$ Boron concentration in the base, and



(a)



(b)

Fig. 5: Non-linearity of the forward branch for each wafer in the positive sweep (a) and the negative sweep (b).

finally full epitaxy process with SiGe in the base ("Epi. SiGe") using three different base Boron concentrations ($5e18$, $7.5e18$ and $1e19$ cm^{-3}). It can be observed that only wafers with SiGe in the base have NL exceeding 10^3. The presence of the SiGe layer in the base improves the non-linearity by several decades, at least by a factor $\sim 10^2$ depending on the other parameters (base doping concentration).

IV. TCAD SIMULATIONS

A 1D TCAD model has been constructed, excluding sidewall effects which have been found to be negligible since no perimeter-dependence was observed in the measurements. This is expected because of the width of the devices considered in this study ($\sim \mu m$ range). The stack profile is directly imported from the SIMS measurements displayed in Fig. 2b, removing the noise present in the Phosphorus concentration of the base. The unstable nature of the device and its floating base complicate the simulations. In particular, quasi-static simulations

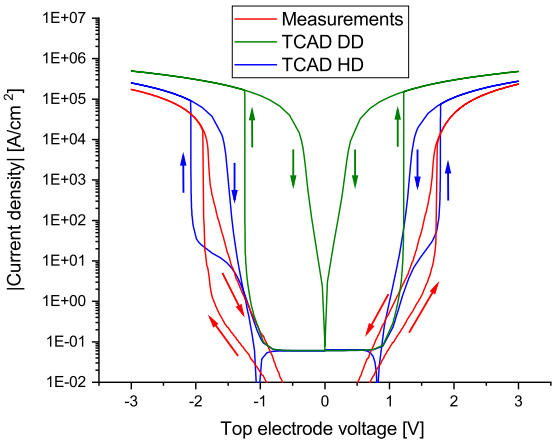


Fig. 6: Comparison between measurements and TCAD simulations with the drift-diffusion model and the hydro-dynamic model.

fail to converge as the bias of the P-type region is not defined. Transient simulations are therefore required. The simulations results obtained by applying a triangular voltage ramp of 10 μs are shown in Fig. 6. The displacement current caused by the transient voltage ramp runs through the device capacitance in addition to the conduction current. This displacement current dominates the simulated current of the device between -1V and 1V, where it leads to a flat plateau of $6.1 \cdot 10^{-2} A/cm^{-2}$.

The impact ionization is included with the Okuto-Crowell model [21]. The carriers need to travel a minimum distance to accumulate enough energy to generate electron-hole pairs ("dead space" effect [22]), which has a strong impact on the impact ionization profile. This explains the discrepancy between measurements and simulations with the Drift-Diffusion (DD) model in Fig. 6. One possibility to take the dead space effect into account is to use the hydrodynamic model (HD) [23]. In that case, the carrier temperature is used as the driver for electron-hole pair generation. As can be seen in Fig. 6, the HD model is in much better agreement with the experimental results than the DD model.

V. CONCLUSION

Floating-base HBT latch-up memory selector devices have been investigated. A two-step epitaxy process was used to avoid Phosphorus contamination in the SiGe base of the device. Latch-up behavior was observed below 2V. Compared to the Si BJT devices, open-base SiGe HBT with 25% Ge in the base exhibit $\sim 10^2$ higher non-linearity. This is explained by the lower bandgap obtained in the HBT base through Ge incorporation, which increases the transistor gain and reduces the threshold for impact ionization. TCAD simulations have been used to validate our understanding of the device operation. A good agreement has been obtained with experimental data by including the dead space effect through the Hydro-Dynamic model.

REFERENCES

[1] H.-L. Chiang, T.-C. Chen, M.-Y. Song, Y.-S. Chen, J.-P. Chiu, K. Chiang, M. Manfrini, J. Cai, W. J. Gallagher, T. Wang, C. H. Diaz, and H.-S. P. Wong, "Design space analysis for cross-point 1S1MTJ MRAM: Selector–MTJ cooptimization," *IEEE Transactions on Electron Devices*, vol. 67, no. 8, pp. 3102–3108, 2020.

[2] J. Woo and S. Yu, "Comparative study of cross-point MRAM array with exponential and threshold selectors for read operation," *IEEE Electron Device Letters*, vol. 39, no. 5, pp. 680–683, 2018.

[3] A. Chen, "Analysis of partial bias schemes for the writing of crossbar memory arrays," *IEEE Transactions on Electron Devices*, vol. 62, no. 9, pp. 2845–2849, 2015.

[4] L. Wan, T.-W. Wu, N. Smith, T. Santos, G. Mihajlovic, J.-L. Li, K. Patel, N. D. Melendez, B. Terris, and J. A. Katine, "Fabrication and individual addressing of STT-MRAM bit array with 50 nm full pitch," *IEEE Transactions on Magnetics*, vol. 58, no. 5, pp. 1–6, 2022.

[5] M. Reisch, "On bistable behavior and open-base breakdown of bipolar transistors in the avalanche regime-modeling and applications," *IEEE Transactions on Electron Devices*, vol. 39, no. 6, pp. 1398–1409, 1992.

[6] V. S. S. Srinivasan, S. Chopra, P. Karkare, P. Bafna, S. Lashkare, P. Kumbhare, Y. Kim, S. Srinivasan, S. Kuppurao, S. Lodha, and U. Ganguly, "Punchthrough-diode-based bipolar RRAM selector by Si epitaxy," *IEEE Electron Device Letters*, vol. 33, no. 10, pp. 1396–1398, 2012.

[7] Y. H. Song, S. Y. Park, J. M. Lee, H. J. Yang, and G. H. Kil, "Bidirectional two-terminal switching device for crossbar array architecture," *IEEE Electron Device Letters*, vol. 32, no. 8, pp. 1023–1025, 2011.

[8] S. Kim, D.-I. Moon, W. Lu, D. Hwan Kim, D. Myong Kim, Y.-K. Choi, and S.-J. Choi, "Latch-up based bidirectional npn selector for bipolar resistance-change memory," *Applied Physics Letters*, vol. 103, no. 3, p. 033505, 2013. [Online]. Available: https://doi.org/10.1063/1.4813832

[9] J.-W. Han and Y.-K. Choi, "Biristor—bistable resistor based on a silicon nanowire," *IEEE Electron Device Letters*, vol. 31, no. 8, pp. 797–799, 2010.

[10] J.-W. Han and Y.-K. Choi, "Bistable resistor (biristor) - gateless silicon nanowire memory," in *2010 Symposium on VLSI Technology*, 2010, pp. 171–172.

[11] J.-W. Han and M. Meyyappan, "Trigger and self-latch mechanisms of n-p-n bistable resistor," *IEEE Electron Device Letters*, vol. 35, no. 3, pp. 387–389, 2014.

[12] Y. J. Song, J. H. Lee, H. C. Shin, K. H. Lee, K. Suh, J. R. Kang, S. S. Pyo, H. T. Jung, S. H. Hwang, G. H. Koh, S. C. Oh, S. O. Park, J. K. Kim, J. C. Park, J. Kim, K. H. Hwang, G. T. Jeong, K. P. Lee, and E. S. Jung, "Highly functional and reliable 8Mb STT-MRAM embedded in 28nm logic," in *2016 IEEE International Electron Devices Meeting (IEDM)*, 2016, pp. 27.2.1–27.2.4.

[13] C. Park, H. Lee, C. Ching, J. Ahn, R. Wang, M. Pakala, and S. H. Kang, "Low RA Magnetic Tunnel Junction Arrays in Conjunction with Low Switching Current and High Breakdown Voltage for STT-MRAM at 10 nm and Beyond," in *2018 IEEE Symposium on VLSI Technology*, 2018, pp. 185–186.

[14] B. Das, R. Meshram, V. Ostwal, J. Schulze, and U. Ganguly, "Observation of impact ionization at sub-0.5v and resultant improvement in ideality in i-npn selector device by si epitaxy for rram applications," in *72nd Device Research Conference*, 2014, pp. 139–140.

[15] B. Das, S. Sushama, J. Schulze, and U. Ganguly, "Sub-0.2 V Impact Ionization in Si n-i-p-i-n Diode," *IEEE Transactions on Electron Devices*, vol. 63, no. 12, pp. 4668–4673, 2016.

[16] J. P. Helme and P. A. Houston, "Analytical modeling of speed response of heterojunction bipolar phototransistors," *Journal of Lightwave Technology*, vol. 25, no. 5, pp. 1247–1255, 2007.

[17] R. People, "Physics and applications of GexSi1-x/Si strained-layer heterostructures," *IEEE Journal of Quantum Electronics*, vol. 22, no. 9, pp. 1696–1710, 1986.

[18] H. Kroemer, "Heterostructure bipolar transistors and integrated circuits," *Proceedings of the IEEE*, vol. 70, no. 1, pp. 13–25, 1982.

[19] C. L. Anderson and C. R. Crowell, "Threshold energies for electron-hole pair production by impact ionization in semiconductors," *Phys. Rev. B*, vol. 5, pp. 2267–2272, Mar 1972. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.5.2267

[20] J. Li, P. Ndai, A. Goel, S. Salahuddin, and K. Roy, "Design paradigm for robust spin-torque transfer magnetic RAM (STT MRAM) from circuit/architecture perspective," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 18, no. 12, pp. 1710–1723, 2010.

[21] Y. Okuto and C. Crowell, "Threshold energy effect on avalanche breakdown voltage in semiconductor junctions," *Solid-State Electronics*, vol. 18, no. 2, pp. 161–168, 1975. [Online]. Available: https://www.sciencedirect.com/science/article/pii/0038110175900994

[22] A. Spinelli, A. Pacelli, and A. L. Lacaita, "Dead space approximation for impact ionization in silicon," *Applied Physics Letters*, vol. 69, no. 24, pp. 3707–3709, 1996. [Online]. Available: https://doi.org/10.1063/1.117196

[23] G.-B. Hong and J. Fossum, "Implementation of nonlocal model for impact-ionization current in bipolar circuit simulation and application to SiGe HBT design optimization," *IEEE Transactions on Electron Devices*, vol. 42, no. 6, pp. 1166–1173, 1995.