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# Trapping of Hot Carriers in the Forksheet FET Wall: a TCAD Study

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***Abstract*— We simulate the spatial profile of trapped charge in the forksheet FET wall under hot-carrier stress by calculating carrier distribution functions and using a non-radiative multiphonon model. We observe charge trapping above and below the horizontal projection of the sheet in the wall. We find the charge profile not to depend on the sheet width and the trapping in the forksheet FET wall to be significantly smaller than the trapping in the gate stack.**

***Index Terms*— Border traps, forksheet FETs, hot-carriers, non-equilibrium BTI, non-radiative multiphonon model.**

## I. Introduction

FORKSHEET (FS) field effect transistors (FETs) are a candidate FET architecture to continue technology scaling to 2 nm [1]. By stacking nFET and pFET sheets vertically on opposite sides of a dielectric wall, FS FETs promise a better controlled and thus reduced p- to nFET separation, allowing to scale logic cell area [2], [3]. Recently, the first FS FETs were demonstrated experimentally [4].

The intended material for the FS wall is silicon nitride, a material currently used as a charge trapping layer in non-volatile memories [5]. With increased hot-carrier degradation (HCD) in the latest technologies [6], [7], this poses a concern of FET degradation due to trapping of hot-carriers (HCs) in the FS wall. First experimental studies on the reliability of the FS wall are based on comparing nanosheet (NS) and FS FETs co-integrated on the same wafer for bias temperature instability, HCD and time-dependent dielectric breakdown [8], [9]. Complementarily, we quantified the sensing of fixed charge in the FS wall using simulations [10]. As we did not include a mechanism for the trapping process in [10], we had to assume in that work a box shape for the spatial charge profile in the wall.

Here, we extend non-equilibrium non-radiative multiphonon (NMP) models, for the first time used in compact [11], [12] and 2D TCAD [13], [14] approaches, to a full 3D TCAD approach, to calculate the trap charging *kinetics* in the FS FET wall. This allows us to simulate the spatial profile of trapped charge in the wall starting from the HC stress conditions. We provide extensive insights in the 3D nature of the FS wall charge trapping problem, we show that the spatial profile of trapped charge differs considerably from the box profile assumed before [10] and we compare the magnitude of charge trapping in the FS wall to trapping in the gate stack.

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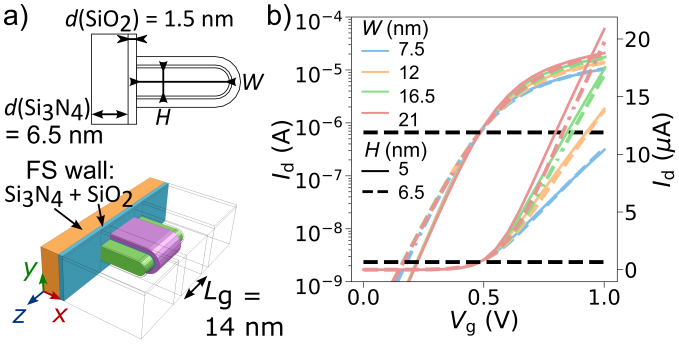


Fig. 1. a) Structure of the simulated FS FET with the key dimensions (see the "FET2" series in [10] for all dimensions). b) $\boldsymbol{I_d}$-$\boldsymbol{V_g}$'s of the FS FETs. The FETs of different sheet widths $\boldsymbol{W}$ and heights $\boldsymbol{H}$ are compared with their $\boldsymbol{I_d}$-$\boldsymbol{V_g}$'s normalized to have the same current at a fixed gate voltage (see the dashed line).

## II. Methodology

The used FS FET structures are nFETs with gate length $L_g = 14$ nm, varying sheet width $W = 7.5, 12, 16.5, 21$ nm and two sheet height $H = 5, 6.5$ nm (see Fig. 1a, same as the "FET2" series in our previous work [10]). Only one sheet is simulated. The FS FET wall is made of $Si_3N_4$ and $SiO_2$, in line with the first fabricated FS FETs of *imec* [4]. The $I_d$-$V_g$'s of the different devices are normalized to have the same current of $6.6 \times 10^{-7}$ A at a fixed gate voltage of $V_g = 0.48$ V (Fig. 1b). We refer to [10] for all device details.

The simulations consist of three steps: calculation of *i*) the carrier energy distribution functions (DFs), *ii*) the occupancy of defects in the wall and *iii*) $I$-$V$ degradation caused by the trapped charge. For our FS wall study in [10], we only performed the third step, using the assumed box charge profile as input. To obtain the DF, we solve the Boltzmann transport equation in ViennaSHE [15] in the same way as in our work on interface state generation [10]. The stress condition is $V_{g,stress} \sim V_{d,stress}$ ($V_{g,stress} > V_{d,stress}$ in Fig. 4c) and $T_{stress} = 25$ °C. As explained in [10], quantum confinement is not included in the DF calculation. Impact ionization (I/I) is also not captured and Section III discusses this simplification.

The wall defect occupancy calculation uses a custom 3D implementation of the non-equilibrium two-state NMP model of Rzepa *et al.* [16] and Jech *et al.* [13], [14]. This model takes into account *i*) the tunneling of carriers to/from the traps, *ii*) the difference between the energy $E$ of the carrier in the channel and the trap energy $E_t$, increased with the phonon-mediated deformation and relaxation energy of the defect site during charge capture/emission and *iii*) the DF at the channel/wall interface [17]. The same code and model is also used for charge trapping in the gate stack (= $SiO_2$ + $HfO_2$ layer) in Fig. 6b. Since hole trapping is only relevant for $V_{g,stress} \sim 0$ V in

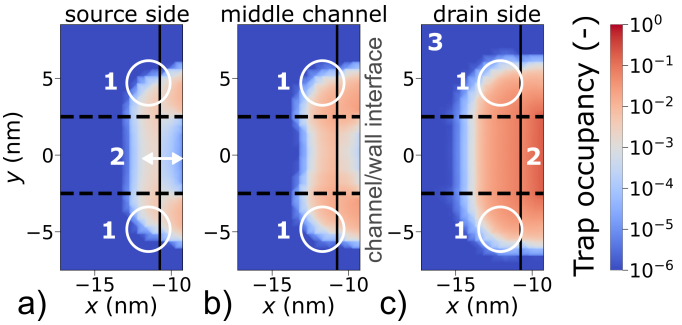


Fig. 2. FS wall trap occupancy for $V_g = 1.7$ V, $V_d = 1.6$ V, $t = 1$ ks, $W = 21$ nm, $H = 5$ nm for $x$-$y$ cuts (see Fig. 1a) in the wall at a) the source, b) the middle and c) the drain side of the channel. The silicon sheet is always to the right of the cut and is not shown. The region between the two dashed black lines (i.e. $|y| < 2.5$ nm) is the horizontal projection of the sheet in the wall. The full black line indicates the interface between the $Si_3N_4$ and $SiO_2$ layer of the wall. The numbers refer to peculiarities of the profile discussed in the text.

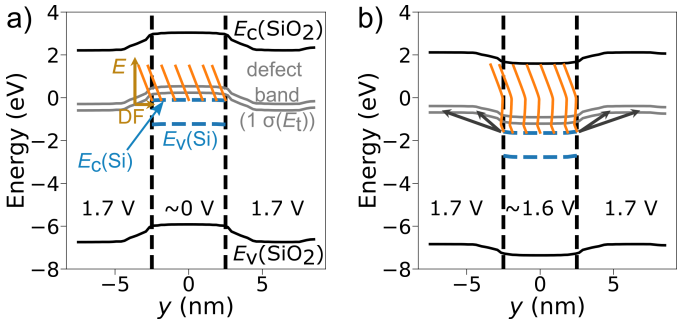


Fig. 3. Band diagram of the FS wall for a cutline in the $y$-direction (see Fig. 1a) at a depth of $0.25$ nm in the wall for two $z$-positions along the channel (same as in Fig. 2a and 2c): a) source and b) drain side. The orange curves in a) and b) are the carrier energy distribution functions and indicate how much carriers are available to charge defects at energies $E > E_c$(Si). We see that the electrons reach higher energies at the drain b) compared to the source a) side. The black arrows in b) show how carriers in the Si conduction band can charge defects above ($y > 2.5$ nm) and below ($y < -2.5$ nm) the horizontal projection of the sheet in the wall and this also applies to a) (observation # 1 in Fig. 2). The device and stress condition are the same as in Fig. 2.

nFETs [18], we restrict for the wall and gate stack dielectrics to the shallow defect bands, which trap electrons. The defect parameters for $SiO_2$ and $HfO_2$ are taken from Table 7 in [16] (foundry 28 nm column) and for $Si_3N_4$ from Table 1 in [19] (TCAD column). However, to the best of our knowledge, the $Si_3N_4$ NMP relaxation energy $S$ and curvature ratio $R$ (as defined in [16]) are not known. We used for these $Si_3N_4$ parameters the values of $SiO_2$. In Fig. 6, we then estimate the sensitivity of the resulting $\Delta I_d$ and $\Delta V_{th}$ on these parameters by varying them $\pm 20\%$ around the $SiO_2$ value.

We calculate $I$-$V$ degradation in Minimos-NT [20] using the drift-diffusion scheme. As the defects are bulk traps, only their electrostatic impact is considered (no mobility degradation).

## III. Results and Discussion

Fig. 2 shows the charge occupancy $P$ of defects in the FS wall after HC stress ($V_{g,stress} \sim V_{d,stress}$). The charged defect density $N_{ot}$ is then $N_{ot} = PN_T$, with $N_T$ the density of pre-existing traps. Three observations are apparent. *First*, defects above or below the horizontal projection of the sheet in the wall can become charged during stress. At the source side and the middle of the channel, these defects are more charged than defects lying in the horizontal projection of the sheet in the wall. *Second*, depending on the $z$-position along the channel, the charge occupancy maximum is at a certain depth away from or at the wall/channel interface. *Third*, the occupancy is larger at the drain than at the source.

To understand the first observation, we make a cutline in the wall in the $y$-direction (Fig. 3). The black arrows in Fig. 3b show how electrons in the channel conduction band can tunnel to and charge defects above ($y > 2.5$ nm) and below ($y < -2.5$ nm) the horizontal projection of the sheet in the wall (the same applies for Fig. 3a). We see a band bending over the horizontal projection of the sheet. Indeed, the parts of the wall above and below the horizontal projection of the sheet are in direct contact with the gate, which is at a fixed $V_g = 1.7$ V. The part of the wall in the horizontal projection of the sheet is in direct contact with the channel, of which the potential varies from 0 V (source side) to 1.6 V (drain side). Therefore, at the source side (Fig. 3a), the defects above and below the horizontal projection of the sheet are pulled closer (in energy) to the channel conduction band edge compared to the defects in the horizontal projection of the sheet. This leads to higher defect charging above and below, compared to that in the horizontal projection of the sheet at these positions. At the drain side, the situation is reversed (Fig. 3b).

For the second observation, we make a cutline in the wall and the channel in the $x$-direction (Fig. 4a-b). Due to the non-zero $V_d$, the orientation of the oxide field changes between the source (Fig. 4a) and drain (Fig. 4b) side of the channel. At the source side, defect energy levels are located closer to the channel conduction band edge when going deeper in the wall. This increases the defect occupancy with increasing depth. At the same time, the tunneling in the wall decreases with depth. Both factors counteract each other, leading to a maximum of the charge occupancy as a function of the depth (Fig. 2a-b). Due to the material change and the associated electric field discontinuity, this charge occupancy maximum is often at the interface between the $Si_3N_4$ and $SiO_2$ layer in the wall. At the drain side, the reversed oxide field results in defect energy levels pushed away from the channel conduction band edge with increasing depth. This reduces the charge occupancy with depth, similar to the tunneling. The net effect is a monotonic decrease of charge occupancy with increasing depth (Fig. 2c).

The source/drain asymmetry in the charge occupancy follows from the HC stress condition (large $V_{ds}$). Indeed, we find the charge occupancy profile to be fully source/drain symmetric for $V_d = 0.1$ V and to gradually show higher occupancies at the drain for larger $V_d$ (Fig. 4c).

We comment on the effect of neglecting I/I in the DF calculation on the occupancy maps in Fig. 2. From Fig. 3, we see that the DF at the channel/wall interface ($x = -9.25$ nm), needed for the calculation of the occupancy maps, only varies with the $z$-position, but not with the $y$-coordinate. The shape of the occupancy maps in the $x$ and $y$ direction is thus determined by the band bending and the tunneling in the wall. The band bending will not depend on the I/I rate, as the secondary generated carriers (holes) are orders of magnitude lower in

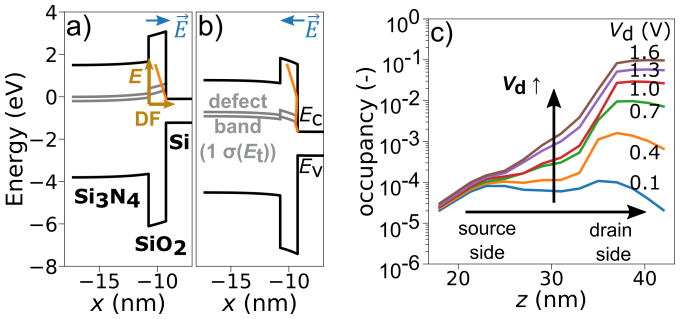


Fig. 4. a)-b) Band diagrams of the FS wall and channel for a cutline in the $x$-direction (see Fig. 1a) for two $z$-positions along the channel (same as in Fig. 2a and 2c): a) source and b) drain side. The change in the orientation of the oxide field from a) to b) explains the change in wall depth at which the maximum of the charge occupancy occurs in Fig. 2 (observation # 2). c) FS wall trap occupancy (at a depth $d = 1$ nm in the wall) for different $V_d$ at fixed $V_g = 1.7$ V. The device and stress time [for a), b) and c)] and stress voltages [for a) and b)] are the same as in Fig. 2. All cuts are in the center of the sheet in the $y$-direction.

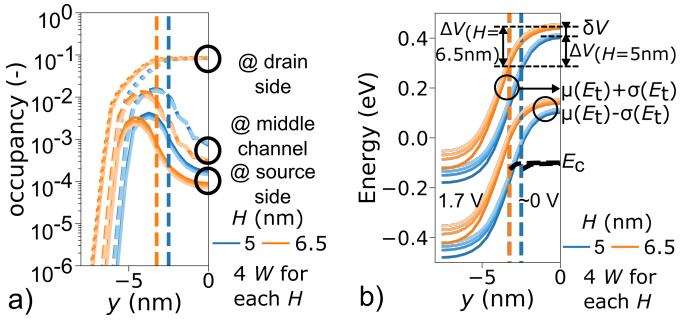


Fig. 5. a) FS wall trap occupancy as function of the sheet $H$ and $W$: cutline in the wall along the $y$-axis (see Fig. 1a) at a depth of 1 nm in the wall. The dimensions are $H = 5, 6.5$ nm (blue and orange lines respectively) and $W = 7.5, 12, 16.5, 21$ nm (indicated by different shades of the color, lines are overlapping). The stress condition is $V_g = 1.7$ V, $V_d = 1.6$ V and $t = 1000$ s. The trap occupancy shows no dependence on the sheet $W$. b) Band diagram of the FS wall with a zoom-in on the defect band for the source side of the channel as in a). In the horizontal projection of the sheet (to the right of the vertical, dashed lines), there is no difference between the four $W$'s. Only $y < 0$ is shown, as the profile is symmetric around $y = 0$ for both a) and b).

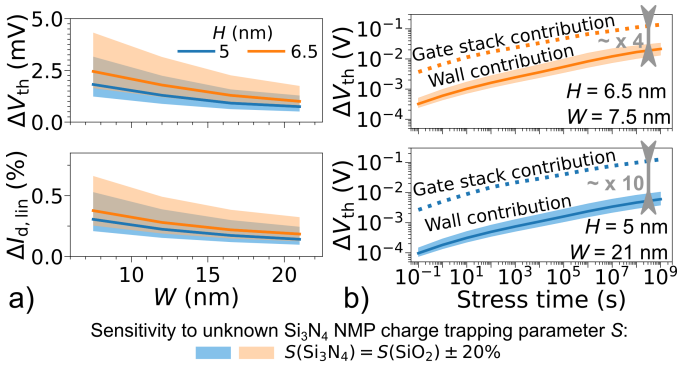


Fig. 6. $I$-$V$ degradation caused by the profiles of trapped charge in the FS FET wall a) as function of sheet width for fixed $t_{stress} = 1$ ks and b) as function of stress time for two $\{W, H\}$ pairs. The stress voltages are the same as in Fig. 5a. For the unknown $Si_3N_4$ NMP parameters $S$ and $R$, the values of $SiO_2$ were used (see full lines). The sensitivity of the calculation to these unknown parameters was determined by varying the $SiO_2$ values ± 20% and the largest variation (which is for all cases the variation of $S$) is plotted as the shaded band. In b), also $I$-$V$ degradation due to charge trapping in the gate stack is included (dashed line). No sensitivity analysis was done for the gate stack charging, as all NMP gate stack parameters are known.

concentration compared to the primary carriers (electrons) and hence will not affect the electrostatics of the device. The tunneling is also not affected by the omission of I/I. The high-energy tail of the distribution function will be lower with I/I, as I/I is an extra scattering mechanism. This effect will be in the first order the same for all sheet widths, since they have the same gate length. Consequently, our calculated occupancy maps will still have the same shape, but might be slightly overestimated at the drain end.

Next, we study the FS wall trap occupancy profile as function of the sheet $W$ and for two sheet $H$'s in Fig. 5a. We observe no dependence of the occupancy profile on the sheet $W$ and no difference (at the drain side) between the two $H$ values. Only at the source and in the middle of the channel, where the trap occupancy is significantly lower compared to the drain side, the defect occupancy differs between the two $H$ values, with the taller $H$ having the lower occupancy. To understand this, we plot the energy position of the defect band in the wall at the source for all FETs in Fig. 5b. For all $\{W, H\}$ pairs, the conduction band edges in the silicon channel lie at the same energy. Similar to Fig. 3, we observe band bending over the horizontal projection of the sheet in the wall. We then find that the sheet with the taller $H$ can accommodate a larger band bending compared to the one with the lower $H$. Consequently, in sheets with the taller $H$, defect energy levels are shifted further away from the channel conduction band edge, resulting in lower charge occupancy there.

Finally, Fig. 6a shows $I$-$V$ degradation caused by the trap occupancy profiles of Fig. 5a. Although the occupancy profiles are independent of the $W$ (Fig. 5a), the $I$-$V$ degradation decreases with increasing $W$. Indeed, FETs with a wider $W$ have a larger part of the channel far away from the wall, causing the same charge to be felt less by wider $W$'s [10]. The $I$-$V$ degradation is larger for the taller $H$. Since the largest trap occupancy is at the drain and is $H$-independent (Fig. 5a), the taller $H$ has more charge in the wall, explaining its larger $I$-$V$ degradation. Fig. 6b shows that $I$-$V$ degradation due to FS wall trapping is smaller than degradation due to trapping in the gate stack for all stress times. For the FS FET with the largest wall trapping (smallest $W = 7.5$ nm, tallest $H = 6.5$ nm), trapping in the wall is a factor 4 smaller than trapping in the gate stack, under the assumption of the unknown $Si_3N_4$ NMP parameters being 20% worse than the ones of $SiO_2$. For the FS FET with dimensions from the roadmap ($W = 21$ nm, $H = 5$ nm) [1], the difference increases to a factor 10. This implies that trapping in the FS FET wall has limited impact on the total device degradation after HC stress. Consequently, we do not expect FS wall trapping to be a reliability red flag for the further development of the FS FET topology.

## IV. Conclusion

We simulated the trap occupancy profile in the FS FET wall under HC stress using carrier DFs and non-equilibrium non-radiative multiphonon physics. We observe charge trapping above and below the horizontal projection of the sheet in the wall. We find the trap profile to be independent on the sheet width and $I$-$V$ degradation due to FS wall trapping to be substantially smaller than due to trapping in the gate stack.

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