Back Barrier Trapping Induced Resistance Dispersion in GaN HEMT: Mechanism, Modeling, and Solutions

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Abstract**—**Trapping in an impurity (e.g. Fe, C) doped back barrier (BB) causes pronounced on-resistance (R_{on}) dispersion of GaN HEMTs. We demonstrate that the BB trapping is alleviated by increasing 2DEG density N_{sh} in the GaN channel (~50% increased N_{sh} results in ~30% less ΔR_{on}) and inserting an additional intrinsic AlGaN BB (100 nm AlGaN with ~50% less ΔR_{on}). We propose a novel flat-AlGaN-BB-energy-band designing criterion for the AlGaN/C-GaN BB combination.

INTRODUCTION

Downscaled GaN HEMTs make candidates for 5G/6G RF applications. A back barrier (BB) in a short-channel HEMT provides 2DEG confinement and improves gate control. But BB trapping (can be categorized into buffer trapping) causes HEMT current collapse, the mechanism of which still not fully understood according to recent technical reviews [1], [2].

In past studies [1], [2], the BB trapping is mainly investigated with a HEMT biased in an off state or a semi-on state with high drain-to-source voltages (V_{ds}); the gate-drain corner regions are subject to high lateral electric fields (E_x) in those states, and the high E_x may induce both top barrier (TB) surface trapping and BB trapping. We demonstrate in this study that significant BB trapping occurs even with small and moderate E_x in HEMTs. This provides insight into the memory effects induced by GaN HEMT trapping in an RF power amplifier (PA), where the Ex across 2DEG and BB constantly vary. Further, we propose solutions to reduction of the BB trapping. While experimentally investigated on carbon doped GaN (C-GaN) BB, the proposed trapping characterizations, models, and solutions apply to general impurity doped BB.

EXPERIMENTAL

The III-N stacks were grown by MOCVD on a high resistivity 200 mm Si (111) substrate. After an $Al_xGa_{1-x}N$ buffer layer and 1 μm ~6×10^{19} cm^{-3} C doped C-GaN BB growth, three groups of samples were prepared:

(1) Samples with 15 nm $Al_{0.28}Ga_{0.72}N$ TB, 1 nm "AlN" (Al-rich $Al_xGa_{1-x}N$ [3]) interlayer, and 10, 20, 35, 50, 100, 150, or 300 nm unintentionally doped GaN (i-GaN) channel;

(2) Samples with 10 nm $In_{0.18}Al_{0.82}N$ TB, 1 nm "AlN", and 50, 100, 150, or 300 nm i-GaN channel;

(3) Samples with 10 nm $Al_{0.28}Ga_{0.72}N$ TB, 1 nm "AlN", 35 or 50 nm i-GaN channel with or without additional unintentionally doped $Al_{0.08}Ga_{0.92}N$ BB (i-AlGaN BB)—i-AlGaN BB thicknesses (th_{BB}) were 15, 100, or 250 nm.

Transmission line model (TLM) resistors and HEMTs were fabricated: HEMTs with 80 nm gate length (L_g) and 9-nm-thickness-left recessed barrier under the gate metal. Complete device fabrication refers to our previous work [4].

CHARACTERIZATIONS

Majority of C act as deep acceptors in C-GaN, which make C-GaN effectively p-type. We extract a net acceptor concentration of ~3×10^{19} cm^{-3} from ~6×10^{19} cm^{-3} C doped C-GaN BB (Fig. 1). Reducing the i-GaN channel thickness (th_{ch}) enhances 2DEG confinement (Fig. 1a) but sacrifices the 2DEG density (N_{sh}) in GaN heterostructures (Fig. 1b). We will demonstrate that reducing th_{ch} also worsens the C-GaN BB induced HEMT on-resistance (R_{on}) dispersion problem.

Trapping induced memory effects are common to GaN devices. But it is difficult to distinguish the BB trapping from other trapping mechanisms due to the complex III-N stack. We adopt substrate-floating two-terminal TLM structures (Fig. 2a) for the BB trapping investigation: TLMs have simple resistance components—contact resistances R_c and 2DEG resistances R_{2D}—and simple E_x distribution across the 2DEG and the BB. Constant V_{ds} stress (V_{str}) is applied for a duration (t_{str}) on the TLM; trapping is monitored by variations of the TLM linear resistance $\Delta R_{TLM,lin}$ (Fig. 2b). We demonstrate that the drain-current I_{ds} transients of gateless TLMs particularly capture the BB trapping behaviour.

Default TLMs under test are 10 μm wide with an electrode spacing of 1.5 μm. The $R_{TLM0,lin}$ of fresh TLM resistors with various TB and th_{ch} are recorded in Fig. 3. The applied V_{str} is not greater than 10 V, corresponding to (initial) $E_x<10^5$ V/cm.

The R_{TLM} with 50 nm th_{ch} are compared in Fig. 5 after 1s stress with varied V_{str}. Key observations include:
(1) The $\Delta R_{TLM,lin}$ increases with V_{str} after the 1s stress;
(2) Even with the short 1s stress, the $\Delta R_{TLM,lin}$ is significant;
(3) A major $R_{TLM,lin}$ relaxation time constant τ_{rel} is observed;
(4) The $R_{TLM,lin}$ after high-V_{str} stress does not always recover to $R_{TLM,lin0}$ even after long relaxation period (>36 hours in Fig. 5).

The R_{TLM} with 50 nm th_{ch} are compared in Fig. 6 after 10 V stress with varied t_{str}. Key observations include:
(1) Time constants τ_{str1} and τ_{str2} are observed in the stress phase;
(2) $\Delta R_{TLM,lin}$ does not increase infinitely with time but reaches a saturation magnitude of 0.22~0.32 Ω·mm after 10-100s stress.

Significant ΔR_{TLM} are caused after the moderate-E_x stress tests. Next, we link the ΔR_{TLM} to the BB trapping, model the process with SPICE and TCAD, and propose solutions.

MECHANISM EXPLORATION

A. ΔR_{TLM} increased with GaN channel thinning

Trapping in a TLM under E_x may have three origins: the TB, the i-GaN channel, and the BB. In the first order, trapping in the TB has little dependence on the th_{ch}, that in the i-GaN channel increases with the th_{ch}, while that in the BB decreases with the th_{ch}. Significantly increased $\Delta R_{TLM,lin}$ with the $1/th_{ch}$ in Fig. 7 suggests dominant BB trapping.

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B. Asymetric ΔR_{TLM} at the source and drain sides

Due to charge redistribution, BB trapping would typically result in asymmetric ΔR_{on} in a device—greater ΔR_{on} at the drain side than at the source side. To verify this signature, end resistance measurement of source (R_S^*) and (R_D^*) [5] is performed on a MIS-HEMT. The MIS-HEMT have similar 2DEG R_{sh} under the gate (~350 Ω/sq) and in the access region (~320 Ω/sq) (Fig. 8), making the gate-floating MIS-HEMT a close approximation to a TLM resistor. The R_S^* and R_D^* measurement approach is introduced in Fig. 8 and Fig. 9. The ΔR_S^* and ΔR_D^* vs t_{str} behavior aligns with BB trapping.

SPICE AND TCAD MODELING

A semi-physical SPICE model [14] is constructed (Fig. 10) to simulate the dynamic R_{TLM} transients. The 2DEG R_{2D} is modelled as an equivalent depletion-mode backgated MOSFET whose N_{sh} is modulated by BB trapping. The MOSFET has a back gate capacitance C_{BG} equal to the GaN channel capacitance $C_{BG}=\varepsilon_{GaN}/th_{ch}$ (ε_{GaN} is the permittivity of GaN) and has a zero-gate-bias channel resistance and a carrier density matching the R_{2D} and the N_{sh} of a fresh TLM resistor. The $R_{2D,hf}$ in the stress phase and the $R_{2D,lin}$ in the relaxation phase (both in Ω·mm) are defined separately in a simplified manner

$$R_{2D,hf} = V/(qN_{sh}v_{sat}) \qquad (1)$$

$$R_{2D,lin} = L/(qN_{sh}\mu_{lin}) \qquad (2)$$

where V is the lateral bias voltage on a lump 2D resistor, v_{sat} is the 2DEG saturation velocity, μ_{lin} is the room-temperature 2DEG low-field mobility, and L is the length of the TLM resistor. The C-GaN resistance R_{CGaN} (Fig. 10) adopts magnitudes from previous C-GaN transport studies [6], [7]. The self-heating effects on TLM are also included in SPICE modeling: the average device temperature T_{DUT} is estimated by $T_{DUT}=R_{th}I_{ds}V_{ds}$, where the R_{th} is the thermal resistance of devices [8]. The T_{DUT} estimation helps accurately transfer experimentally extracted activation energies of τ_{str1}, τ_{str2}, τ_{rel}, into those of resistance components in the SPICE model.

The SPICE model presumes speculated BB trapping/ detrapping processes described in Fig. 11. The results in Fig. 10 reproduce the stress/relaxation transient features and agree with experimental ΔR_{TLM}-th_{ch} relationships in Fig. 7.

The TLM trapping is also investigated with Sentaurus TCAD modelling [13]: the energy band diagrams near the source and the drain are compared at the initial state and after 10^3s stress in Fig. 12. In both SPICE and TCAD modelling, charges trapping in the BB near the drain causes strong 2DEG depletion (Fig. 12c)—the decreased ΔN_{sh} is approximately proportional to $C_{BG}=\varepsilon_{GaN}/th_{ch}$. This highlights a HEMT downscaling challenge, whereby the improved 2DEG confinement by decreasing th_{ch} comes at the price of increasing the BB induced ΔR_{on}.

SOLUTIONS

The R_{TLM} is sensitive to the 2DEG density N_{sh}, and so is the R_{on} of GaN HEMT. If we drastically neglect the V, v_{sat} and μ_{lin} dependence on N_{sh} in (1) and (2), the ΔR_{TLM} follows

$$\Delta R_{2D,hf} \approx \frac{-\Delta N_{sh}V}{qN_{sh}^2 v_{sat}} \propto -\frac{C_{BG}}{N_{sh}^2} \approx -\frac{\varepsilon_{GaN}}{N_{sh}^2 th_{ch}} \qquad (3)$$

$$\Delta R_{2D,lin} \approx \frac{-\Delta N_{sh}L}{qN_{sh}^2 \mu_{lin}} \propto -\frac{C_{BG}}{N_{sh}^2} \approx -\frac{\varepsilon_{GaN}}{N_{sh}^2 th_{ch}} \qquad (4)$$

Therefore, increasing N_{sh} and reducing the back gate C_{BG} would help alleviate the BB induced R_{on} dispersion. Next, we demonstrate two technological solutions based on this strategy.

A. Increase 2DEG N_{sh} with alternative top barrier material

Compared to the N_{sh} of 1.2~1.5×10^{13} cm^{-2} of $Al_{0.28}Ga_{0.72}N$/AlN/GaN (with th_{ch} from 50 to 300 nm, Fig. 1), that of $In_{0.18}Al_{0.82}N$/AlN/GaN reaches 2~2.3×10^{13} cm^{-2}. Both the $R_{TLM,hf}$ and the $R_{TLM,lin}$ of InAlN TB heterostructures show less dispersion (Fig. 13); particularly, the $R_{TLM,hf}$ with InAlN TB is consistently ~30% lower than the AlGaN counterparts.

B. Low-Al content AlGaN BB between 2DEG and C-GaN

Insertion of an additional intrinsic AlGaN BB between the GaN channel and the C-GaN BB effectively reduces C_{BG} in (3) and (4). The resulting reduction of ΔR_{TLM} is verified in Fig. 14. A design criterion was lacking in literature for the AlGaN/C-GaN combined BB [9]–[11], because of complexity of the BB parameters involved including (I) the Al% in the AlGaN, (II) the th_{BB} of AlGaN BB, (III) the C concentration in the C-GaN BB. Here we propose a (near) flat-energy-band-AlGaN-BB (FEBABB) criterion (Fig. 15): it helps preserves a high back barrier height and the 2DEG confinement provided by the C-GaN; it provides a flexible th_{BB} design to reduce C_{BG}; it helps avoid formation of 2DEG/2DHG channels at i-GaN/AlGaN BB/C-GaN BB interfaces; it provides margins for drifts of BB parameters (I-III) but still guarantees the above merits. When a BB is designed based on the FEBABB criterion (Fig. 15), the negative C-GaN charges are screened by the net positive polarization charge at the i-AlGaN/C-GaN interface, while the net negative polarization at the i-GaN/i-AlGaN interface provides 2DEG confinement—Drain induced barrier lowering (DIBL) compared in Fig. 16. With the BB trapping alleviated by reducing the C_{BG}, reduced knee voltage walk-out (Fig. 17) and improved output power and power added efficiency (Pout/PAE) under RF operation (Fig. 18) are demonstrated with 80 nm L_g HEMTs.

CONCLUSIONS

A measure-stress-measure investigation of TLM resistors proves efficient to characterize the back barrier (BB) trapping impact on R_{on} dispersion at varied lateral electric field (E_x). This lays foundations for accurate modeling memory effects of GaN HEMT PA. GaN channel thinning between the top barrier and the C-GaN BB seriously increase R_{on} dispersion. Solutions are demonstrated by increasing 2DEG density and inserting an additional AlGaN BB. The short-channel HEMTs are expected to benefit from the enhanced 2DEG confinement and minimized BB trapping impacts, when combining those two solutions.

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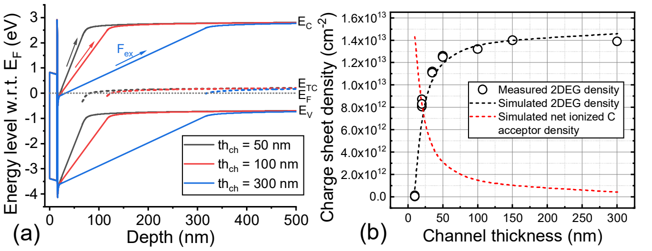

Fig. 1 (a) Simulated energy band diagrams and (b) sheet charge densities in AlGaN/AlN/GaN heterostructures with varied th_{ch}. 3×10^{19} net acceptors in C-GaN BB is assumed in simulation [12].

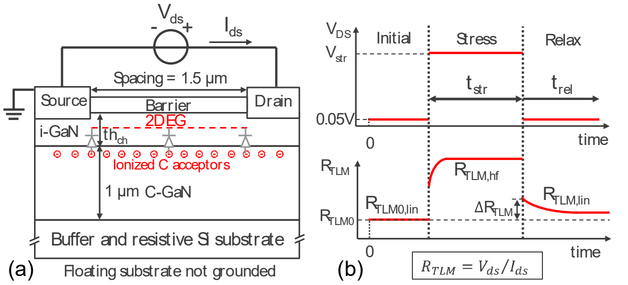

Fig. 2 Schematics of (a) TLM resistor stacks and (b) measure-stress-measure flow for TLM resistors.

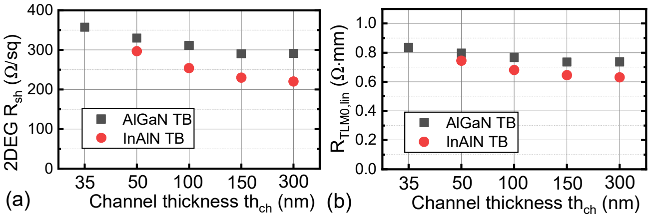

Fig. 3 (a) R_{sh} and (b) $R_{TLM,lin}$ measured from fresh AlGaN/AlN/GaN and InAlN/AlN/GaN heterostructures with varied th_{ch}.

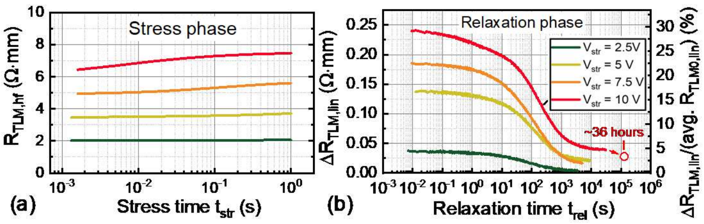

Fig. 5 (a) $R_{TLM,hf}$ transients in the stress phase and (b) $\Delta R_{TLM,lin}$ in the relaxation phase with same th_{ch}=50 nm, same t_{str}=1s, and varied V_{str} from 2.5V and 10V.

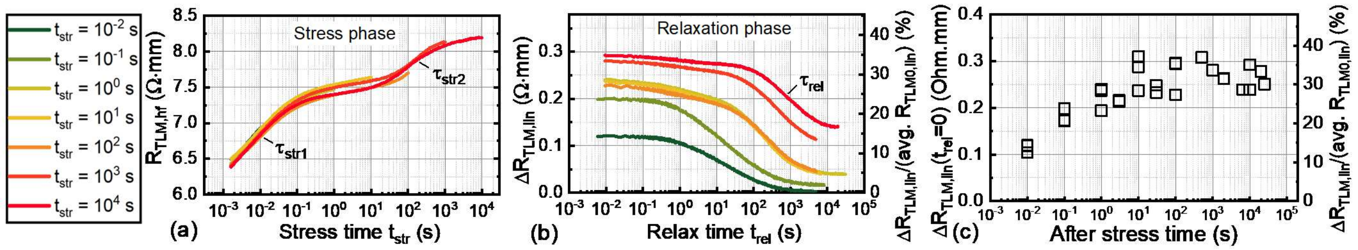

Fig. 6 (a) $R_{TLM,hf}$ transients in the stress phase and (b) $\Delta R_{TLM,lin}$ transients in the relaxation phase with same th_{ch}=50 nm, same V_{str}=10V, and varied t_{str} from 10 ms to 10 ks. (c) $\Delta R_{TLM,lin}$ measured right after 10V stress, each symbol from fresh device.

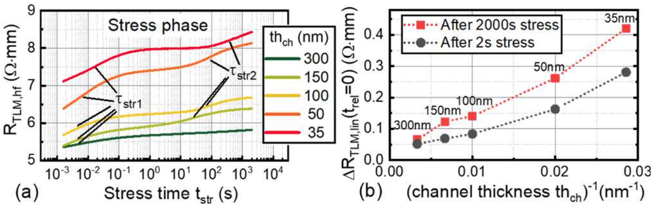

Fig. 7 (a) $R_{TLM,hf}$ transients in the stress phase with same V_{str}=10V, same t_{str}=2000s, and varied th_{ch}. (b) $\Delta R_{TLM,lin}$ right after 2000s or 2s 10V stress.

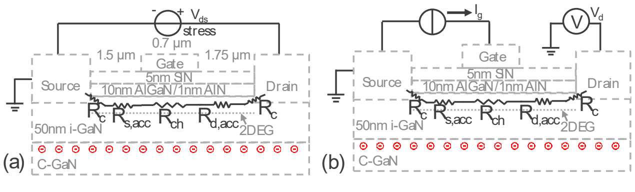

Fig. 8 (a) V_{ds} stress on gate-floating MIS-HEMT, a scenario close to V_{ds} stress on TLM resistor, because R_{sh} is comparable under gate and in access regions. (b) Schematic of source end R_s^* measurement.

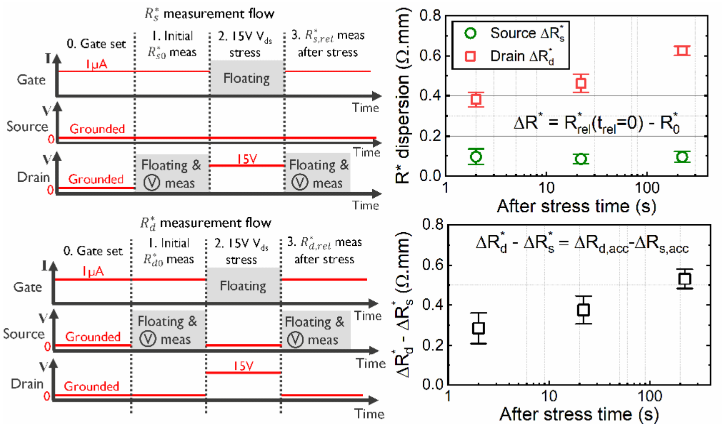

Fig. 9 End resistance R* measurement flow and results. R_s^* was measured with source grounded, I_g injection, and V_d detection; R_d^* was measured with drain grounded, I_g injection, and V_s detection. Asymmetric ΔR_s^* and ΔR_d^* suggests current collapse and 2DEG depletion mainly origin from drain access region.

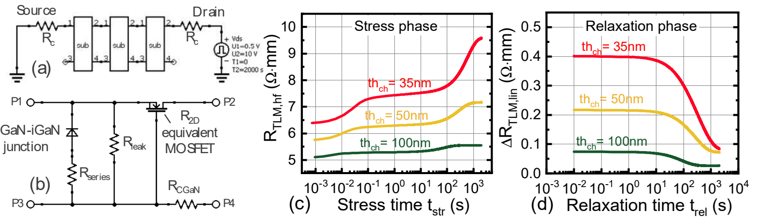

Fig. 10 (a) SPICE based equivalent circuit of TLM and (b) its subcircuit: C-GaN-i-GaN junction is modelled as PN diode; R_{2D} is modelled as MOSFET; R_{CGaN} approximates charge redistribution resistance in C-GaN; R_{series}, and R_{leak} are fitting parameters to simulate τ_{str1}, τ_{str2}, τ_{rel}, and ΔR_{TLM}. (c) $R_{TLM,hf}$ transients in stress phase and (b) $\Delta R_{TLM,lin}$ transients are simulated with SPICE for a 10V 2000s stress experiment.

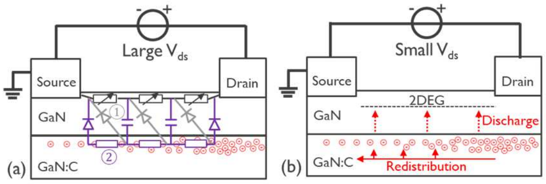

Fig. 11 Schematics describing the charge flow in (a) stress phase and (b) relaxation phase. C-GaN-i-GaN junctions are viewed as PN diodes; PN diodes are turned on by V_{ds} but then turned off again by injected charges into BB. Leakage through PN diodes near drain controls the saturation ΔR_{on} [1]. Stress phase contains ① fastest BB charging route and ② a relatively slower charging route and charge redistribution in BB.

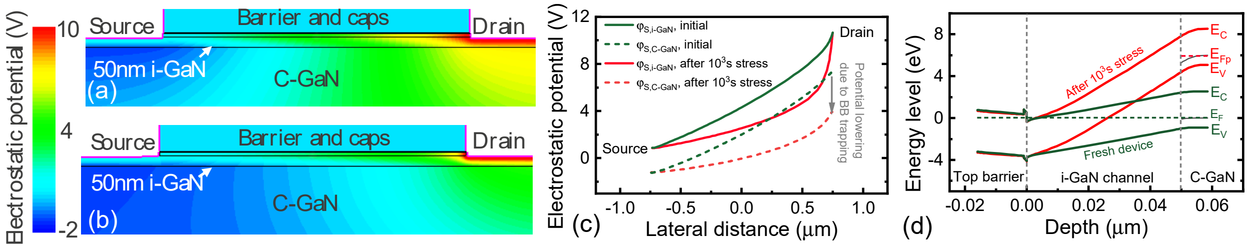

Fig. 12 TCAD modeling of AlGaN/AlN/GaN/C-GaN based TLM resistor with 1.5 μm source/drain spacing. Electrostatic potential is simulated for the stress phase (a) at the beginning and (b) after 10^3s stress. (c) Electrostatic potential is further compared with lateral cut lines at the i–GaN channel surface ($\varphi_{s,i\text{-}GaN}$) and at the i-GaN/C-GaN interface ($\varphi_{s,C\text{-}GaN}$). (d) Cross-sectional energy band diagrams are compared near the drain before and immediately after stress; the C-GaN energy band is lifted after the stress due to BB charging, which further causes 2DEG depletion.

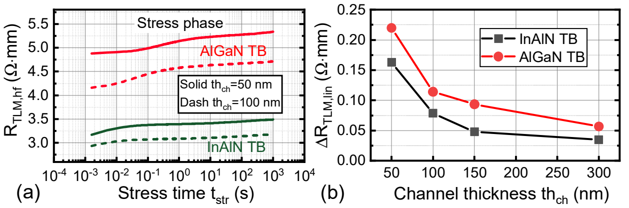

Fig. 13 (a) $R_{TLM,hf}$ transients in the stress phase with same V_{str}=7.5V, same t_{str}=1000s, varied TB, and varied th_{ch}. (b) $\Delta R_{TLM,lin}$ right after 1000s stress with varied TB.

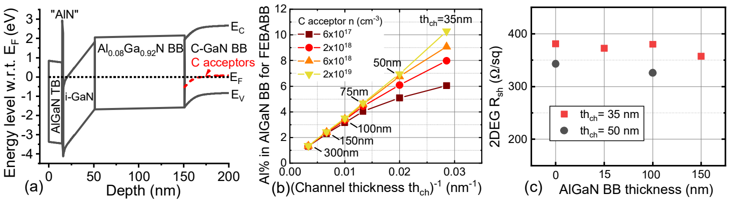

Fig. 15 (a) Heterostructure with $Al_{0.08}Ga_{0.92}$N/C-GaN BB following FEBABB. (b) Required Al content in AlGaN BB to achieve FEBABB. (c) Similar 2DEG R_{sh} with varied AlGaN th_{BB} is a fingerprint of FEBABB.

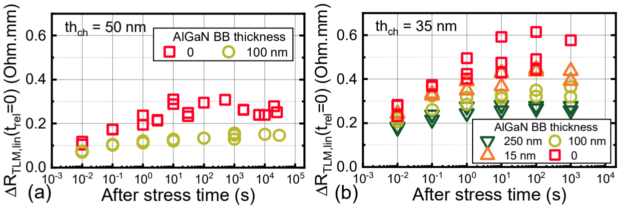

Fig. 14 $\Delta R_{TLM,lin}$ right after 10V stress with varied t_{str}, varied $Al_{0.08}Ga_{0.92}$N th_{BB}, and two th_{ch} of (b) 50 nm and (c) 35 nm.

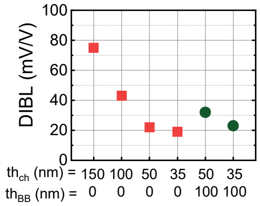

Fig. 16 DIBL measured at 10V V_{ds}.

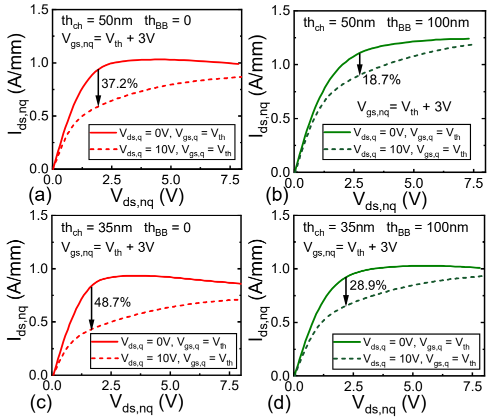

Fig. 17 Pulsed I_{ds}-V_{ds} of HEMTs (a)(c) without and (b)(d) with $Al_{0.08}Ga_{0.92}$N BB for th_{ch}=50nm or 35nm. Maximum current collapse percentage shown in each plot after high-V_{ds} off-state quiescent bias stress.

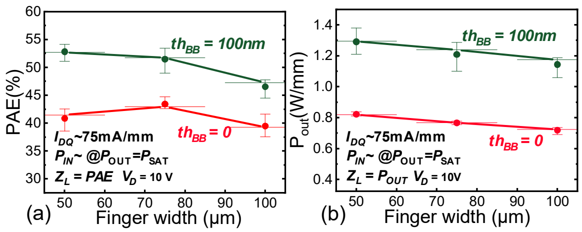

Fig. 18 (a) PAE and (b) P_{out} of 2-finger HEMTs from 28GHz passive 1ms pulsed load-pull characterizations at V_{ds} of 10V, Z_L matched for (a) PAE and (b) P_{SAT}. Th_{ch}=35 nm, L_{gd}=1.75 μm, L_{gs}=0.75 μm.