First demonstration of field-free perpendicular SOT-MRAM for ultrafast and high-density embedded memories

K. Cai[1], G. Talmelli[1], K. Fan[1,2], S. Van Beek[1], V. Kateel[1,2], M. Gupta[1], M.G. Monteiro[1], M. Ben Chroud[1,3], G. Jayakumar[1], A. Trovato[1], S. Rao[1], G.S. Kar[1], and S. Couet[1]
[1]imec, Kapeldreef 75, 3001 Leuven, Belgium, email: email: Kaiming.Cai@imec.be, [2]ESAT, KU Leuven, 3001 Leuven, Belgium,
[3]Department of Physics and Astronomy, KU Leuven, 3001 Leuven, Belgium

***Abstract*—**For the first time, we experimentally demonstrate the field-free switching in multi-pillar (MP) spin-orbit torque magnetic random-access memory (SOT-MRAM) devices, which are CMOS-compatible 300mm integrated perpendicular MTJs (p-MTJs). The field-free switching (FFS) is achieved by integrating an additional in-plane (IP) magnet layer below the conventional heavy metal layer, forming a hybrid spin source layer. The in-plane magnet contributes to additional unconventional spin-orbit torque, breaking the symmetry for field-free switching and leading to high SOT switching efficiency. We demonstrate ultrafast field-free switching with current pulses down to 0.3 ns, corresponding to a power consumption of 60 fJ/bit. Moreover, this FFS scheme is fully compatible with the standard integration process and the voltage-gated SOT (VG-SOT) switching in MP devices. Selective operations of independent write and read between multiple MTJs on a shared SOT track can also be achieved without external magnetic field. The FFS concept is scalable, agnostic to SOT material, and enables the reduction of the external periphery (*i.e.*: transistors). Thus, our proposed concept is advantageous for further improving the density and energy efficiency of SOT-MRAM technology.

I. Introduction

MRAM has become a strong candidate for embedded memories, due to its non-volatility, infinite endurance (>10^{12}), fast speed (ns timescale), low power consumption and good CMOS and BEOL compatibility. To date, spin-transfer torque (STT)-MRAM has become a mature technology in recent years with major foundries announcing large volume production of embedded STT-MRAM products, which have been used as the replacement of e-FLASH [1]. However, the nanoseconds incubation delay and endurance issues of STT-MRAM makes it unsuitable for high-level memory, such as L1/L2 cache SRAM replacement [2].

Recently, SOT-MRAM has been highlighted as a potential candidate owing to its sub-ns switching speeds and enhanced endurance due to separated read/write paths [2, 3]. However, the relatively high switching current and the 3-terminal configuration adversely impacts its reliability and bit-cell area, thus limiting the integration density. Moreover, an in-plane external field is typically required to achieve deterministic switching in perpendicular SOT-MRAM, which is also an obstacle for integration. To mitigate these issues, concepts of selective operations through voltage-control multi-bits and SOT shared-write-channel [4,5,6] have been proposed. However, field-free solutions compatible with multi-pillar operations are still not well developed. Although several methods have been proposed to remove the necessity of the external field [7,8,9], these solutions compromise scalability and efficiency due to the complexity for the write operation and device integration, making the solutions impractical for MRAM products.

In this paper, we propose and demonstrate a field-free SOT switching scheme in multi-bit integrated p-MTJs with bit-selective R/W operations on 300mm wafers. Our demonstration removes the necessity of the external field and reduces the number of transistors/bit and switching current simultaneously, providing a reliable solution for high-density and low power SOT-MRAM.

II. Hybrid SOT for field-free SOT-MRAM

A. *Concept of field-free switching multi-pillar device*

In conventional SOT devices, the spin currents are generated from heavy metals (such as W, Pt, and Ta) or their alloys, exhibiting an in-plane spin polarization [10]. To switch a p-MTJ device, an in-plane external field is generally needed to break the symmetry for achieving deterministic switching. Magnets with in-plane anisotropy can also contribute to unconventional SOT with out-of-plane spin polarization for FFS [11]. Here, we propose an FFS scheme of a hybrid SOT track, which consists of a heavy metal and an in-plane magnet, combining the high spin generation and unconventional SOT for FFS (as shown in Figure 1). In this scheme, the additional in-plane magnet layer is separated from the MTJ pillars by the SOT track, which can accommodate multiple pillars, thereby enabling voltage-controlled selective R/W operations.

B. *Film stack development and device integration*

In this work, each MTJ consists of a top-pinned MTJ stack defined as substrate/[magnet/W]/CoFeB (FL)/MgO/CoFeB (RL). Compared to the conventional SOT-MTJ structure, an additional magnetic layer was deposited below the W layer, forming a hybrid SOT track to generate the spin current and break the symmetry. Figure 2 shows the resistivity of W in a magnet/W (*t* nm) structure as deposited and after annealing. The high resistivity of ~130 μΩ·cm is obtained for W thickness less than 3.2 nm, indicating a β-W [3].

The devices were fabricated in the IMEC 300mm pilot line. Figure 3 shows the cross sections views of the proposed MTJ devices. The in-plane magnet below the heavy metal has minimal impact on the integration process, which is the same as in our previous reports [3,5]. In Fig. 4, we show a typical hysteresis loop of a 60nm-sized MTJ. The square shape of the

R-B curve indicates good PMA of the device. The size dependent MTJ performance was evaluated (over 100 devices/CD size) as shown in Fig. 5. For 80nm MTJs, the median values of TMR, coercivity (B_c) and offset field (B_{offset}) are 105%, 55.4 mT, and -22.3 mT, respectively. In Fig. 6, the thermal stability (Δ) and anisotropy field (B_k) of FFS samples are ~ 50 k_bT and 120 mT, respectively. No distinct differences in Δ and B_k were found between the FFS and W-POR samples. The SOT track resistivity is 155 μΩ·cm, which is in line with the resistivity of β-W. The bottom magnetic layer has limited impact on the free and SOT layer.

III. Field-free SOT swtiching peformance

A. Field-free SOT switching

Figure 7 shows the typical current-induced magnetization switching curves in an 80nm MTJ device under different in-plane external fields (B_x). The deterministic switching loops can be obtained even at zero B_x. The field-free switching is achieved in devices with different CDs. We extracted the effective fields (B_{eff}) for FFS from the sign change in switching polarity. The results are summarized in Fig. 8. B_{eff} increases with shrinking the CD size, which is beneficial for device scalability. In small devices (with CD < 100 nm), strong B_{eff} is obtained, which can go up to 40 mT. While in large MTJ devices, it is difficult to get full field-free switching due to insufficient B_{eff}.

B. SOT efficiency and switching performance

The SOT efficiency is characterized by current-induced hysteresis loop shift measurement [12]. From Fig. 9, the non-zero SOT efficiency (χ_{SOT}) at B_x = 0 mT confirms the unconventional SOT for field-free switching, corresponding to an effective spin Hall angle (θ_{SH}) of -18.1%. A total effective θ_{SH} of -37.6% in hybrid SOT track can be obtained under B_x = -30mT (green dash line $\theta_{SH,\beta\text{-W}}$ = -32% [3]), indicating that the in-plane magnet contributes the additional spin generation (with θ_{SH} = -5.6%), which is in good agreement with previously reported results [13].

Figure 10 shows the FFS loops for different pulse widths. The ultrafast switching can be obtained with pulse down to 0.3 ns. In a typical 60nm device, the switching current density at 1 ns is 5.7×10^{11} A/m^2 with a power consumption of 60 fJ. The benchmark plots of J_{sw} vs. Δ and E_{sw} vs. Δ are shown in Figure 11. Devices with hybrid SOT track show high SOT efficiency, which is comparable with W-POR samples.

Figure 12 shows the 63%-lifetime measurement results of FFS devices. From extrapolation [14], an endurance of $>10^{12}$ could be expected in both CD = 60 and 80 nm devices at the switching current for P_{sw} = 50%.

IV. Voltage-gated field-free switching

A. VCMA effect and VG-SOT switching in single pillar

To further enhance the SOT efficiency and device density, a voltage-gated scheme was proposed in the FFS devices by utilizing the VCMA effect [4, 5]. We evaluate the impact of gate voltage (V_G) for VCMA-induced modulations of magnetic anisotropy (B_k) and switching current (I_{sw}) in our FFS devices (as illustrated in Figure 13). Figure 14 shows the R-B loops with V_G. We extracted the anisotropy field B_k from hysteresis loops of MTJs with V_G. B_k-V_G curves of MTJs show a slope of -34.7 mT/V in Fig. 15. The corresponding VCMA coefficient is estimated to be ~17.5 fJ/Vm.

Figure 16 shows the switching loop and switching probability (P_{sw}) for different V_G in a 60 nm MTJ at 1 ns pulse. I_{sw} shows a linear dependence on V_G. A ~30% reduction in I_{sw} can be obtained by applying V_G within 0.5 V.

B. Voltage-gated FFS and selective operation in multi-pillar devices

Similarly, we performed the VG-SOT switching measurements in the MP devices. In the measurements, we completely removed the magnet fields, the deterministic switching with different gate voltages can also be obtained. Figure 17 shows the typical VG-SOT switching loops in one of four MTJs in MP devices. By applying gate voltages, the FFS could be modulated to a higher/lower critical switching voltage, enabling the selective operations of multi-bits [5].

Combined on our experimental observations, the results on FFS SOT performance with previously reported technologies are summarized in Table 1. The proposed FFS scheme by hybrid SOT track exhibits good compatibility with high-density integration and maintains high SOT efficiency. Further optimizations may focus on improving switching efficiency, reliability (WER performance) and VCMA coefficient.

V. Conclusions

We demonstrated a field-free perpendicular SOT-MRAM design by a hybrid spin source layer, consisting of a heavy metal and an in-plane magnet. The hybrid spin source enables ultrafast field-free switching with high switching efficiency and fast operational speed down to 0.3 ns. Moreover, this scheme is suitable for multi-bit SOT devices and is CMOS and back-end-of-line compatible. Our solution provides a path for high performance and high-density MRAM applications.

Acknowledgment

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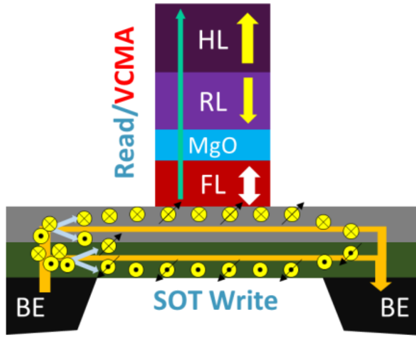


Fig. 1. Schematic of the field-free switching MTJ stack with hybrid SOT track design: SOT(magnet + heavy metal)/CoFeB(FL)/MgO/CoFeB(RL)/SAF(HL).

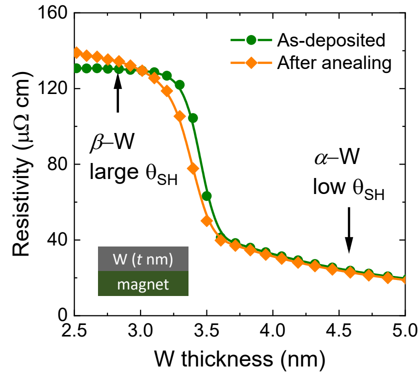


Fig. 2. W resistivity as a function of thickness in a magnet/W bilayer structure.

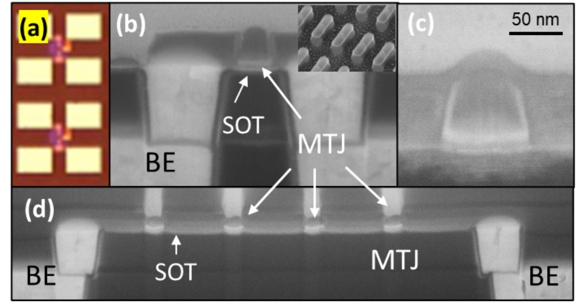


Fig. 3. (a) An optical image of MTJ devices. (b) TEM cross section view of a single pillar device. (c) Zoom in view of a 60 nm MTJ. (d) the integrated multi-pillar SOT device.

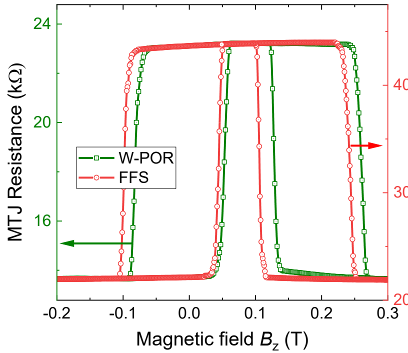


Fig. 4. Hysteresis loops of 60 nm FFS-SOT and W-POR (reference stack) devices. Bottom in-plane magnet shows low impact on FL and RL.

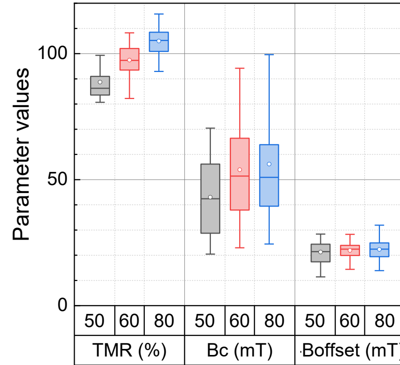


Fig. 5. Statistics of basic characterizations on FFS-SOT MTJ samples (over 100 devices/CD size). (a) TMR, (b) B_c, (c) B_{offset}.

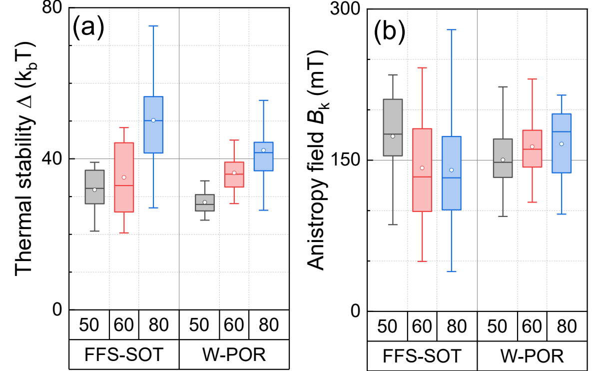


Fig. 6. Comparisons between FFS-SOT and W-POR samples. (a) thermal stability (Δ); (b) anisotropy field (B_k).

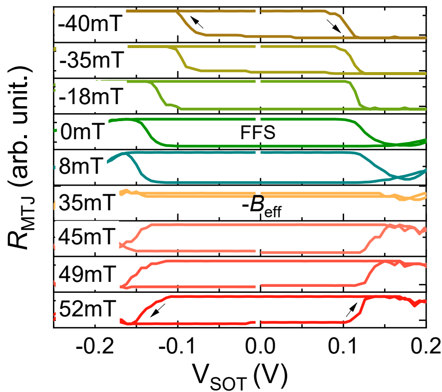


Fig. 7. Current-induced switching loops of an 80nm MTJ device for different B_x. As indicated, the full switching loop is obtained for $B_x = 0$ mT. The switching diminishes at 35 mT when B_x fully compensates the effective field.

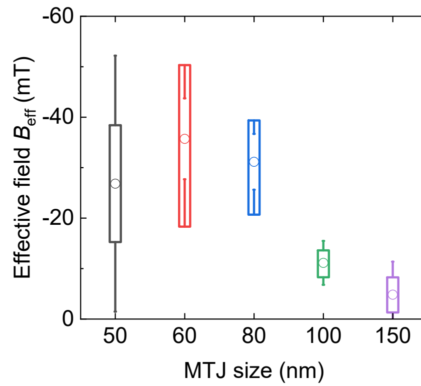


Fig. 8. Extracted effective field B_{eff} for field-free switching of MTJs with different CD sizes.

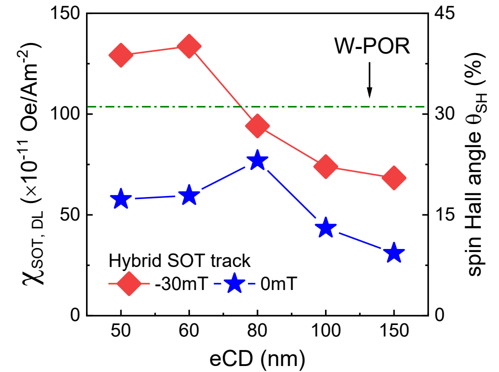
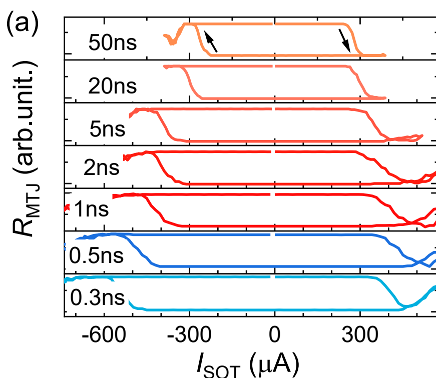
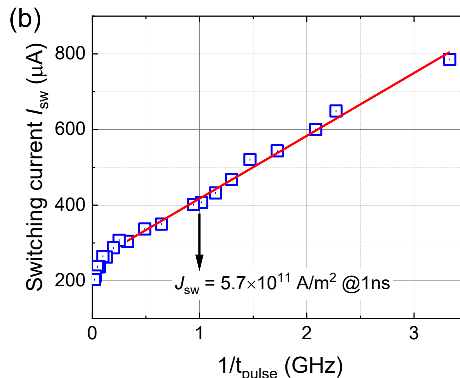


Fig. 9: Damping-like spin-orbit torque efficiency of hybrid SOT track at $B_x = 0$ and -30 mT. The green dash line shows the reference results of W-POR.





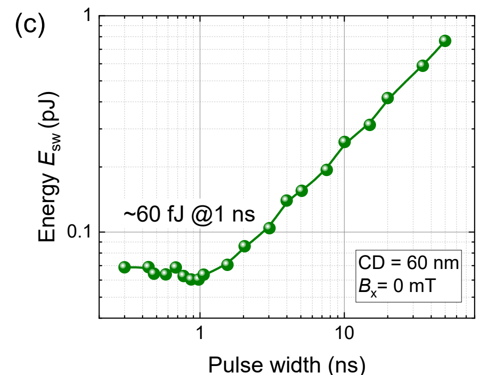


Fig. 10. Ultrafast field-free SOT switching. (a) Switching loops for different pulse widths without external magnetic field. (b) Critical switching current as a function of the inverse of pulse width. (c) switching energy as a function of pulse width. It shows the sub-ns switching and low energy consumption.

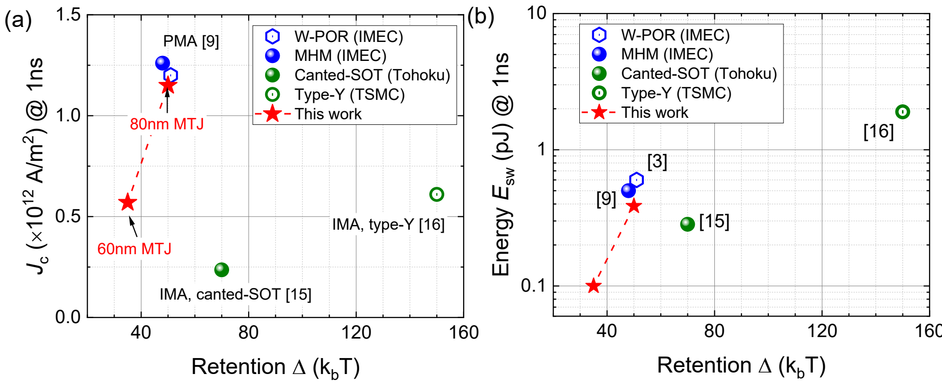


Fig. 11. (a) Switching current density and (b) energy consumption at 1ns as a function of retention (Δ) in W-POR and FFS devices. The red points show the results of 60nm and 80nm devices. The hybrid SOT track shows comparable efficiency as W-POR samples.

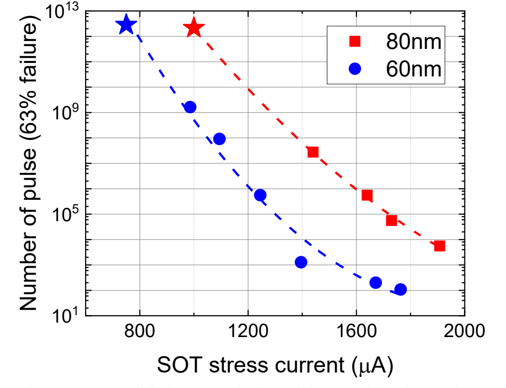


Fig. 12. 63% lifetime analysis with 1 ns bipolar pulses. 14 devices stressed at each condition. Star symbols depict lifetime at critical I_{sw} condition (at P_{sw}=50%).

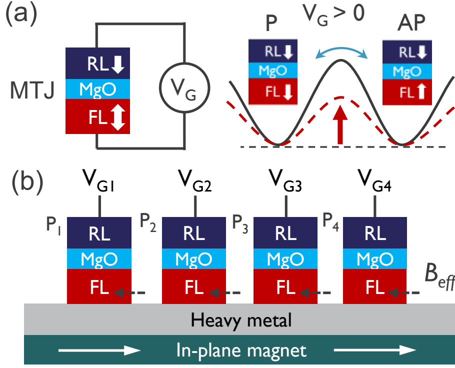


Fig. 13. Schematic of voltage controlled magnetic anisotropy (VCMA) effect and multi-pillar devices. (a) the gate voltage modulates the energy barrier for switching. (b) the hybrid SOT track enables the field-free operations on multi-pillar devices.

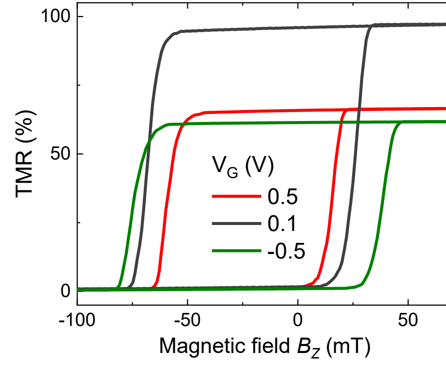


Fig. 14: Hysteresis loops of a 60nm FFS-MTJ devices for different gate voltages.

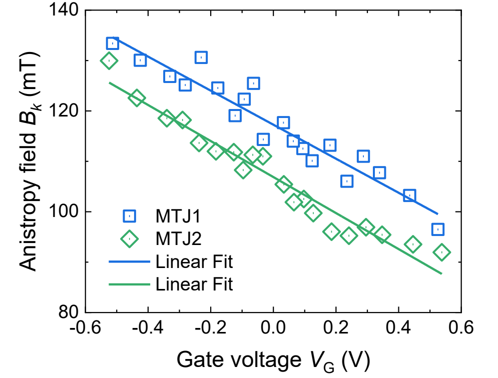
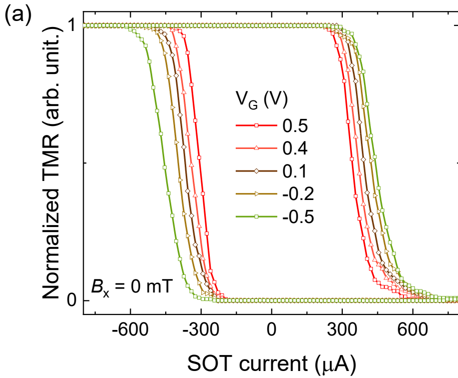


Fig. 15. Anisotropy field B_k as a function of gate voltage V_g of two 80nm FFS-MTJ devices.



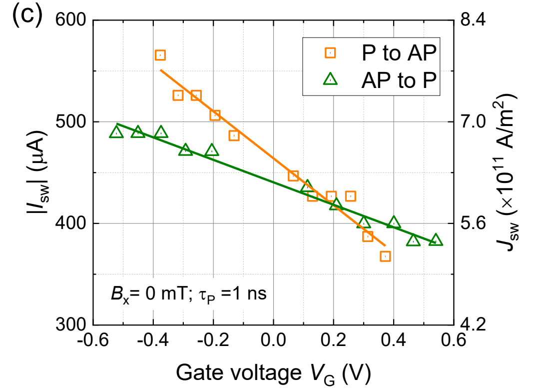


Fig. 16. Voltage-gated SOT (VG-SOT) switching. (a) Normalized switching loops for different V_G by 1ns pulses in a 60nm FFS device. (b) Switching probability P_{SW} curves for different V_G. (c) Critical switching current I_{sw} (at P_{sw} = 50%) as a function of gate voltage V_G.

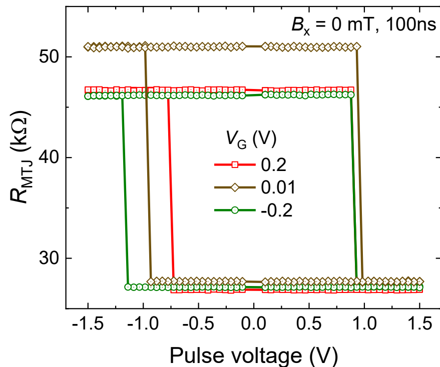


Fig. 17. A typical field-free VG-SOT switching by 100ns current pulses in one of four MTJs in multi-pillar devices.

Specification		IMEC W-POR [3]	IMEC MHM [9]	Tohoku Univ. Canted-SOT [15]	Beihang Univ. EB [8]	TSMC Type-Y [16]	**This work**
Device	Type of MTJ	PMA	PMA	IMA	PMA	IMA	PMA
	CD (nm)	60	60	88*340	700	75*230	60
	RA (Ω·μm²)	40	40	~500	~3000	10	100
	TMR (%)	110	110	167	101	140	105
	B_c (mT)	94.5	83.5	~13.5	N.A.	~20	53.7
	Δ (k_bT)	51	48	70	N.A.	152	35
	VCMA & MP compatible	N.A.	No	N.A.	N.A.	N.A.	**Yes**
Process	Annealing (°C)	300	300	400	300	400	300
	Wafer Process	300mm	300mm	300mm	N.A.	N.A.	300mm
SOT Performance	External Field (mT)	32	0	0	0	0	**0**
	J_c (MA/cm²) @1ns	120	126	23.6	170 @10ns	61	57
	Pulse width (ns)	0.21	0.30	0.35	10	0.4	0.30
	Endurance	$>5\times10^{11}$	$>10^{11}$	N.A.	$>10^{10}$	$>7\times10^{12}$	$>10^{12}$

Table 1: Benchmark table of our FFS devices with hybrid SOT track and other published field-free SOT devices.