A 134 dB Dynamic Range Noise Shaping Slope Light-to-Digital Converter for Wearable Chest PPG Applications

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***Abstract*— This paper presents a low power, high dynamic range (DR), light-to-digital converter (LDC) for wearable chest photoplethysmogram (PPG) applications. The proposed LDC utilizes a novel 2nd-order noise-shaping slope architecture, directly converting the photocurrent to a digital code. This LDC applies a high-resolution dual-slope quantizer for data conversion. An auxiliary noise shaping loop is used to shape the residual quantization noise. Moreover, a DC compensation loop is implemented to cancel the PPG signal's DC component, thus further boosting the DR. The prototype is fabricated with 0.18 µm standard CMOS and characterized experimentally. The LDC consumes 28µW per readout channel while achieving a maximum 134 dB DR. The LDC is also validated with on-body chest PPG measurement.**

***Index Terms*— Photoplethysmogram (PPG), chest PPG, light-to-digital converter (LDC), dynamic range (DR), ambient light cancellation, dual-slope, noise shaping (NS).**

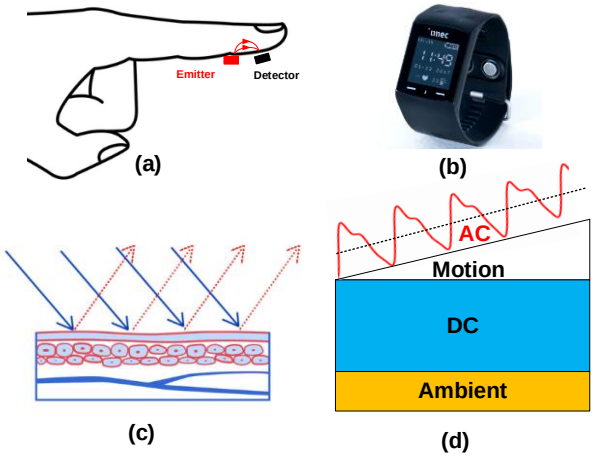

Fig. 1 (a) Reflective mode PPG on finger (b) Apple smartwatch, green PPG (c) Reflect PPG on the skin tissue (d) A typical PPG waveform.

I. Introduction

Optical photoplethysmogram (PPG) has attracted considerable consumer interest over the past decade [1][2]. Wearable devices develop very fast for health and fitness applications. People are no longer only focused on simple fitness tracking measurements such as the number of steps taken in a day. PPG-enabled wearables could monitor additional health-related parameters such as HR, HRV, blood pressure level, glucose level, and oxygen saturation (SpO_2) [3]-[5]. Various consumer electronics companies have developed and integrated PPG monitoring in smartwatches or wristbands for the consumer/fitness market (Fig. 1 (a)(b)). PPG is a diffuse optical imaging method. LED-induced light scatters inside the tissue (Fig. 1 (c)), and a small fraction of this light eventually reaches photon detectors (reflective mode) [6]. During this process, the chromophores such as oxygen hemoglobin (Hb) and de-oxygen hemoglobin (HbO_2), which vary with metabolic activity, can absorb a small portion of light. Thus, the received light contains a pulsatile component. Such an AC component represents microvascular blood volume change within each heartbeat [7]. This AC component is superimposed on a large DC component related to static tissue like bones or muscle tissue. Next to these physiological signals, the detector also receives ambient light interference (Fig.1 (d)). Moreover, motion artifacts can degrade the signal quality further [8][9]. A PPG signal obtained by single green or red light can detect heart rate by measuring the blood volume changes, while a two-channel PPG setup using different wavelengths can measure SpO_2 [10]-[15].

Besides the more conventional measuring locations such as the finger and the wrist, many studies have been conducted on obtaining additional parameters from PPG from other locations on the body [16]-[18], such as the chest. Conventionally, SpO_2 is measured with a dedicated finger clip in a clinical environment. Chest-based patches are an interesting form factor for accurate vital signs recording. Such patches usually contain electrophysiology circuitry to record ECG and potentially derive respiration from tissue impedance recording. These

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patches can provide HR, HRV, arrhythmia detection, and respiration rate information. Adding PPG could benefit many clinical settings, including critical and neonatal care, sleep assessment, and during anaesthesia [19][20]. Next to critical care, such chest patches enable long-term monitoring of respiratory diseases, especially in the patient with (chronic) pulmonary diseases such as SARS, MERS, COVID-19, or lung cancers and chronic obstructive pulmonary diseases. People who suffer from these diseases show a SpO_2 level consistently lower than 90% and fast respiration rate [21].

Unfortunately, obtaining reliable PPG recording from the chest is quite challenging [17]. Compared to the finger, the chest can be covered by thick muscle tissue, which results in a perfusion index (PI), defined as the ratio between the AC and DC components of chest PPG, of lower than 0.1 % typically. In contrast, the typical PI at the finger can range from 1% to 4% [22] since the sensor is placed closer to the distal and ulnar arteries. To record reliable HR, a common design target is to achieve at least 25 dB of SNR on AC pulsatile recording [23]. The design target goes up to >39 dB in SpO_2 monitoring [22]. However, these numbers do not include the margin required to cope with motion and respiration-related artifacts and variability in adherence, skin tones, and skin-sensor pressure [24]. So, it is good to leave another 20 dB margin for these non-idealities. Considering all these effects, the required DR is >120 dB for chest PPG recording [25]. Meanwhile, it is also essential to minimize the power consumption [26]-[27] to extend the wearables' battery life, making long-term monitoring a reality.

Meeting these stringent requirements for chest PPG monitoring calls for circuit innovation. Conventionally, a TIA-based architecture (Fig. 2(a)) is used to convert the PPG current into a voltage [28][29]. Followed by an ADC, the light current is converted into a digital code. However, to reach the resolution target, a 20-bit ADC is required [31][32]. Furthermore, the folded TIA noise caused by the pulsed LED is an obstacle [33]. To avoid such high-resolution ADC's, the large DC-component can be compensated before the analog to digital conversion [23][34]. The work illustrated in [35] demonstrated a digital-controlled TIA to control the transimpedance gain and suppress the DC components, achieving a DR of 130 dB while consuming 72 µW in the analog front-end (AFE).

However, the TIA-based architectures tend to be less power efficient compared to integrator-based PPG readouts [36][37]. The integrator can serve a double purpose as part of data conversion, leading to a simpler architecture with fewer building blocks and better noise efficiency. This concept is exploited in the direct light-to-digital converter (LDC) (Fig. 2(b)). An imager-based LDC was proposed in [38], where the photocurrent is integrated onto the PD's parasitic capacitance. Followed by a comparator, the PPG signal is converted into a data stream with a power consumption of less than 25 µW. A similar imager-based LDC reported in [39] only consumes 2.63 µW AFE power. Such imager-based PPG readouts boast impressive power numbers [38][39], but the passive integration on the imager's parasitic capacitor might lead to big non-linearity and noise, ultimately limiting the achievable DR. To improve the achievable DR with LDC-readouts, an active integrator can be used to implement higher-order noise shaping (NS) [40][41]. This work achieves 108.2 dB DR while consuming 15.7 µW AFE power. Finally, a dual-slope LDC is proposed, which shifts the accuracy requirements from the voltage to the time domain to realize a 119 dB DR and consuming 89 µW AFE power [42][43] which is again in the same ballpark as TIA-based solutions.

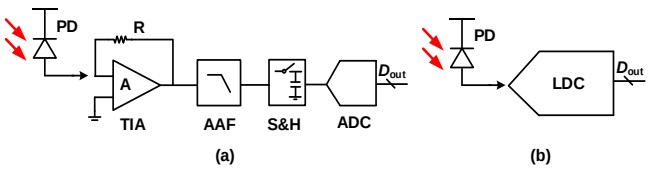

Fig. 2 (a) Conventional TIA based PPG readout (b) LDC based PPG readout.

To achieve both high DR and low AFE power consumption, a 2nd-order NS LDC is proposed. It employs a multi-bit dual-slope converter to convert the signal current to a voltage directly with high resolution. Apart from this, the converter also performs sample/hold and anti-aliasing [33][42]. The quantization residual is further processed by a 2nd-order NS loop. As a result, it significantly decreases the quantization noise while keeping the conversion time and the AFE power low [40]. The DR is further boosted by the DC compensation loop and a 7-bit IDAC. A prototype is implemented in a standard 0.18 µm CMOS technology. Measurement results show that the proposed LDC achieves a best-in-class DR of 134 dB with relatively low power consumption.

The rest of the paper is organized as follows. Section II describes the system architecture and the operating principles. Section III shows the detailed circuit implementation of the LDC. Section IV presents the noise analysis. Section V describes the electrical and in-vivo measurement results, while section VI draws the conclusion.

II. The Proposed Architecture

The working principles of the LDC are described in this section, including the system architecture and the timing diagram. Moreover, details about the dual-slope quantizer, the NS loop, and the DC compensation loop are introduced.

A. *Motivation and topology design*

Previous LDC works usually apply single data conversion

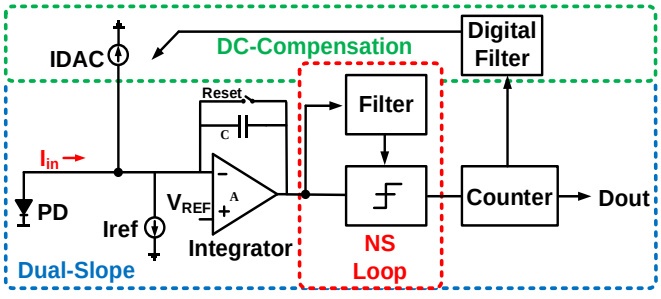

Fig. 3 The potential topology of the NS-Slope LDC and the three main parts including the dual-slope converter, the NS loop and the DC compensation loop.

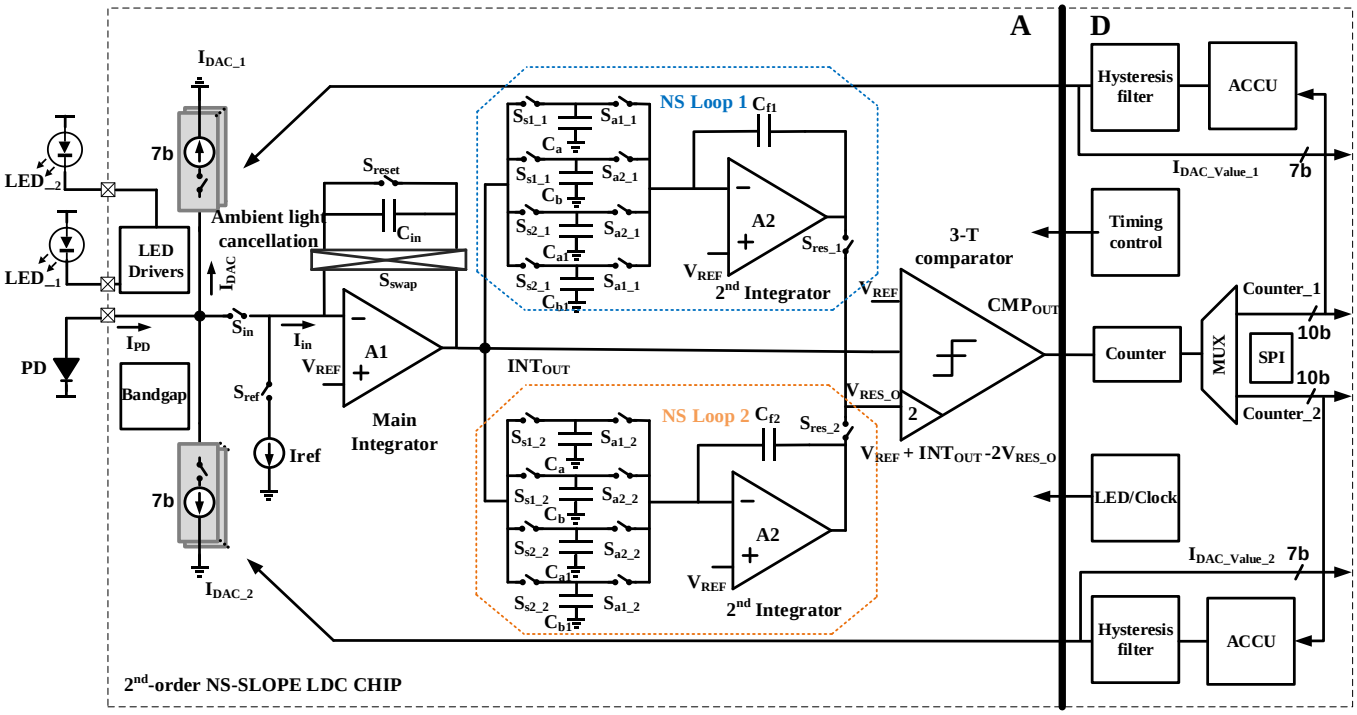

Fig. 4 Block diagram and implementation details of the LDC

strategies, e.g., ∑Δ LDC or dual-slope LDC. They do not reach the DR requirement for chest PPG monitoring and consume considerable power. Hybrid ADCs are an interesting evolution, where drawbacks of a specific ADC architecture can be compensated by integrating techniques from other ADC types, achieving excellent FOMs in certain use cases [44]. Inspired by this idea, we explored a dual-slope PPG LDC expanded with a new NS topology. The dual-slope LDC suffers from a long conversion time and high comparator power [33]. By using the noise-shaping mechanism, it is possible to achieve a lower quantization noise and decouple the internal trade-off between DR and the conversion time of the slope type ADC. In the ∑Δ type LDC architecture, the low quantization noise is usually achieved by a high OSR ratio, corresponding to high LED power [40][45]. When a dual-slope quantizer is introduced, which is a multi-bit (>8 bit), it greatly relaxes the requirement for OSR. Fig. 3 shows such a noise-shaping slope LDC (Fig. 3). The proposed topology has several benefits. First, the dual-slope ADC is used as a multi-bit quantizer, which has high resolution and linearity. Secondly, with the help of NS, which is an efficient way to decrease the quantization noise. Also, the conversion time can be reduced. This saves power at the same time. The topology is well suited for a mixed-signal DC-compensation loop as is often employed to achieve a high DR.

B. *Dual-slope converter*

Fig. 4 shows the detailed system architecture. It has three main functional blocks. The dual-slope quantizer is formed by the main integrator (A1), a 3-T comparator, a reference current (I_{ref}), and a 10-bit counter. Since the readout supports SpO_2 recording, it will be time-multiplexed to record signals corresponding to two distinct LEDs with different wavelengths. In traditional readouts, this time-multiplexing is no problem, but in our topology, we will be adding noise-shaping loops. These loops contain memory elements which make time multiplexing not possible. Hence two NS loops are designed for dual-wavelength SpO_2 extraction. Each loop consists of a capacitor bank and an integrator. The loop is closed by the 3-T comparator. Similarly, two DC compensation loops are implemented. To simplify the hardware (HW) cost, the digital filter is implemented as a threshold-based filter with hysteresis preceded. If the input signal drifts near the maximum (minimum) input range of the main integrator, $IDAC_{1,2}$ will switch to pull the input signal back into the acceptable current range avoiding saturation of the main integrator. The full range signal, which is needed to calculate SpO_2, can again be reconstructed easily in the digital domain with a simple multiply-accumulation. The proposed filtering method has a lower HW cost than a fully digital LPF and hence can easily be duplicated to support the two wavelengths.

In this LDC, a 10-bit dual-slope quantizer is used. The timing diagram and the detailed circuitry blocks are shown in Fig. 5. The LDC works with red (R) and infrared (IR) LEDs alternating at 2048 Hz. The pulse repetition frequency (PRF) can be reconfigured to be as low as 128 Hz to save power. Each dual-slope conversion starts with a reset of the main integrator A1. Then ambient light is integrated on C_{in} during a period t_1, equal to the LED pulse width (Fig. 5 (b)), but without the LED being active. Since the LED is disabled, this only captures ambient light. Right before the LED is activated, the polarity of C_{in} is swapped. The incoming current from the photodiode (PD), which now consists of the ambient light and the PPG current signal, gets integrated onto C_{in}. This effectively suppresses the ambient light since it implements a current-domain correlated-

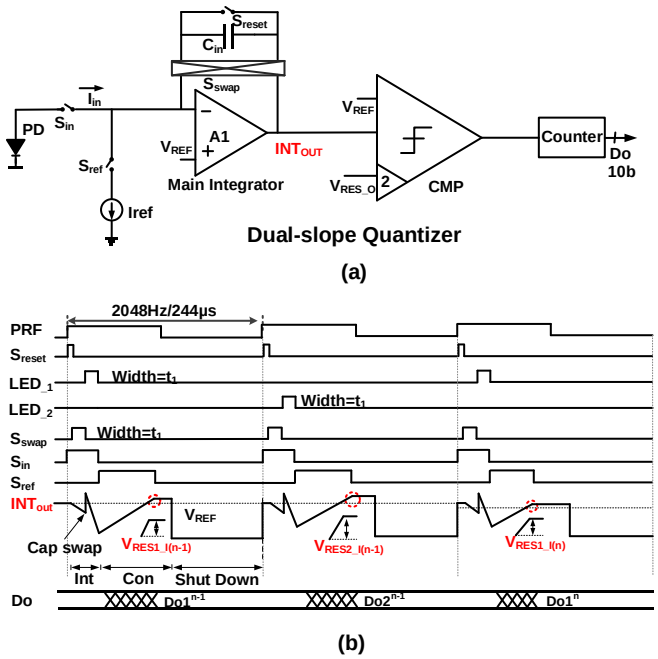

Fig. 5 (a)The detailed circuitry blocks of the dual-slope quantizer. (b) The timing diagram of the quantizer.

double-sampling (CDS) operation. Therefore, only the PPG current pulse will be integrated and sampled on C_{in}. Moreover, the pulse window integration has a sinc filter transfer function for the high-frequency noise. Assume IDAC is disabled, the voltage output can be expressed as:

$$Vo(f) = \frac{I_{in}}{C_{in}} \cdot t_1 \cdot sinc(\pi f t_1) \quad (1)$$

Since the integration time is very short, the output voltage of the integrator can be rewritten as:

$$Vo = \frac{I_{in}}{C_{in}} \cdot t_1 \quad (2)$$

After the integration phase, the current source I_{ref} is enabled to discharge C_{in} until it reaches the dynamic comparator threshold. The total discharge time is counted with a 10-bit counter operating at frequency f_{clock} up to 13.1 MHz. The input current can be expressed as:

$$I_{in} = I_{ref} \cdot \frac{D_{out}}{t_1 \cdot f_{clock}} \quad (3)$$

Thanks to the dual-slope mechanism, the 10b conversion is inherently linear. It is worth noting that the same current sink I_{ref} is used to count the charge in each conversion, and hence there is no matching requirement for I_{ref}. The I_{ref} can be calibrated on-chip. After the conversion, the quantization error is left on the integrator's output and will be sampled into the NS loop (see next section). At the end of the conversion cycle, the integrator can be powered down to save power (Fig. 5(a)).

C. *The NS loop*

To meet the chest PPG DR requirement, only a dual-slope quantizer is not enough. Thus, the NS loop is introduced. The main purpose of the NS loop is to shape the quantization noise generated from the dual-slope conversion. The proposed NS loop has four main parts: the residual sampling capacitor banks, the finite impulse response (FIR) filter, the infinite impulse response (IIR) filter, and a 3-terminal (3-T) comparator (Fig. 6 (a)).

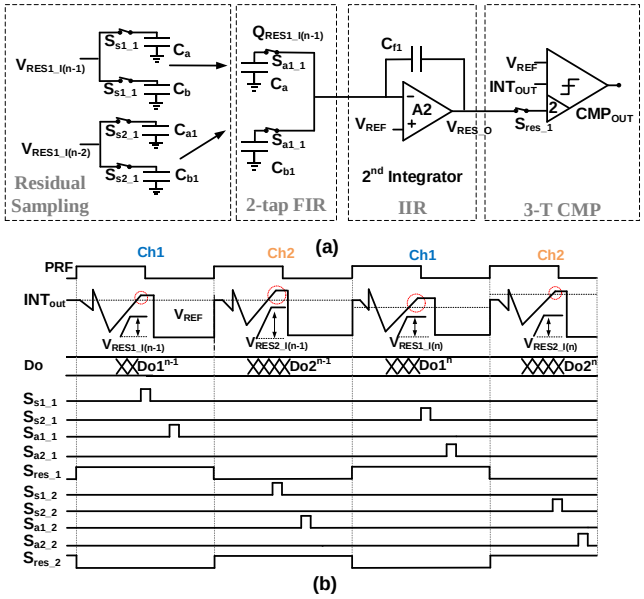

Fig. 6 (a) The detailed circuit blocks of the 2nd-order NS loop. (b) The timing diagram of the loop filter.

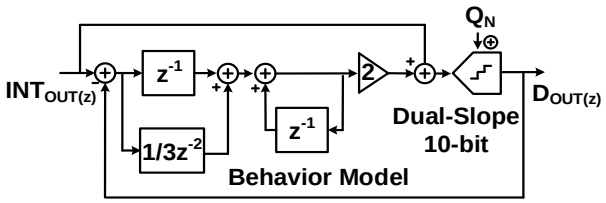

Fig. 7 The behavioral model of the 2nd-order NS Slope conversion.

Since the data conversion is a discrete-time procedure, the quantization errors of the current ($V_{RES1\_1(n-1)}$) and the previous sample period ($V_{RES1\_1(n-2)}$) are stored on the capacitor banks C_a, C_b and C_{a1}, C_{b1} respectively to build a two-tap FIR filter. Alternately summing charges on C_a, C_{b1}, and C_{a1}, C_b, the accumulated charges transfer to another integrator (IIR) to form a 2nd-order loop filter ((Fig. 6 (b)).). The ratio between the capacitor banks and the feedback capacitor of the integrator comprises the filter's coefficients. The transfer function between the residual to the 2nd integrator's output is:

$$V_{RES\_O(z)} = \left(\frac{C_a}{C_f} Z^{-1} + \frac{C_b}{C_f} Z^{-2}\right) \cdot \left(\frac{1}{1 - Z^{-1}}\right) V_{RES\_I(z)} \quad (4)$$

Where $C_a = C_f$ *(10pF)* and $C_b = 0.33 \cdot C_f$ in this design. The filtered quantization error is applied to offset the 3-T comparator, which closes the loop and determines the threshold to stop counting. A gain of 2 is incorporated into the comparator

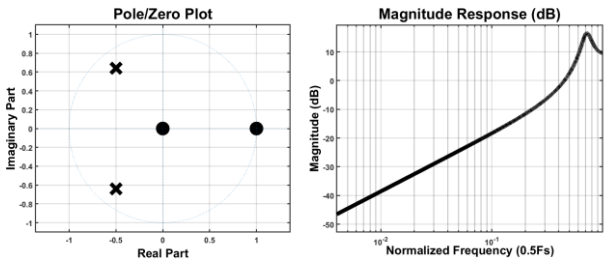

Fig. 8 (a) The pole-zero diagram of the NS transfer function. (b) The frequency response of the NS transfer function, Fs is the sampling frequency.

to achieve higher quantization noise suppression while keeping the loop stable. Thus, the transfer function of the loop filter is:

$$V_{RES\_O(z)}=(Z^{-1}+\frac{1}{3}Z^{-2})\cdot(\frac{1}{1-Z^{-1}})V_{RES\_I(z)} \quad (5)$$

Combined with the dual-slope quantizer, the behavior model of the 2nd-order NS LDC is shown in Fig. 7. As a result, together with the dual-slope operation, the entire transfer function between the input current I_{in} and the digital output Dout can be derived:

$$D_{OUT(z)}=\frac{I_{in(z)}t_1}{C_{in}}\cdot+(\frac{1-Z^{-1}}{1+Z^{-1}+\frac{2}{3}Z^{-2}})Q_{N(z)} \quad (6)$$

Where Q_N is the quantization error. From (6), there is a linear relationship between the light current and the digital output. At the same time, the quantization error is shaped to a higher frequency. The pole-zero diagram (Fig. 8 (a)) shows this transfer function is stable, and the NS frequency response (Fig. 8 (b)) presents the highpass NS behavior. It can be noted that there is an overshoot near the Nyquist frequency which means this NS LDC has a better shape when the OSR is low [46]. E.g.,

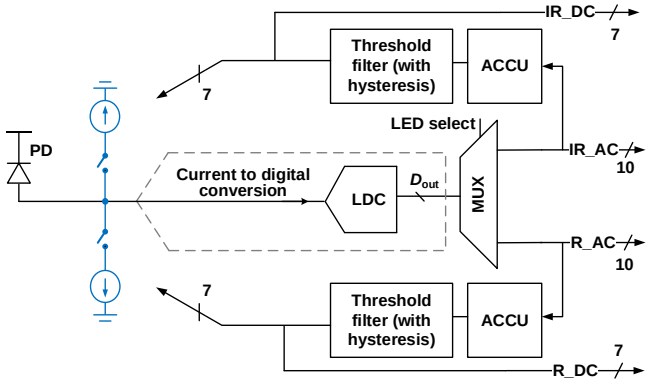

Fig. 9 DC compensation circuit building blocks.

the NS loop can have more than 38 dB quantization error suppression in signal bandwidth with an oversampling ratio of 50. This will help to ease the resolution requirement of the dual-slope quantizer [42]. The mismatch of the capacitor band is not important. A 10 % mismatch can only result in < 1 dB noise shaping suppression. However, this is also unlikely to happen. As a result, fewer counting steps are needed to achieve the same quantization noise level, significantly saving the conversion time.

D. *The DC compensation loop*

With the help of a dual-slope converter and the NS loop, the input signal current can be read with low additional noise. However, as the PPG signal contains a large DC component, it needs to be compensated before going into the converter to relax the converter requirement. This helps in obtaining a high DR without extra high-resolution ADC (>20-bit).

Two DC compensation loops are implemented to compensate for the DC components from the red light and the infrared light. The block diagram is shown in Fig. 9. The digital output is fed into the corresponding DC compensation loop using a MUX. An accumulator helps to decrease the sampling rate if the DC component is considered unchanged or drifts slowly. A digital threshold filter is then applied with internal hysteresis to regulate the digital output of the counter within the up and low thresholds, which are pre-set and slightly lower than its full range. The output of the threshold filter is truncated and used to control the 7-bit IDAC to compensate for the DC component. The IDAC is synchronized to the LED pulse. The 7-bit IDAC digital control code is recorded together with the LDC output. This way, the whole input PPG current can be reconstructed in the digital domain. If a very large DC component is induced, the IDAC can adjust by at most 8 LSB/sample to fast track the DC change.

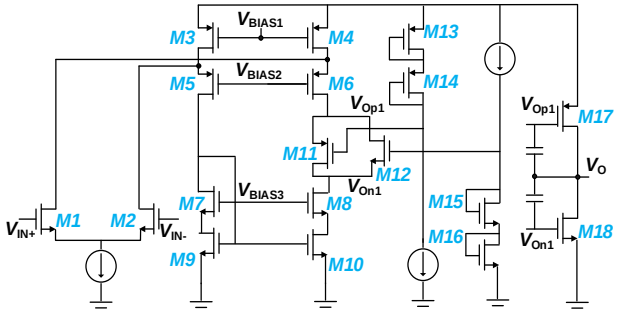

Fig. 10 Schematic of the amplifier in the main integrator with two-stages, class-ab output.

III. Circuit Implementation

The main building blocks are described in this section, including the main and the 2nd integrator, 3-T comparator, capacitor bank, and IDAC. The digital circuitry provides the control signals.

A. *The main integrator and the 2nd integrator*

Although the offset requirement of the main integrator can be eased due to the dual-slope operation, the noise and the power consumption need to be taken care of.

In this design, the amplifier is a two-stage, single-ended topology [48][50](Fig. 10). The folded-cascode input stage is used with NMOS input pairs to achieve a high DC gain, which helps to minimize the input impedance. To achieve a higher output swing, we can leverage the knowledge that the current direction is known when the anode of the PD is connected to the input. Hence the common-mode (CM) input voltage of the amplifier is set to 0.9 V instead of mid-supply. The input differential pair is biased in the subthreshold (weak inversion) region and sized sufficiently large (W/L = 200/2) to minimize flicker noise [47]. The output stage employs a class-AB topology for large current driving ability and uses miller compensation for stability [48]. M11-M6 and the output stage M17-M18 are all biased in the subthreshold region to minimize the quiescent current flow through the output stage. Take M11, M13, M14, and M17, for example, these four transistors form a trans-linear loop:

$$\frac{I_{D13}}{\frac{W_{13}}{L_{13}}}\cdot\frac{I_{D14}}{\frac{W_{14}}{L_{14}}}=\frac{I_{D11}}{\frac{W_{11}}{L_{11}}}\cdot\frac{I_{D17}}{\frac{W_{17}}{L_{17}}} \quad (7)$$

The simulation results confirm the theoretical design. The simulated DC gain of this amplifier is 81 dB with a phase margin of 65 degrees. The unity-gain bandwidth is 3.5 MHz, amplifying even a 1 µs pulse with enough settling time. The

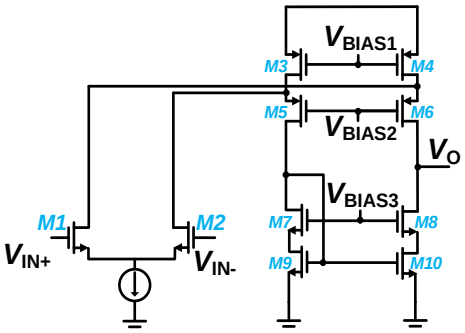

Fig. 11 Schematic of the amplifier in the 2nd integrator.

total noise within the unity-gain bandwidth is 68 µVrms. Within 20 Hz, the output noise of A1 is 2.16 µVrms. This noise can be referred to input by dividing with the transimpedance gain. Finally, a bandgap reference is also implemented to provide the bias voltages and the bias current. The integrator consumes 50 µA current at a 1.2 V supply voltage.

After the dual-slope operation (input current integration followed by the discharge phase with I_{ref}), in the NS loop, a capacitor bank is used to alternately sample the quantization noise to form an FIR filter. Then a 2nd integrator is applied to form an IIR filter to achieve a high-order NS. The quantization noise is a 10-bit level residual, which varies around the common-mode voltage. This relaxes the design requirement since both input and output swing of the 2nd integrator are low. The 2nd-integrator is only used to deal with the quantization error, operating at the sampling frequency. It applies a cascode architecture with very low current consumption (Fig. 11). The input differential pairs are again NMOS devices and the common-mode voltage is 0.9 V to align with the main integrator.

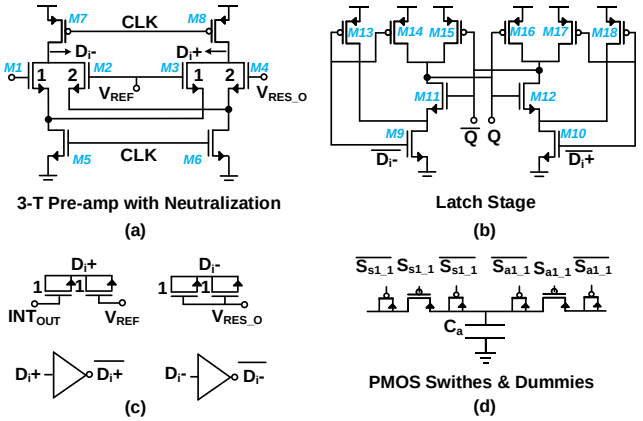

Fig. 12 (a) Schematic of the 3-T comparator pre-amplifier stage (b) 3-T comparator latch stage (c) Dummies and the inverters (d) Switches of the capacitor bank.

The simulated DC gain of this amplifier is 61 dB with a phase margin of 84▫. The unity-gain bandwidth is 350 kHz. Including the bias blocks, the total current consumption is 3 µA.

B. 3-T comparator and capacitor bank

The 3-T comparator has multiple functions. First, it needs to determine the time to stop the down integration (discharge with I_{ref}) in the dual-slope operation. Thus, one terminal of the comparator needs to connect the main integrator's output while another terminal needs to connect to the reference voltage. The comparator is also employed to close the NS loop. So, an additional terminal is needed to receive the filtered residual from the NS loop. Moreover, the filtered residual should be amplified to have a higher noise suppression ratio.

Fig. 12 (a) (b) shows the implementation of the two-stage 3-T comparator. It achieves all the functions mentioned above. M4 has double the width of M1, which realizes a gain of 2. The comparison takes place around 0.9 V, with the same DC bias. The gain mismatch between M1 and M4 is low. Still, a 50 % gain mismatch is allowed for M1 and M4. Since the filtered residual is at a 10-bit level, the kickback effect needs to be considered. Therefore, the input transistors M1 to M4 are implemented with small sizes (The size of M1 and M3 are 2.5/0.2 µm, the size of M2 and M4 are 5/0.2 µm). Also, the 3-T dynamic comparator uses a charge injection compensation method by adding cross-coupled dummy input pairs (Fig. 12 (c)), decreasing the kickback effect further. The inverters are used to reduce the kickback from the latch stages [49].

For the capacitor banks in the NS loop, the quantization error can be disturbed by charge injection during sampling or comparison. A small size PMOS switch (Fig. 12 (d)) with dummies is used to reduce this charge injection and minimize the leakage current.

C. Current reference and IDAC

In the dual-slope converter, a current reference is used to discharge the feedback capacitor C_f during the conversion. Therefore, the noise of the current reference should be minimized. A 5-bit current source is implemented for high programmability. It can provide a DC current from 50 nA to 1.6 µA. A degeneration resistor is used for each current branch to boost the output impedance of the current source. The degeneration can linearize the current reference and decrease the noise [50][51]. Although the degeneration resistor increases the voltage headroom requirement, this is not a problem for a 0.9 V CM voltage. An external load capacitor is applied to further filter out the high-frequency noise.

Two current DACs (IDACs) are employed to compensate for the large DC current. The 7-bit IDAC also applies a similar topology as the current reference. It has 128 branches controlled by a thermometer code to ensure good matching. The IDACs can provide at most 200 µA, sufficiently large to cancel the DC components. Source degeneration and filtering are also implemented to decrease the noise of IDAC.

IV. The Noise of the LDC

The main target of the LDC is to achieve high DR for chest PPG monitoring. Therefore, the noise is of paramount importance and needs to be carefully analyzed. Since the architecture is quite complicated, the first step is to find all contributing noise sources. In the dual-slope quantizer, the main integrator contributes thermal and flicker noise while the quantizer generates quantization noise. In the NS loop, sampling the quantization error can lead to additional noise. Moreover, the 2nd integrator also contributes flicker and thermal noise. In the DC compensation loop, the IDAC also generates flicker and thermal noise. All these noise sources need to be analyzed together with their appropriate transfer functions.

The noise from the amplifier, reference current, and IDAC

can be superimposed to the input current. Thus, the transfer function towards the digital output can be modeled [52]. Considering the current reference is part of the integrator, the output noise from the main integrator can be expressed as:

$$V_{nO\_INT1}^2 \cong 4kT\gamma g_m \frac{{t_{tot}}^2}{{C_{in}}^2} \cdot \left(\frac{1}{2t_{tot}} + f_k \cdot \ln(f_k) \right) + \frac{kT}{C_{in}} \quad (8)$$

Where the first term refers to the main integrator's flicker and thermal noise, the second term refers to the reset noise in each cycle [52]. t_{tot} is the total integration time for each sample, and f_k is the corner frequency of the main integrator. The reset noise can be neglected as the thermal noise of the main integrator is dominant [42]. The bandwidth of the first integrator is much higher than the sampling frequency to amplify the short pulse. The white noise parameter γ is 1. The thermal noise is hence dominant and can be derived from [42]

$$V_{nO\_INT1}^2 = \frac{kT}{C_{in}} \cdot \left(\frac{4\pi n}{D} \right) \quad (9)$$

where n (usually n > 3~10) is the number of time constants needed for settling purposes, and D is the duty-cycle ratio.

Once the IDAC is enabled, it introduces current noise as well. The major noise of the IDAC is the flicker noise since the thermal noise gets filtered by a big capacitor. Since the IDAC is synchronized with the LED pulse, the gain of the IDAC current can be regarded as a constant.

$$V_{nO\_IDAC}^2 = \left(\frac{t_1}{C_{in}} \right)^2 \cdot I_{nO\_IDAC}^2 \quad (10)$$

Where t_1 is the LED time window, again, the white noise parameter γ is 1, the first-order approximation is,

$$V_{nO\_IDAC}^2 = 4kT g_{m\_IDAC} f_{k\_IDAC} \ln(f_{k\_IDAC}) \cdot \left(\frac{t_1}{C_{in}} \right)^2 \quad (11)$$

Also, the total noise of the IDAC depends on how many current branches are enabled. The larger the input DC current, the more noise the IDAC contributes.

Another noise source is the quantization error. The LSB of the dual-slope quantizer is defined as the voltage drop within one counting step at the main integrator's output. Thus, the in-band quantization noise can be expressed as

$$V_{nO\_Q}^2 = \left(\frac{I_{ref}}{C_{in} \cdot f_{clock}} \right)^2 \frac{1}{12} \cdot \frac{1}{1+H(z)} \quad (12)$$

where f_{clock} is the comparison clock frequency, and $H_{(z)}$ is the noise transfer function shown in (5). E.g., the LDC can have more than 38 dB noise suppression at an OSR of 50, which is an efficient way to decrease the quantization noise.

The transfer functions of the noise sources in the NS loop need to be defined. The sampling noise is generated by sampling the quantization error onto the capacitor bank. It can be derived as

$$V_{nO\_S}^2 = \frac{H(z)}{1+H(z)} \cdot \frac{kT}{C_S} \quad (13)$$

The transfer function of the sampling noise to the LDC's output can be regarded as unity. Also, its value depends on the sampling capacitor size and becomes negligible for sampling capacitor values of 1 pF or larger. The sampling noise can also be used as a dither to increase the linearity of the LDC [53]. The noise contributed by the second integrator can be derived as

$$V_{nO\_INT2}^2 = \frac{2}{1+H(z)} \cdot \frac{4kT}{g_{m2}} (f_2 + f_{k2} \cdot \ln(f_{k2})) \quad (14)$$

The NS loop can shape the second integrator's thermal and flicker noise, just like the quantization noise. The gain of two is coming from the comparator. However, compared to NS, the effectiveness of the noise gain is negligible. Furthermore, the second integrator is only used to process a 10-bit level residual signal, which greatly relaxes the speed and bandwidth requirement. Thus, the second integrator can have limited bandwidth to decrease its total integrated noise. Its contribution to the output can also be optimized, saving power at the same time.

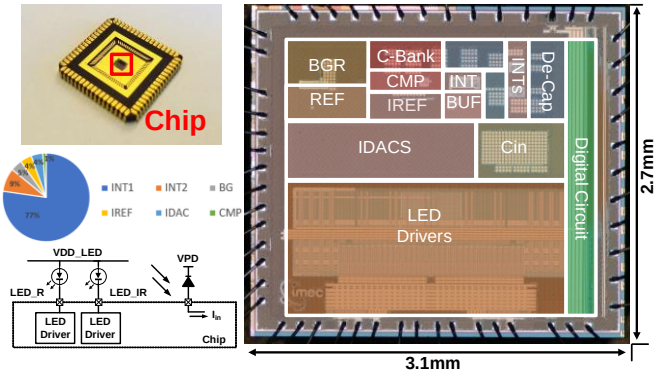

Fig. 13 Micro-diagram of the LDC, packaged chip, power breakdown and the PD connection.

In conclusion, in this NS LDC, the dominant noise sources are the main integrator's thermal noise, the flicker noise of the IDAC, and the quantization noise:

$$V_{nO}^2 \cong V_{nO\_INT1}^2 + V_{nO\_Q}^2 + V_{nO\_IDAC}^2 \quad (15)$$

The first two items do not relate to the input signal amplitude. They are the dominant noise sources if the input PPG signal DC level is low. Once a large DC component is present, the IDAC's noise starts to impact and can become the dominant noise source.

V. Measurement Results

This 2nd-order NS slope LDC has been implemented and fabricated in a standard TSMC 0.18 µm CMOS technology. Fig. 13 shows the micrograph of the prototype. The total area is 8.4 mm^2. Most of the chip area is taken by the LED drivers, which can carry peak current levels up to 100 mA. Therefore, a large area is needed for heat dissipation. All the digital control, including low-level timing, clocking, dc-offset compensation, NS loop control and LED timing are implemented on-chip. The communication protocol between the chip and the PC is a standard SPI interface. The readout IC operates from a supply voltage of 1.2 V. For chest PPG measurement, the PD/LED pairs (SFH 7060) are connected to the chip using a soft patch, ensuring good connectivity to the skin.

To characterize the electrical performance of the readout, a known current input must be applied. We used a precision signal generator that outputs a voltage, connected via a 200 kOhm resistor to the LDC, generating the input current signal while at the same time considering the correct DC-biasing. The input of the LDC gets reset to the common-mode voltage by the reset switch each cycle. Fig. 14 (a) shows the recorded output spectrum for a 1.08 µA, 4.72 Hz input sinewave current. The sampling rate for the LDC is 2048 Sps. The 2nd-order NS can be observed near the Nyquist frequency, which effectively

decreases the quantization noise. After filtering to the band-of-the-interest, which is less than 20 Hz, an SFDR of 95.96 dB and an SNDR of 86.95 dB are obtained, equivalent to an ENOB of 14 bits. The measurements confirm that the flicker noise is not dominant when the IDAC is disabled, and the main noise comes from the thermal parts of the main integrator and quantization noise. The PPG signal can even be filtered to 5 Hz for a higher SNR if needed. The main distortions are the 2nd and 3rd harmonics. The 2nd order harmonic is coming from the signal source. The mains interference is out of the band-of-the-interest and was not filtered out in the measurement results.

Using the same setup, we measured the SN(D)R for various input amplitudes (see Fig. 14(b)). As can be seen, the lowest detectable input current is around 40 pA when the IDAC is disabled. The distortion increases as the input current become higher than 1.2 µA. As a result, the SNDR decreases. However, the SNR keeps increasing for a higher input current.

When the input current signal contains a large DC component, the hysteresis filter automatically regulates the digital output code to a certain range by compensating the DC via an IDAC, which, as explained earlier, will affect the noise performance. To verify this, we enabled different levels of IDAC current and measured the corresponding noise spectrum. Seen from Fig. 14(c), when 25 µA DC input current is applied and compensated by the IDAC, the noise level increases by only 0.5 dB. Most of the noise introduced is flicker noise. When the IDAC is set to 50 µA the noise floor increases by 2.5 dB.

So, when the PPG is recorded at locations on the body like the finger or wrist, where the input current signal only contains a relatively small DC part (<30 µA), the dominant noise source is only the main integrator thermal noise and the quantization noise. If one records PPG is in a condition where a much larger DC part is present (like on the chest), higher IDAC values are needed, resulting in degraded noise performance. The total SNR saturates for DAC values of around 100 µA since then the flicker noise contributions have become too large. When enabling all the current branches, the maximum DR is extended to 134 dB, and the maximum SNR is 120 dB (Fig. 14(d)). This is sufficient to measure the chest PPG signal. The analog power consumption of each channel is 28 µW from a 1.2 V supply.

We also validated the LDC in an in-vivo setting. To this end, we embedded PD/LED pairs into a soft patch which was attached to the chest with black tape to shield ambient light. This patch was wired into our bench test setup. While this setup is not optimal for signal integrity due to the long cabling from the patch to the ASIC, it was found stable enough to do validation on human volunteers. Data were recorded with a laptop connected via USB to the bench setup.

Dual-wavelength chest PPG recordings were done on human subjects. The red LED has a wavelength of 660 nm, and the infrared LED has a wavelength of 950 nm. The duty cycle of the LED was 1 %, and the total average LED power was 0.305 mW. These values yielded good results on the test subject, but a higher LED current can, of course, be applied to compensate for various skin tones to yield a larger PPG signal. Fig. 15 (a) shows a typical measurement result. The subject was asked to hold his breath initially for roughly 50 seconds and then resume normal breathing. Fig. 15 (a) shows the full reconstructed (AC+DC part) of the recorded PPG signal. The heartbeat signal is not immediately visible in the raw PPG signal. This is expected due to the low PI index when recording PPG signals on the chest. It is also important to note that no guidance whatsoever (i.e., to guarantee the PD/LEDs are placed over a vein) was used for the placement of the patch. The patch was just put arbitrarily on the chest, which results in a typical PI of less than 0.1% for the test subject. Nevertheless, thanks to the high DR, the heartbeat signal is clearly visible after applying bandpass filtering (0.5-10 Hz), with both the systolic and diastolic peaks visible (Fig. 15 (b)). A second observation that can be made is related to motion and respiration-related artifacts. A slow drift can be observed several times larger than the actual heartbeat signal during the breath-holding period. When normal respiration resumes, a respiration-related artifact due to chest motion becomes clearly visible. Since the respiration rate is much slower than the PPG signal, the above-mentioned bandpass filter is sufficient to extract the heartbeat signal even under normal breathing conditions. The respiration rate is shown in Fig. 15(c). As expected, since both red and IR have comparable tissue attenuation levels, they show similar responses.

Fig. 16 shows the calculated SpO_2 during a controlled

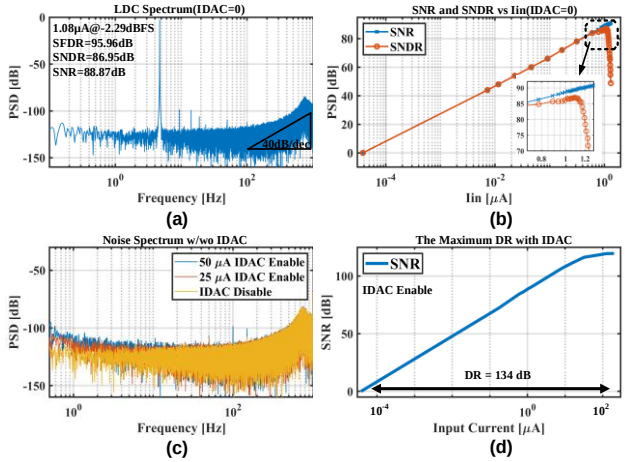

Fig. 14 (a) Output spectrum with sine current input. (b) SNR and SNDR vs Iin when IDAC is disabled. (c) Noise spectrum w/wo. (d) The maximum DR when IDAC is enabled.

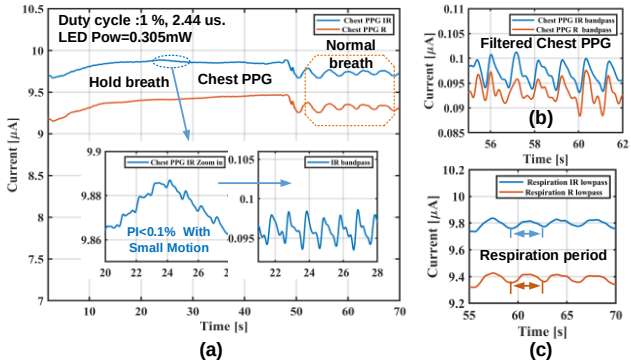

Fig. 15 (a) Dual-channel chest PPG. (b) Chest PPG with breath after bandpass filtering. (c) Chest respiration after lowpass filtering.

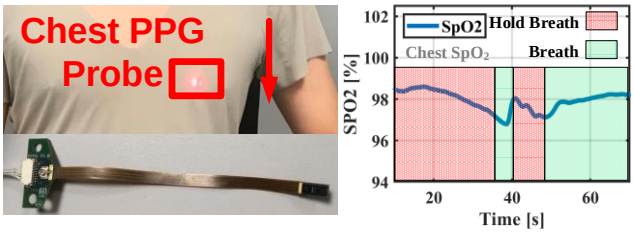

Fig. 16 Chest SpO_2 extraction in a breath-holding test.

breathing exercise. A clear SpO_2 drop can be observed when the subject was holding their breath. When resuming normal breathing, the SpO_2 level goes back to normal levels. The algorithm to extract the SpO_2 information is from [54][55].

To verify the effectiveness of the DC compensation loop and the hysteresis filter, we devised a test condition where we would force the input current to go outside the maximum range forcing the DC-compensation loop to switch the IDACs. We achieved this by forcing a much larger LED current than is strictly needed

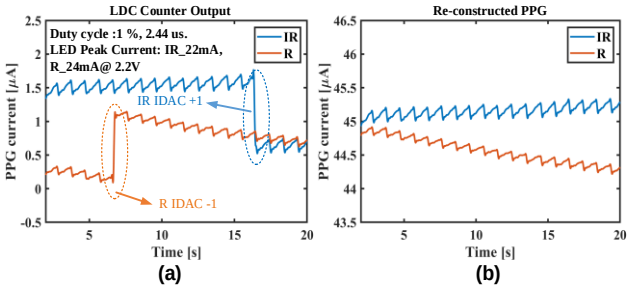

Fig. 17 (a) The LDC counter output. (b) The re-constructed PPG signal.

for this subject. Fig. 17 shows a zoom-in of the recorded signal on the time instant where the IDAC values changed. Fig.17 (a)

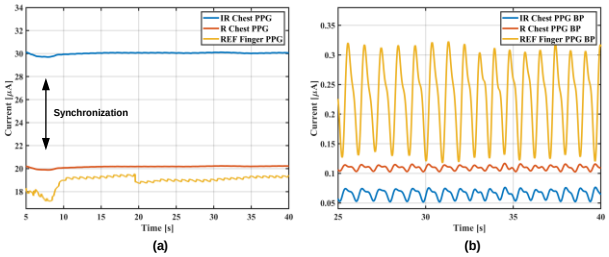

Fig. 18 (a) Dual-channel chest PPG with finger reference. (b) Filtered chest PPG with finger PPG reference.

shows the LDC counter output, while 17 (b) shows the reconstructed full-range signal. Whenever the input current drifts beyond the threshold, the DC-compensation loops will adjust the IDACs accordingly. Since the IDACs have discrete steps, this results in a noticeable step in the LDC output counter values. However, the fully reconstructed signal, which is nothing more than adding the LDC counter value to the digitally scaled IDAC control bits (Fig.17 (b)) shows a nice smooth PPG signal with no noticeable glitches or signal distortion occurring when the IDACs switch. This confirms that the DC compensation loop can cancel and quantize the DC current and boost the effective DR of the LDC. As a side note, the heartbeat signal is of course larger in these tests because of the much larger LED current applied.

In all our in-vivo measurements, we used a TI 4403 evaluation system connected to a medical grade finger-clip sensor as the ground truth [55]. Since both systems run on their own clock, the test protocol foresaw the test subject touching the LDC sensor with the finger clip sensor. This results in a noticeable artefact in both recordings which we used to align both data streams in post-processing. Fig. 18 (a) shows the

TABLE I PERFORMANCE COMPARISON

Reference	This Work	ISSCC[40]	SSCL[45]	TBCAS[42]	ISSCC[39]	JSSC[56]	ISSCC[57]	ISSCC[35]	ESSCIRC[38]
Year	2021	2020	2020	2020	2018	2021	2021	2020	2017
Technology	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	65nm	65nm	55nm	0.18μm
Supply (V)	1.2/3.3	1.5/2.5	1/2.5	1.2/3.3	1.8/3.3	0.6 [h]	1.8/1 [j]	1.8/2.8	-
Amb.Remove	50 μA	25.6 μA[c]	28.2 μA	50 μA	-	-	128 μA	200 μA	-
DC Comp	7-bit	10-bit	8-bit	8-bit	-	10-bit	7-bit	11-bit [m]	-
Max Input Range	200 μA	51.2 μA	51.2 μA	200 μA	-	-	138 μA [k]	200 μA	-
Gain Range	5k-500k	-	-	5k-4M	-	4M	-	-	-
Pulse Frequency	2048 Hz	250 Hz	100 Hz	512 Hz[e]	40 Hz	20 Hz	20 Hz	2560 Hz	160 kHz
Noise BW	0.5-20 Hz	0.5-10 Hz	0.5-10 Hz	0.5-20 Hz	20 Hz	0.55-5 Hz	-	0.5-20 Hz	0.5-10 Hz
Max DR (dB)	134 dB	108.2 dB	92.7 dB	119 dB	-	92 dB	90 dB	130 dB	-
LED Duty cycle	1%	3.2%	10.24% [d]	1%	0.07%	0.5%	0.04%	0.625%	-
LED Power	305 μW [a]	264 μW	1.95 mW	107 μW	1.97 μW [g]	8.5 μW	-	-	-
AFE Power	28 μW [b]	15.7 μW	8.1 μW	89 μW	2.63 μW	9.032 μW	24 μW	72 μW	13-25 μW [o]
Area	8.4 mm	-	4.8 mm^2	7 mm^2 [f]	20 mm^2 [p]	5 mm^2 [i]	5.5 mm^2	4.5 mm^2 [n]	1.8 mm^2 [p]
Topology	LDC (NS-Slope)	LDC (ISDM)	LDC (ISDM)	LDC (Slope)	PD+ADC	TIA+ADC	TIA+ADC	(D)TIA+ADC	LDC (1b-SDM)

[a] For Chest PPG [b] Single channel AFE power [c] 10-bit ambient light removal [d] Needs two LEDs for operation [e] From 2Hz~2048 Hz [f] External cap for filtering reference current [g] Green LED=12.04 μW Red LED=1.97 μW [h] Core supply w.o IO [i] Including other readout channels [j] Analog and digital supply [k] AC input range and DC input range [m] Not required, can be regarded as ambient cancellation [n] Including other readout channels [o] Including the LED power [p] Including On-chip PD, monolithic solution.

recordings together with the ground truth. They have different DC current levels, but after applying bandpass filtering (Fig. 18 (b)), the three PPG waveforms align well, and the systolic/diastolic peaks are clearly visible. Furthermore, they match the beat-to-beat PPG cycle very well, which confirms the proposed LDC is very reliable for PPG monitoring.

Table I summarizes the performance of the proposed LDC and compares it with recently published PPG readout circuits. The LDC achieves a maximum DR of 134 dB, which is more than two times (4 dB) higher than the state-of-the-art. Meanwhile, a low AFE power consumption of 28 µW is reported.

VI. Conclusion

This paper presents a sub-mW LDC for chest PPG applications. The proposed readout architecture achieves the highest DR at a low AFE power consumption, and it can measure HR, SpO_2, and respiration. The LDC has been validated with a chest PPG measurement compared to a reference system. Therefore, this PPG chip opens opportunities for developing compact, power-efficient, and high-performance medical chest patches for long-term monitoring of vital signs in patients with COVID-19 or other lung diseases.

VII. Acknowledgement

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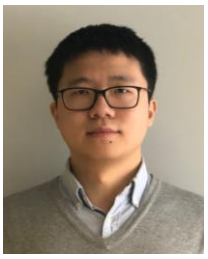

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