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Challenges in introducing high-density interconnect technology in printed circuit boards for space applications

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Abstract
Despite its introduction over three decades ago, designing, manufacturing and testing of high-density interconnect (HDI) printed circuit boards (PCBs) remains a topic of discussion. A plethora of advanced manufacturing processes is used to realize HDI PCBs in general and microvias in particular. The introduction of HDI technology for space applications and the pursuit for qualification by the European Space Agency create the need for a critical review of existing test methods. Two categories of HDI technology are considered: two levels of staggered microvias (basic HDI) and three levels of semi-stacked microvias (complex HDI). Several challenges were encountered during the design, testing and evaluation of the basic HDI technology. The main issues were related to the positioning of the microvias with respect to the core via, interconnection stress testing (IST) coupon design, microvia failures and core via performance. ESA has gained significant heritage with interconnection stress testing. IST parameters for mechanical vias and microvias are defined in the current European Cooperation for Space Standardization (ECSS) standard for PCBs. Especially for microvias, recent experiences with failures have led to a revision of the test method. Alternatives microvia test methods as convection reflow assembly simulation and current-induced thermal cycling (CITC) are explored in this study. A thorough understanding of the impact of design variables, manufacturing processes and test parameters is vital for meaningful microvia testing.

Introduction

Two main drivers are commonly identified for high-density interconnect (HDI) printed circuit boards (PCBs): (1) the small pitch and high number of I/Os of key components and (2) the increasing performance of these components resulting in high-speed signal lines on the boards. The use of microvias allows to reduce the length of the signal path, improving both signal integrity and power integrity. Critical nets may suffer from crosstalk due to the dense routing within the fan-out. The routing of differential pairs in between the pins of a 1.0 mm pitch component requires fine line widths and spacing. Differential pair routing in between the core vias for 0.8 mm pitch components is no longer possible. The pairs need to be split within the fan-out area and the effect on signal integrity will depend on the length of the split. The change in width on single-ended nets, as well as a change in the spacing and/or trace widths of a differential pair will cause an impedance discontinuity. Choosing the appropriate layer build-up and via types will thus improve both route-ability and signal integrity. Insulation is an important factor for satellite design in general and electronic equipment in particular [1]. HDI technology inherently pushes the limits of the insulation principles, requiring continuous concessions between design and reliability.

An important consideration in the definition of technology parameters for HDI PCBs is that component pitch and the number of I/Os cannot be addressed independently. A high pin count component (> 1000 pins) with 1.0 mm pitch can require the use of microvias to reduce the total layer count or to improve the shielding of controlled impedance lines. On the other hand, the escape routing of a 0.5 mm pitch component with only two rows of solder balls can be performed without microvias and fine line widths and spacing. Increasing the layer count to be able to route one or more high pin count components will result in an increase in PCB thickness, which impacts the minimum via drill diameter through limitations on the via aspect ratio and thus again restricts routing possibilities.

Increasing the capability for dense routing, signal integrity at high speeds and a high number of I/Os undoubtedly has its impact on reliability. Reducing line width and spacing, via pad size and drill diameters all influence the manufacturing yield and quality and thus present a reliability risk. New materials need to be introduced to corroborate the increasing capability demands without diminishing the reliability standards.

High-density interconnect PCBs have been used for over three decades and are currently applied in all markets. Numerous studies on HDI technology and its reliability have been executed [2, 3, and 4]. The returning theme in almost all HDI technology studies is that the technology can be very reliable, if manufactured properly [3]. Process control and quality assurance are key to reliable HDI PCBs.

A plethora of advanced manufacturing processes is used to realize microvias, each contributing to the quality and thus reliability of the microvia: mechanical or laser drilling (UV, UV-CO2 or CO2 direct), pre-etch and pre-cleaning, plasma and/or wet desmear, micro-etch, electroless copper plating, galvanic flash plating, copper via filling, etc. All of these processes consist of multiple process steps, each with their own set of parameters and possible failure mechanisms. These variables emphasize the challenge of manufacturing the perfect microvia. Besides the manufacturing processes, the reliability of microvia technology is also affected by their design, such as aspect ratio, drill diameter (aperture), the dielectric layer uniformity, the style of glass weave, the copper distribution and the distance to adjacent microvias and core vias, via density and pitch, among other things.

This paper provides an overview of the ongoing ESA activity on high-density PCB assemblies, led by imec with the aid of ACB and Thales Alenia Space in Belgium. The goal of the project is to design, evaluate and qualify HDI PCBs that are capable of providing a platform for assembly and the routing of small pitch AAD for space projects.

HDI technology parameters

Table 1 - HDI technology parameters for basic and complex HDI technology

Technology parameter	basic HDI	complex HDI
Conductor width and spacing, as-designed	75 µm line width and 75 µm spacing on non-plated inner layers (17 µm Cu foil); 120 µm line width and 100 µm spacing on plated inner layers (12 µm Cu foil with plating).	50 µm line width and 50 µm spacing on non-plated inner layers (12 µm Cu foil); 75 µm line width and 75 µm spacing on plated inner layers (12 µm Cu foil with plating).
Configuration of microvias	Two levels of microvias, staggered, Cu filled, 175 µm diameter as-designed.	Three levels of microvias, Cu filled, 125 µm diameter as-designed. Semi-stacked inside configuration.
Number of layers	≤ 20	≤ 26
Construction of HDI layers	Staggered to core, two sheets of prepreg.	Staggered to core, one sheet of prepreg.
Aspect ratio of core vias	≤ 8	≤ 10
PCB thickness	2.8 mm	Approx. 3 mm
Filling medium for core vias	Prepreg resin (from HDI layers)	Via plugging (with cap plating)
Construction of core	Single sequence, 300 µm drill diameter and 600 µm pad diameter for core vias.	Single sequence, 250 µm drill diameter and 550 µm pad diameter for core vias.
Back drilling	No	Back drilling on core
Presence of non-functional pads	As per ECSS-Q-ST-70-12C [8]	Full pad stack removed on core vias
Dielectric material	Polyimide (Ventec VT-901)	Polyimide (Ventec VT-901)
RF material	No	Panasonic Megtron 6
Surface finish and solder mask	SnPb, no solder mask	ENIG or ENEPIG with solder mask

Based on the feedback of European prime satellite contractors, equipment manufacturers, space agencies, ESA qualified PCB manufacturers and ESA technical officers, a set of HDI technology parameters was defined in 2018 (Table 1). It was decided to differentiate between "*basic HDI technology"*, intended for immediate qualification, and "*complex HDI technology"*, covering more advanced technology parameters. The basic HDI technology parameters cover the short-term need for increased functionality at an acceptable manufacturing risk level, without compromising reliability. Large FPGA components, based on 1.0 mm pitch CCGA packages with up to 1752 pins, are the primary drivers for the basic HDI technology. In addition, area array devices (AAD) with 0.8 mm pitch and a few hundred I/Os should be compatible with the basic HDI technology. Other driving components are small passives (0402 chip components) and fine-pitch lead frame components (QFP 0.5 mm) when routing space is limited. Polyimide remains the material of choice for HDI PCBs in space applications, in a single-sequence core construction with two levels of copper-filled microvias. Two levels of microvias is considered sufficient to route the AADs

with 0.8 mm and 1.0 mm pitch, covering the functional requirements in the foreseeable future. To minimize the reliability risk, the microvias are staggered with respect to each other and to the buried via in the core. Filling of core vias with prepreg resin from the HDI layers is initially preferred as it involves fewer materials and processes and is close to the qualified sequential lamination technology. Two sheets of prepreg are to be applied on all layers.

In future projects, components will have up to 2000 to 3000 I/Os and will use AADs with 0.8 mm and 1.0 mm pitch. These will likely be non-hermetic polymer-based packages (PBGA), as a package size of 45 mm x 45 mm for ceramic packages is the limit in terms of CTE mismatch [5]. A further reduction in pitch to 0.5 mm pitch is expected for low I/O (200 – 300) and for memory devices. The increased number of I/Os and reduced pitch translate into the need for three levels of microvias in the complex HDI technology. The microvia configuration of choice is the semi-stacked option consisting of two stacked microvias plus one staggered microvia. Stacking three levels of microvias is considered a reliability risk. Via plugging and capping will be used for the core vias in the complex HDI technology. The effect on reliability of removing the non-functional pads and back-drilling of the core vias will be investigated as part of the upcoming complex HDI technology evaluation.

To accommodate the need for RF and high-speed digital applications, Panasonic Megtron 6 is included in the complex HDI technology evaluation. Low in-plane CTE materials are currently not seen as a priority for HDI in future projects. The use of a single sheet of prepreg for the microvia layers will be evaluated.

Solder mask is a requirement for the complex HDI technology. Other surface finishes (ENIG, ENIPIG, ENEPIG, and EPIG) are of interest, but the focus of this study is not to evaluate alternative surface finishes. The complex HDI technology will be evaluated with both ENIG and ENEPIG (one finish per base material). A surface finish without Ni has benefits with respect to RF performance and avoids the creation of more brittle Ni-Sn intermetallic [6]. Ni-free options are either still rare (EPIG, ISIG) or not compatible with the fine spacing and planarity requirements of HDI components (reflowed SnPb). Electroless Nickel Immersion Gold (ENIG) is considered more suitable for large AAD components, while adding an additional electroless palladium layer makes the ENEPIG finish suitable for wirebonding [7].

HDI technology qualification

To support the needs of current space projects, a formal qualification of the basic HDI technology is targeted. A qualification test vehicle (QTV) is subjected to the qualification test flow for HDI technology as defined in ECSS-Q-ST-70-60C [9]. Group 1 (*visual inspection and non-destructive test*) consists of visual inspection, dimensional verification, impedance test, cleanliness and electrical testing. Peel testing is performed in group 2 (*miscellaneous testing*) and group 3 (*thermal stress*) covers microsectioning before and after solder bath float and rework simulation, and interconnection stress testing (IST). Group 4 (*assembly and life test*) combines reflow simulation, rework simulation and thermal cycling. Electrochemical migration (ECM) testing is part of group 5.

Within the ECSS-Q-ST-70-60C standard, IST is an important test method to evaluate the quality of a via (PTH, blind, core and microvia). The test method is applied for process monitoring, procurement and qualification. IST is a form of current-induced thermal cycling and is described in IPC-TM-650-2.6.26A (Method A). The coupon is heated using a power circuit and the resistance of the structures under test is monitored continuously via the sense circuit(s) of the coupon. The coupon design should represent the PCB technology of highest complexity and cover all aspects of a given design or technology that are expected to affect thermal endurance.

The reference test method for evaluating thermal reliability of HDI PCBs remains thermal cycling. This is performed in a single chamber system at ambient pressure. The test samples are subjected to reflow simulation and rework simulation prior to thermal cycling at test conditions generally representative for ESA missions.

Because of the reduced insulation distances, HDI technology is more susceptible to electrochemical migration. This is assessed through THB and CAF testing. To assess the CAF performance of a given HDI PCB technology, an HDI CAF test vehicle has been employed that resembles the final product as much as possible (build-up, via configuration, routing…).

Three panels were randomly selected from the qualification test vehicle manufacturing batch and subjected to the tests described above. Each panel contains three IST coupons (one TVX and two SLX coupons), two BGA coupons and two times the dedicated test structures for HDI qualification test flow (coupons A/B, Bn, E, H and P). For CAF testing, 10 samples of the HDI CAF test vehicle were manufactured on dedicated panels. All manufacturing was performed by ACB (Dendermonde, Belgium).

The BGA coupon (Figure 1) mimics (part of) an actual HDI PCB design and acts as “PCB” for the qualification test flow. The real component fan-out for 1.0 mm and 0.8 mm pitch components are based on the actual pin-out diagrams for the Xilinx Virtex 5QV FPGA and the Teledyne e2v EV12AQ600 ADC, respectively. Controlled impedance differential pair routing was applied

to all relevant output pins. As high-density connectors can impose restriction on routing and are thus also driving components for HDI, two candidates are included in the BGA coupon. The differential pair interconnections of the Xilinx Virtex 5QV FPGA component fan-out are routed to eight KVPX connectors. The fan-out of the Teledyne e2v EV12AQ600 is combined with the Axon nano-D connector.

Details about the test vehicles, test methods and test results for the HDI qualification can be found in [10]. Microvia failures were observed during IST. Cracks in the core vias were detected after thermal cycling testing in both the 0.8 mm and 1.0 mm pitch fanout. No non-conformance were observed related to the through-going vias. The failures and the most important lessons learnt from the basic HDI technology qualification are further discussed in the next section.

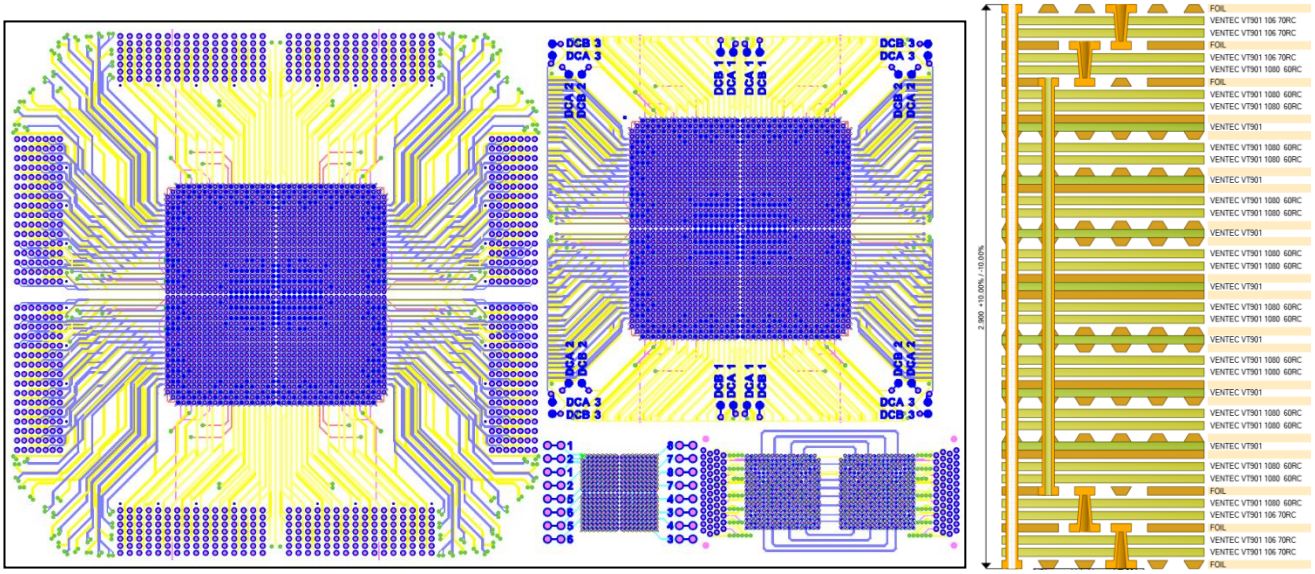

Figure 1 - BGA coupon with real and daisy-chain component fan-out for 1.0 mm and 0.8 mm pitch component *(left)* **and build-up of the qualification test vehicle** *(right)*

Challenges encountered in HDI technology qualification

Several challenges were encountered during the design, testing and evaluation of the basic HDI technology. The main issues were related to the positioning of the microvias, IST coupon design, microvia failures and core via performance.

Two levels of staggered microvias can be implemented in different ways. The design rule for the staggered microvias in the basic HDI technology is tangency of the pads. This is implemented to assure that the two microvias do not overlap after manufacturing. The lower microvia shall also be designed tangent to the core via for the same reason. Stacking of microvias on top of the core via or on top of each other is considered an unnecessary reliability risk for the basic HDI technology. Despite the stringent design rules, there is still a lot of design freedom in where to position the microvias with respect to the core vias. The location of the outer microvia in particular has an impact on the stress levels it is exposed to, as will be illustrated hereafter.

In the design of the BGA coupon, two different approaches for positioning the microvias are integrated (Figure 2). For the 1.0 mm pitch fan-out, both microvias are placed completely next to the core via. Due to the limited space, this approach was not possible for the 0.8 mm pitch fan-out. As a consequence, the outer microvia is partially superimposed to the core via.

The hierarchy of failure for the basic HDI technology is the resin-filled core via before the through-going via, despite the longer barrel of the latter. This is related to the higher CTE of the pure resin inside the core via. The performance of the core via will also depend on the pitch of the via, meaning different coupon designs are required for 0.8 mm and 1.0 mm pitch. No planarization of the core vias is performed for the basic HDI technology, so the coupon design does not need to focus on the knee crack failure mode. Five coupon designs are needed to cover the basic HDI technology. Besides a dedicated coupon for the through-going vias (“TVX”), four different sequential lamination (“SLX”) coupons are designed. All the SLX coupons contain core vias combined with staggered microvias and differ only in pitch of the core vias and the configuration of the sensing circuitry. The location of the microvias with respect to the core vias is copied from the real component fan-out in the QTV. Similarly, the dimensions of the PTHs and the grid size of the TVX coupon are based on the high-density connector layout of the QTV.

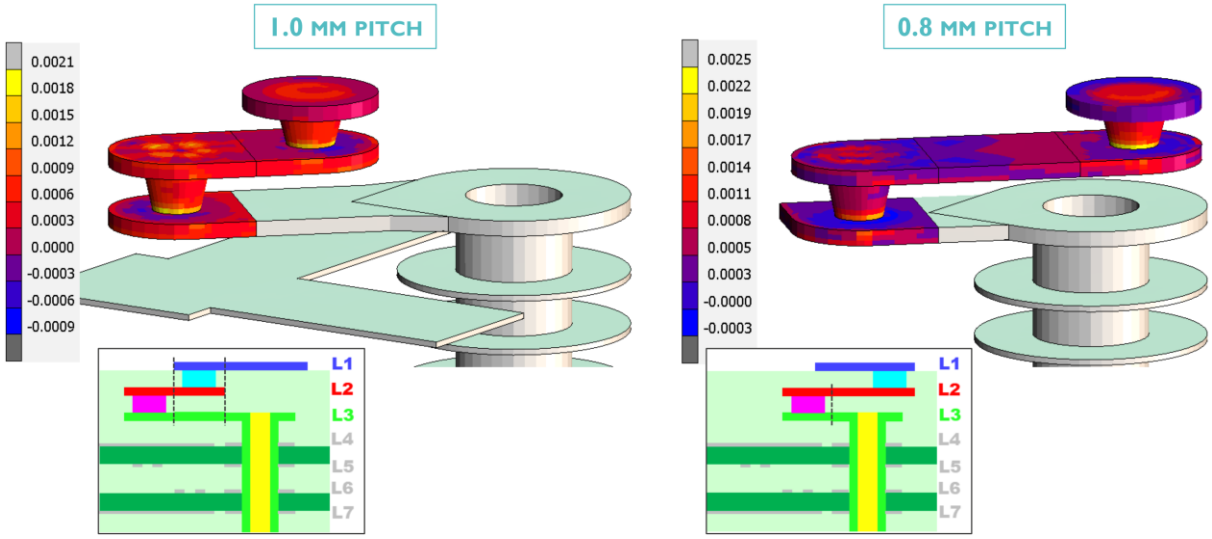

Figure 2. Positioning of the microvias with respect to the core via on the qualification test vehicle (1.0 mm pitch with both microvias off-set to the core via *(left)* and 0.8 mm pitch with the external microvia partially superimposed to the core via *(right)*)

Due to the limitation in available panel space, only two IST coupon designs are included on the panel to cover the most critical design features of the BGA coupon. The reasoning was that if the most critical features pass the test (i.e. the core vias and microvias at 0.8 mm pitch), the less critical features at 1.0 mm pitch would also pass. Based on the experience during testing [10], it is advised to include IST coupons for all design variations on a qualification test vehicle. This aids in understanding the failure mode and allows to differentiate between what design aspects influence the test result.

Acceptability of PCBs in general, and thus also for HDI PCBs, is determined after manufacturing based on the inspection of dedicated test coupons placed on the periphery of the panel. Due to the mixture of high-density features with areas of lower density, the location on an HDI PCB panel becomes more critical. The location can have an impact on critical features such as dielectric thickness and copper plating thickness. While both standard and HDI PCB technology can have variations in high and low density copper and drilling patterns, the narrow tolerances of HDI technology make this effect more precarious (e.g. dielectric thickness for microvia layers). During qualification testing, differences between values measured on coupons and in the actual PCB were observed. These could be explained by the discrepancy between the high-density features on the PCB and low density surrounding the coupon. This translates into a risk of accepting a PCB based on values that are not representative for the actual PCB. To minimize this risk, the design of the inspection coupon should be as representative as possible for the actual PCB.

PCBs for space applications are traditionally manufactured using polyimide as base material. The main advantage of a polyimide resin system is the high glass transition temperature (Tg), which is typically around 250 °C. This is above the SnPb reflow temperature of 230 °C, meaning very little damage is introduced when the PCB is submitted to assembly cycles and possible rework and repair. Alternative materials, such as high-Tg epoxy resin systems have a lower Tg compared to polyimide (160 – 180 °C). While the coefficient of thermal expansion in Z-direction (CTE_z) for these materials increases significantly above Tg, the CTE_z below Tg is often much lower than for polyimide resins system. HDI PCBs use thin laminate and prepreg layers in their construction, which are provided with relatively high overall resin content (volume ratio of resin to glass fiber). Regardless of the resin system, HDI constructions exhibit a higher thermal expansion in Z-direction due to the use of thin glass fiber styles such as 106 or 1080 [11]. For unfilled polyimide resin systems, the impact of switching to a high-resin content HDI construction on the overall CTEz is observed to be significant. Figure 3 shows a TMA measurement of the basic HDI construction using a polyimide resin system. While the Tg is estimated to be around 235 °C, the CTE_z below Tg is measured to be in excess of 120 ppm/°C (datasheet value of 50 ppm/°C). Finally, polyimide resin can suffer from embrittlement after the multiple laminations required for an HDI PCB construction.

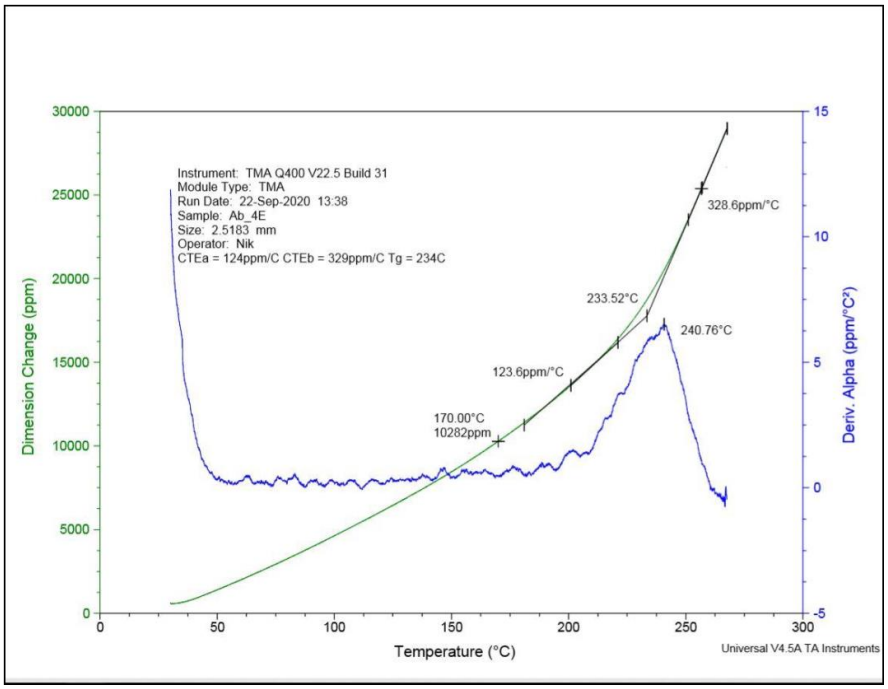

Figure 3. TMA measurement of the basic HDI construction using a polyimide resin system

The high thermal expansion of the (pure) polyimide resin has another implication for HDI PCBs. Filling of the core vias can be performed in different ways. Using the resin from the prepregs during the lamination of the first microvia layers offers a straightforward manufacturing solution. The drawback is that it is more difficult to control the dielectric thickness of the microvia layers. In addition, the pure resin, no longer restraint by the glass fibers, expands in all directions equally resulting in high stress concentrations along the via barrel. Filling the core vias using a dedicated plugging paste, followed by a cap plating process, is more complex from a manufacturing process, but offers better dielectric thickness control and a wider selection of filling medium with suitable thermomechanical properties. Resin systems with lower CTE_z are often not suitable for filling core vias due to insufficient flow and thus always require via plugging.

Around the start of the qualification testing, the Global Association for Electronics Manufacturing (IPC) issued a worldwide electronic industry warning on PCB microvia reliability for high performance products [12]. Field failures in stacked microvias were observed at large Original Equipment Manufacturers (OEMs), which seemed to be related to weak interfaces at or near the microvia target pad. In addition, latent microvia failures were encountered in the frame of ESA projects. Obviously, this had a big impact on the ongoing qualification. The ECSS test methods for IST of microvias were reviewed and revised based on new findings [13]. In addition, manufacturing processes were reviewed [14] and alternative microvia test methods were explored [15].

The present activity has achieved a significant step towards qualification of basic HDI technology, as almost all elements of the test campaign were meeting the acceptance criteria [10]. During the test campaign, a concern arose for the core vias that appeared to show microcracks in the barrel after thermal stress. This is subject of a comprehensive design of experiments to investigate root cause, define corrective actions, and investigate detailed new acceptance criteria at end of test. A repetition of this test campaign is ongoing with a view to polish away this final hurdle.

Complex HDI technology evaluation

The complex HDI technology introduces several new features, such as three levels of microvias, via plugging, cap plating, back drilling, solder mask and alternative surface finishes. Manufacturing risks and new failure modes are associated with each of these features. The goal of the evaluation test campaign is to assess the performance of these features. This may lead to formal qualification for all or a subset of the technology features, depending on the occurrence of nonconformance in the evaluation. The test methodology aims at decoupling the risks associated with these features as much as possible. This not only increases the overall chance of success, but also allows achieving qualifications status where successful. The overall test plan does not deviate significantly from the test flow specified in ECSS-Q-ST-70-60C [9].

Three levels of microvias can be implemented in different ways. Staggering all microvias ("*full staggered*") is known to have the best reliability, while stacking all the microvias ("*full stacked*") offers the highest design flexibility. As a compromise, two levels of stacked microvias can be combined with one level of staggered microvias ("*semi-stacked*"). Full stacked microvias will not be used for the complex HDI technology. Full staggered is considered a safe backup option. The microvia configuration of choice is the semi-stacked option.

Removing non-functional pads is a common practice in the PCB industry, even for high-reliability products. At the design stage, removing the pads can free up space for routing (if the design rules allow). Without the pads, the capacitance of the via is reduced and thus the signal integrity is improved. PCB manufacturers remove the non-functional pads during data processing to reduce drill wear and improve the yield of the PCB. The influence of removing non-functional pads on the reliability of the via is an ongoing debate. An important remark in this discussion is that the influence of non-functional pads is secondary to other design parameters (aspect ratio, material properties) and certainly to the quality of the interconnect (plating thickness and absence of defects).

Back drilling or controlled depth drilling is applied to remove unwanted via stubs in order to improve signal quality. Accurately controlling the drilling depth across the entire panel is a challenge for the PCB manufacturer. The diameter of the back drilling is determined by the dimensional stability of the core and the alignment tolerance of the drilling process. The latter is influenced by the fact that when the back drilling is performed from the bottom side of the board, the panel needs to be flipped compared to standard drilling. For the complex HDI technology, back drilling is only evaluated on the buried vias. The buried vias are back drilled before the via plugging, so both the remaining part of the buried via as the back-drilled part are filled with epoxy paste.

The complex HDI technology evaluation is ongoing and will be published elsewhere.

Microvia testing

Microvia technology has been used in production since the 1990s. In the beginning, the design freedom for HDI PCBs was only limited by the imagination of the designer, resulting in some very ambitions construction. It became apparent quickly that there are limitations on how many microvias one can stack on top of each other and where to place them with respect to the core via. In 2011, MSI Applied Technology observed in-house and fielded product failures related to stacked microvias and subsequently mandated all new designs require staggered microvia chains [16]. As similar microvia issues started popping up in other places, IPC released an *Industry Warning on Printed Board Microvia Reliability for High Performance Products* [12]. In addition, unexpected late microvia failure in IST has been recently reported [13]. All these failures resulted in a renewed interest in microvia testing.

In HDI PCBs, interconnection failures can occur at through-going vias, at the core vias or at the microvias. Focusing on the core vias and the microvias, the core via is expected to fail before the microvia. If a microvia is manufactured properly, it is not expected to fail during thermal cycling, as it does not show a fatigue failure mode. When failures do occur, these are typically related to relatively early and abrupt separation of the microvia from the target pad [17]. In case of staggered, copper-filled microvias, the internal microvia typically outperforms the external microvia, with the dominant failure mode being target pad separation. Resin-filled microvias may exhibit multiple failure modes (barrel crack, knee crack), and are therefore considered less reliable. Stacking of microvias leads to additional failure modes since the stacked microvias form a tall structure that results in increased levels of thermal stress. The dominant failure mode remains interface separation, often located at a weak interface between the microvia target pad and the electrolytic copper fill of the internal microvia [12].

Due to its size and construction, a microvia is inherently less susceptible to failure as a result of thermal stress. Thermal cycling is generally accepted as an accelerated test method for traditional via structures. The applied temperature extremes result in a cyclic strain that induces plastic deformation of the plated copper inside the via barrel, manifesting itself as barrel cracking. Applying the same temperature extremes to a microvia does not create plastic strain and thus the microvia can theoretically withstand millions of thermal cycles [18].

Since product acceptance testing is time constraint, microvia testing is often performed at elevated stress levels that do not relate to product life. The aim of the testing is to assert the manufacturing quality of the microvia, under the assumption that a properly manufactured microvia will not affect the reliability of the product. If and how a test coupon can represent the

manufacturing quality of a whole panel is an ongoing debate. PCB manufacturers do not intend for their PCBs to merely pass the product acceptance testing. They would like to know how much margin there is with respect to the acceptance criteria and which parameters affect this margin. Microvia testing at elevated stress levels until failures are observed can help to determine and optimize process robustness.

The difficulty with designing test coupons for microvia testing does not lie in performing the lay-out, but in choosing between the endless possibilities. The first step is to define the design parameters of the individual microvia: the drill diameter for the given dielectric thickness (which determines the aspect ratio) and the pad diameter. For product acceptance, the build-up of the board will be fixed, but for a dedicated test campaign, the number of prepreg sheets and the choice of glass fiber weave could have an impact on the test results. When multiple levels of microvias are present, the positioning of the microvias with respect to each other becomes a test variable. Two levels of microvias can be stacked or staggered. The staggering can be designed as adjacency of the microvia pads or the microvias can be placed closer together or further apart. Three levels of microvias can be fully stacked, fully staggered or a combination of two stacked and one staggered microvia (Figure 4). The two stacked microvias can be placed between layer 1 and 3 (semi-stacked outside) or between layer 2 and 4 (semi-stacked inside). In case of staggering, this can be in a staircase fashion or in a spring-like fashion, with varying distance between microvias.

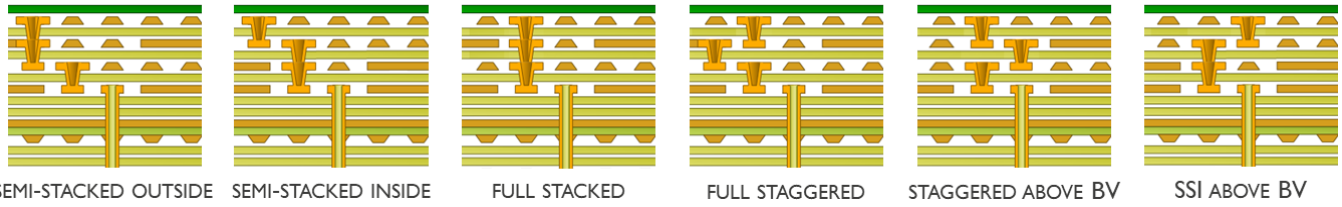

Figure 4. Selection of possible configurations for three levels of microvias: (*from left to right*) **semi-stacked outside, semi-stacked inside, full stacked, full staggered, staggered above core via and semi-stacked above core via**

Another design variable for microvia test coupons is the presence and location of the core via. The presence of the core via near the microvia can have a significant impact on the test results. This is not only the case when stacking the microvia on top of the core via. The distance between the core via and the microvia in the connecting layer has an influence as well. In addition, placing the microvia above the core via in an adjacent layer can reduce the lifetime of the microvia. In version 2.0 (June 2018) of IPC-2221B appendix A, IPC introduced propagated test structures for D coupons. In this case, the core vias are part of the daisy chain and a failure in the core via will stop the test. While this makes sense for acceptance testing, it will obscure the results of comparative testing of different microvia configurations. A work-around, which is applied in IST coupon design, is to include the core via in the coupon, but not make it part of the daisy chain [2].

A final consideration in microvia test coupon design is the number of microvias to include in a daisy chain. Independent on the actual test method, a daisy-chain can consist of a single microvia up to a few hundreds of microvias. Two conflicting requirements play a role here. A threshold is defined as failure criterion for the resistance monitoring of the daisy chain during testing. This threshold needs to be high enough to be detected accurately and low enough to facilitate root cause analysis. A long daisy-chain inherently has a high resistance, with a significant portion of that resistance in the interconnecting traces. When all the (micro)vias in the chain start failing at the same time (wear-out type failure), the test is stopped before the vias fail completely. If, however, a single via fails, the resistance of that via needs to be almost infinite (nearly electrical open) before the threshold on the overall resistance is reached. With the right precautions, shorter chains can be measured more accurately and thus the testing can be stopped earlier in the failure process. The drawback of shorter chains is that fewer microvias are tested and thus more test coupons are needed to represent the high amount of microvias on the entire panel. In addition, a short chain of 10 microvias with a pitch of 1.27 mm (or higher) cannot be considered representative for an array of more than a thousand microvias in a BGA pattern with 0.8 mm pitch.

The reference test method for evaluating thermal reliability remains thermal cycling. This is performed in a single chamber system at ambient pressure. As explained above, the stress levels applied during testing are too low to induce failures in microvias. In addition, microvia separation is known to occur at high temperature and becomes difficult to detect when the temperature decreases again. High precision measurements at intervals of 1 s to 10 s are required to electrically detect these intermittent failures, which is hard to implement in a typical single-chamber configuration. Since the interface separation is known to recover at room temperature and because it is hard to detect in optical microscopy, relying solely on microsectioning might not reveal defects in microvias after chamber thermal cycling (**Figure 5**). Microsectioning, however, remains an

important tool in failure analysis after testing and advanced techniques such as ion beam polishing can be applied to improve the defect coverage for microvias [14].

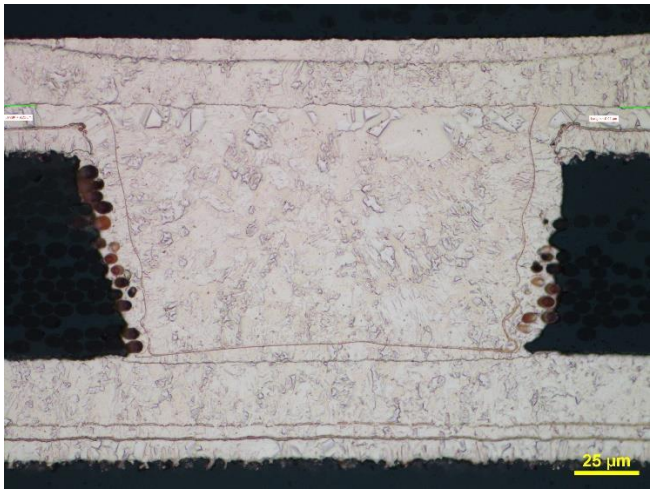

Figure 5. Etched microsection of a microvia after thermal cycling (200 cycles from -60 °C to +140 °C)

Microvia testing using IST follows a dedicated approach. As microvias experience lower stress levels during cycling, the test temperature needs to be increased to apply sufficient stress to the microvia. For epoxy-based materials, a test temperature of 190 °C is used, while for polyimide testing is performed to 210 °C. This stress level is no longer related to the mission profile, but applied to determine if the manufacturing quality of the microvia is adequate. Until recently, it was believed that the microvia would fail either early (less than 100 cycles) or not at all. An IST endurance of ≥ 100 cycles was specified with a maximum increase in resistance of 4 %. After encountering failures on microvias that successfully passed the 100 cycles and observing wear-out type failure mechanisms in microvias after a few hundred cycles, it was decided to increase the threshold to 400 cycles, in line with the standard vias.

In the frame of the basic HDI qualification, late microvia failures were encountered during IST. Two coupons failed at about 300 cycles from room temperature to 210 °C, following six times preconditioning to 230 °C and 500 cycles at 170 °C. Failure analysis confirmed that the cracks originate at the edge of the contact area between the microvia and the target pad and preferably propagate along the plating interfaces (for example, between the electroless and galvanic flash plating in the case of Figure 6). This failure location corresponds to the areas of highest stress in the microvia, as can be seen from the modelled strain values in Figure 2 (areas of highest stress indicated in yellow). Note that this failure mode is different from the weak microvia interface failures from the IPC alert, which typically manifest themselves during the first few reflow cycles (or "*preconditioning*" in IST terminology). In-depth process optimization resulted in reinforcing the plating interfaces and the failure did not occur anymore in any subsequent testing. An extensive IST benchmarking activity including multiple ESA qualified PCB manufacturers was performed [19]. No failures were observed for the microvias at 0.8 mm and 1.0 mm pitch from any of the manufacturers after 1000 cycles to 210 °C.

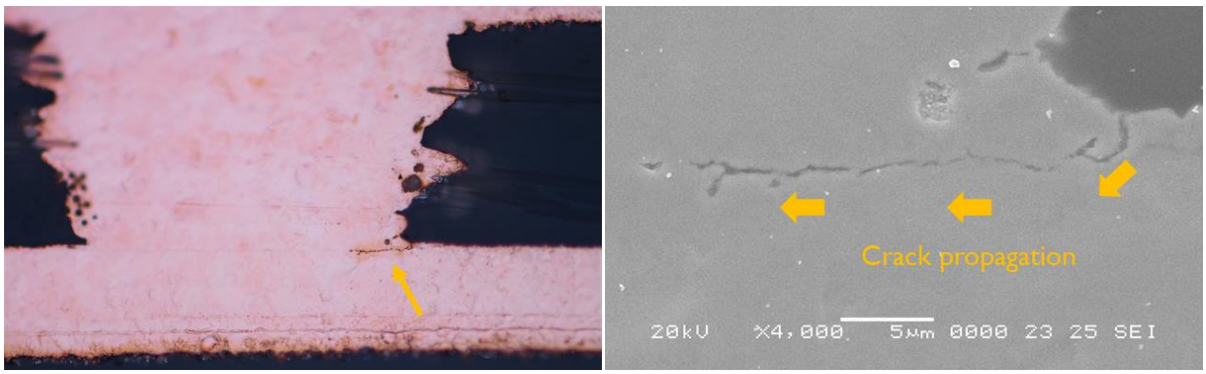

Figure 6. Optical (*left*) **and SEM** (*right*) **inspection of microvia failure after IST**

In response to the weak microvia interface issues, the IPC put forward convection reflow assembly simulation (IPC-TM-650 2.6.27B) as a method to screen microvias after production. The motivation for this test method is that the highest temperature extremes that a PCB is subjected to in its lifetime is during reflow assembly. The key aspect of this test method, compared to IPC recommended testing in the past, is the continuous resistance monitoring of daisy chains in order to detect intermittent failures. While electrical monitoring is feasible inside a traditional reflow oven, dedicated test systems are easier to setup and provide better measurement accuracy and speed. Test method IPC-TM-650 2.6.27B defines A/B, AB-R, and/or the D coupon in accordance with the requirements of IPC-2221B Appendix A as allowable test specimens. The coupons shall be subjected to a 230 °C, 245 °C or 260 °C reflow profile, with a minimum of six reflow cycles. Resistance measurement are to be performed every second during the entire reflow cycle. The acceptance criterion is a less than 5 % increase in resistance using the first cycle's peak temperature resistance as the reference value. After testing, the test specimens are microsectioned for compliance to the applicable performance specification. Several large OEMs in the US space and defense sector have implemented this test method to screen for weak microvia interfaces [16, 20, and 21]. The perceived disadvantage for testing HDI technology in space applications using this protocol is the fact that six reflow cycles only represents the start of the product life cycle, not the end. There is the option to continue performing reflow cycles beyond the required six, but this is yet again a higher test temperature (compared to IST) and thus, even less representative with the risk to overtest.

To address this disadvantage, the convection reflow assembly simulation is sometimes complimented with air-to-air thermal shock (IPC-TM-650 2.6.7.2C) as these can be performed in the same test system and using the same test coupons (IPC-2221B D coupon). The acceptance criterion of 5 % remains the same, although the resistance is measured only once per cycle at the high temperature extreme. The test conditions are dependent on the material parameters (Tg) and the peak reflow temperature. With temperature ranges (ΔT) up to 250 degrees and more, this test method becomes efficient for microvia testing.

D-coupons from the same batch of the qualification test vehicle for the basic HDI technology were subjected to convection reflow assembly simulation (six times reflow to 230 °C), followed by air-to-air thermal shock. A similar temperature range as for thermal cycling was applied (-55 °C to +145 °C) for up to a 1000 cycles. The daisy chains with individual microvias (no core vias present) did not show any resistance increase after reflow simulation nor after 1000 thermal shocks (Figure 7). D-coupons with propagated structures from the same panels showed failures in the core vias after 650 and 570 cycles on average, for 0.8mm and 1.0mm pitch respectively. The failures observed during IST were not observed during convection reflow assembly simulation and air-to-air thermal shock testing. The reason for this can be found in the lower maximum temperature that was adjusted to represent the standard ECSS chamber thermal cycling profile (from -55 °C to +145 °C). Future work includes retesting at higher maximum temperature, as per the standard protocol, to 10 °C below Tg. In addition, the absence of core vias in the individual microvia daisy-chains results in lower stress on the microvia.

A second test method that relies on current to heat the test coupon is current-induced thermal cycling (CITC), which is described as method B in IPC-TM-650 2.6.26A. The test method was developed at IBM Endicott (now part of TTM Technologies, Inc.) and has been applied to microvias since the late 1990s. While the heating method is similar to IST, the coupon design, test parameters and overall approach are somewhat different. A first, important difference is that the CITC test coupon contains only a single daisy chain that is used for both powering and resistance monitoring. The temperature coefficient of resistance (TCR) is determined for each coupon before starting the test. The temperature control and failure detection are both realized through the continuous monitoring of the TCR. The maximum allowed resistance increase at high temperature is calculated based on the acceptance criterion (typically 5 %) and the TCR at the start of the cycle. The test method allows for rapid temperature cycling from room temperature to any desired temperature. Based on experience from previous testing, cycling for microvia evaluation is preferably performed up to reflow temperatures (220 – 230 °C for SnPb assembly, 245 – 260 °C for lead-free assembly). This differs from the recommended IST parameters in ECSS-Q-ST-70-60C, consisting of six times reflow simulation ("preconditioning") followed by cycling to 190 °C (epoxy) or 210 °C (polyimide). More details on the CITC test method and an excellent read on microvia testing in general can be found in [22].

As part of the complex HDI technology evaluation, the thermal reliability of the microvia configurations from Figure 4 will be assessed using convection reflow assembly simulation, air-to-air thermal shock, interconnection stress testing and current-induced thermal cycling. The results will be published elsewhere.

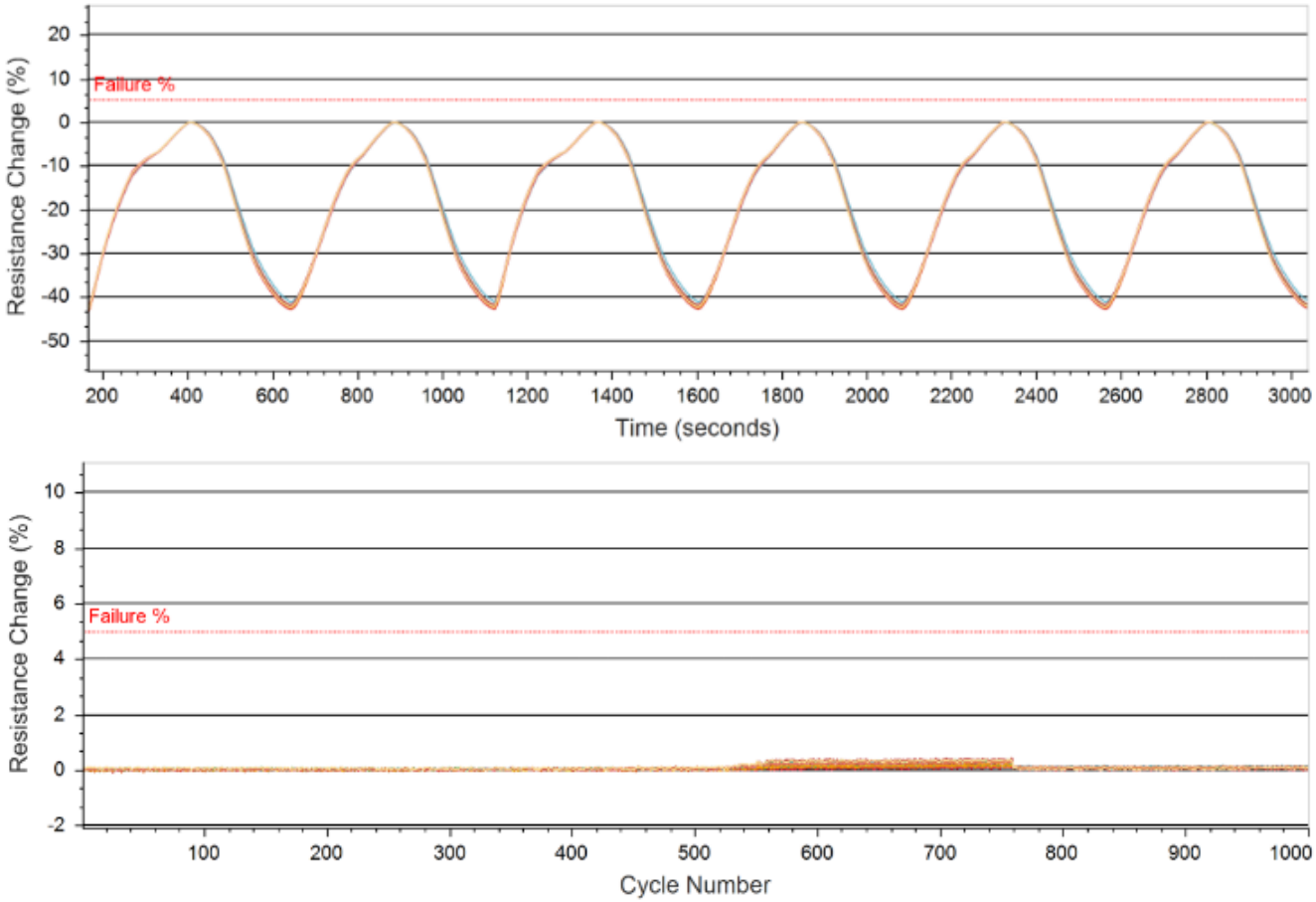

Figure 7. Test results for individual microvia daisy chains using IPC-TM-650 2.6.27B (*top*, six times reflow to 230 °C) and 2.6.7.2C (*bottom*, 1000 cycles from -55 °C to +145 °C)

Conclusion

Based on the dimensional and functional requirements of relevant AADs for space applications, the HDI technology parameters and associated design rules were determined. Two categories of HDI technology are evaluated: two levels of staggered microvias (basic HDI) and (up to) three levels of stacked microvias (complex HDI).

The lessons-learnt from the qualification testing of the basic HDI technology are presented. Several challenges were encountered during the design, testing and evaluation of the basic HDI technology. The main issues were related to the positioning of the microvias, IST coupon design, microvia failures and core via performance. The present activity has achieved a significant step towards qualification of basic HDI technology, as almost all elements of the test campaign were meeting the acceptance criteria. A repetition of this test campaign is ongoing with a view to polish away the final hurdles.

The qualification of the basic HDI technology is only the first step in this extensive study on HDI technology for space applications. A thorough reliability assessment is underway. Various test methods for microvias will be evaluated in order to arrive at a test flow that can assure an adequate confidence level for both qualification and procurement.

As most test houses agree, there is no single, ideal test method to evaluate microvias. All test methods apply elevated (and not necessarily representative) stress levels to assess the quality of the microvia. Poorly manufactured microvias are screened by implementing continuous resistance monitoring during stress application. Comparing results between test methods is precarious, even under well-controlled circumstances. Experience is key in evaluating test results. Test houses with decades of test results are still learning every day. A thorough understanding of the impact of design variables, manufacturing processes and test parameters is more important than the choice of a microvia test method.

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