Challenges for spacer and source/drain cavity patterning in CFET devices

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ABSTRACT

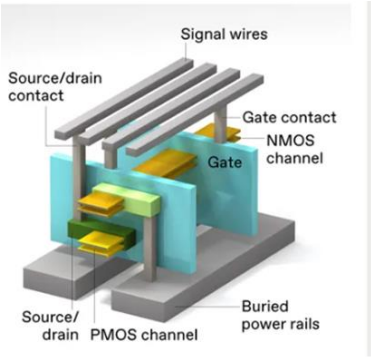
In a complementary-FET (CFET), n- and p- type transistors are stacked on top of each other. This stacking approach results in very high aspect ratio vertical features which brings critical challenges for nanosheet (NSH), gate, spacer, and source/drain (S/D) cavity patterning. Silicon nitride spacers are commonly used to electrically isolate and protect the silicon gate during S/D epitaxial growth and to precisely define the channel length (Lg) [1-4].
In this work, we will discuss the spacer film opening, the optimization of the S/D cavity profile and propose options to reduce the gate hard mask consumption. We were able to straighten the S/D cavity profile in the SiGe superlattice substrate by tuning specific process parameters, during the various etch and over-etch steps of the stack. Chemical analysis of the sidewall of the cavity, by TEM/EDS, confirmed that the formation of a passivation oxi-nitride compound is key to achieve vertical cavity profile. The chemical mapping of the cavity was done through the Si and SiGe25% sheets. A Si, O and N containing passivation layer is present in the cavity which seems to be thicker at the top and thinner at the bottom of the cavity. Furthermore, polymer capping methods were investigated to reduce the consumption of oxide hard mask (HM) during spacer etch. Process optimization for the cavity shape in the S/D recess etch was conducted using TEM characterization.

1. INTRODUCTION

As we approach the limits of scaling, novel device architectures are needed to meet the demand of a smaller transistor footprint while maintaining high performance [1]. Scaling started at "planar/horizontal" designs and along the journey it brought us towards the 3D fin shaped devices and the gate-all-around structures. These designs have shown their challenges to further scale down device footprints in horizontal device designs. Leveraging the 3rd dimension (vertical) seems to provide a path forward. In CFET, both polarities n-MOS and p-MOS are stacked on top of each other and share a common gate, whereas the source/drain (SD) contacts are separated. This design enables reduction of the area footprint and the power consumption in the device. This 3D-stacked CFET will be the key to extending Moore's Law into the next decade [2]. However, making stacked CFET transistors poses serious integration challenges. In the monolithic approach, both n- and p-MOS devices (top and bottom) are stacked and high aspect ratio (HAR) nanosheet, gate and spacer/source-drain patterning steps are required. Moreover, complex superlattice structures, containing stacked sheets of tall epitaxially grown Si and SiGe in variable concentrations. In specific integration schemes that implement the mid-dielectric isolation layers after the gate etch the high Ge-content epi layers are even replaced with Si_3N_4 dielectric layers forming a complex stack for the S/D recess etch these. These new stacks make these patterning steps even more demanding. Both top and bottom, devices may contain one or more Si channels, defining the channel length and isolation materials between the top Si channel and the bottom Si channel. In this paper we report about the challenges for the spacer-S/D -drain patterning step, and we mainly consider the integration concept of a fin with only two Si channels separated by SiGe material to make a uni-channel top or bottom device by introducing a cover spacer (Figure 1b.). The thinner cover spacer protects the top Si channel during the epitaxial growth of the bottom device.

We don't report yet on the patterning requirements for the CMOS CFET's. Figure 1b shows the sequence of integration steps to make a bottom device containing one Si channel. After gate etch and wet clean the PEALD Si_3N_4 film (8 – 14 nm) is deposited conformally over the high aspect ratio (HAR) gate and nanosheet fin. The "spacer etch and fin recess 1" is the first patterning step and subject in this paper, followed by "spacer etch and fin recess 2" after cover spacer deposition. The

spacer creates an offset between gate and highly doped (N or P) source/drain area. It also electrically isolates and protects the silicon gate during the epitaxial growth in the source/drain area, and it precisely defines the channel length.



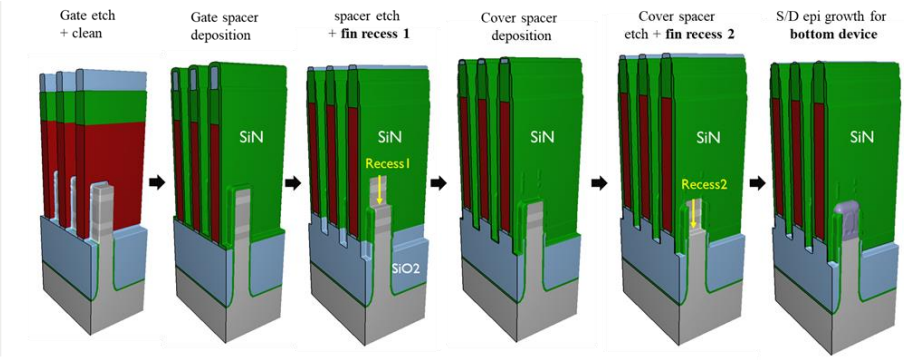


Figure 1a (left). Cross section of a CMOS CFET device, with two Si-channels per device.

Figure 1b (right). Sequence of steps to make the source and drain in a bottom device, single Si-channel per device is illustrated in this scheme.

Multiple requirements are needed for both patterning steps. The spacer etch should be anisotropic to minimize the lateral Si_3N_4 spacer consumption. Spacer pull back at the top of the gate should be minimized to avoid dummy poly Si, from the gate, to be exposed during epitaxial growth of the source/drain area. Selectivity towards the gate oxide hard mask is important allowing sufficient Si_3N_4 HM budget to act as a stopping layer for subsequent CMP steps. Selectivity to STI oxide is important to maintain good lateral electrical isolation. The cavity profile is the most important parameter as it will define the epi defectivity and the total source/drain volume. It is directly linked to the electrical performance of the CFET device. Furthermore, lateral SiGe consumption should be controlled. Overall, the structure that will be etched is a high aspect ratio feature (11:1) at contacted poly pitch (CPP) of 48 nm that requires special plasma tuning knobs, such as plasma pulsing, cyclic etch and high ion energy.

2. ETCH RECIPE SET UP

A conventional spacer etch recipe contains a main etch step (ME), followed by an over etch (OE) and a S/D cavity etch, or recess etch step. Figure 2 shows the configuration of the spacer etch process. The ME step opens the Si_3N_4 film in the source/drain area and on top of the gate, while the OE targets to etch back the spacer along the tall NSH fin. The ME and OE are F-based plasmas that must be very anisotropic, especially during the OE and exhibit high selectivity over the oxide. Since we target full pull back of the Si_3N_4 along the NSH, the gate HM and STI oxide are exposed during the OE, Typical F-based chemistries have lower oxide selectivity on the real topography wafers than on blanket wafers. Consequently, they cause gate HM and STI oxide consumption. There are ways to overcome the selectivity challenges, which will be discussed later in this paper. The S/D cavity etch, or NSH recess, is typically done using Cl or HBr based plasmas. These chemistries typically provide better selectivity towards Si_3N_4 and SiO_2 materials, however, sufficient sidewall passivation by oxidation and advanced process knobs are needed to attain S/D cavity profile specifications and selectivity's. These advanced knobs include, for example, ion energy pulsing, high ion energies and cyclic etch approaches. The cavity is etched subsequently in the source/drain area next to the gates, where it will contain the epitaxially grown material afterwards.

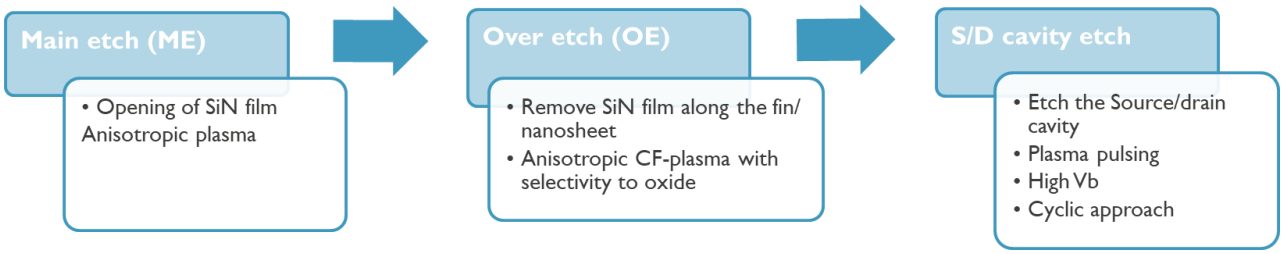


Figure 2. Etch recipe configuration: Main etch / over etch / cavity etch with typical plasma characteristics.

Figure 3. Shows the calibration curves for the cavity depth and the spacer height during the cavity etch and spacer over etch, respectively. In the OE step, it is key to pull down the Si_3N_4 spacer along the NSH. The spacer pull-back in the OE is typically done before the cavity etch as it increases the plasma access towards the source/drain area. Also, the spacer pull back (OE) can be linearly intra- or extrapolated to target full or partial spacer pull back.

. The cavity etch rate, under specific process conditions can be linearly intra- or extrapolated to target a specific cavity depth. Both steps demonstrate very good center-to-edge uniformity.

The dry etch performance is typically evaluated by CD SEM, optical emission spectroscopy, FIB and TEM.

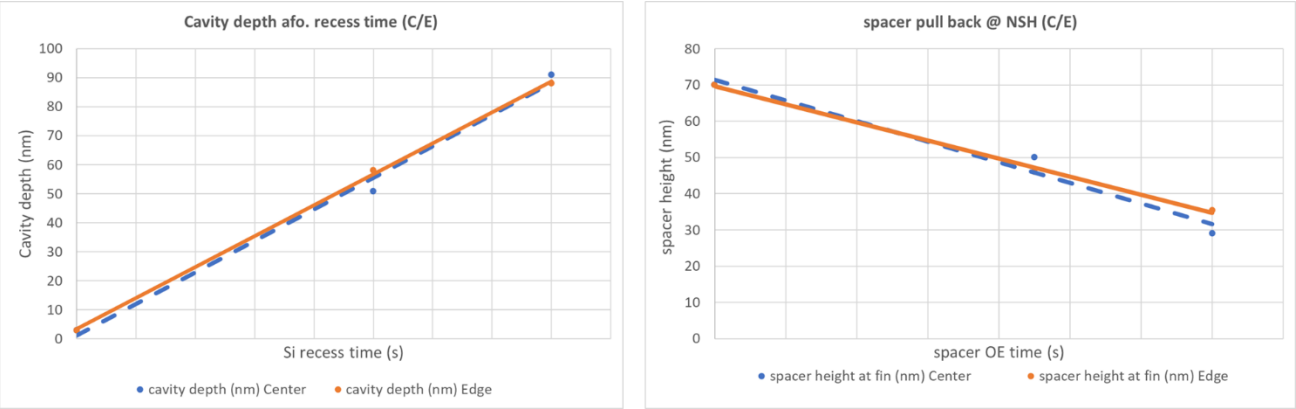


Figure 3. calibration curves for cavity depth and spacer pull back as function of etch time collected on TEM pictures.

It's key to execute an accurate breakdown of the process (process movie) in the target structures to assess the contribution of every individual step in the final patterning result. Figure 4. shows the preliminary process movie, collected by TEM, in the device structures starting from the Si_3N_4 film as deposited, over the spacer film opening (ME) and early cavity etch results. The Si_3N_4 spacer film is deposited in a very conformal way, resulting in equally thick Si_3N_4, wrapped around the gate. After the main etch, in a non-selective F-containing plasma, the film is opened at the top and the bottom of the gate. The subsequent over etch removes the Si_3N_4 along the NSH fin and fully consumes the gate oxide HM on top of the Si_3N_4 part. This HM process was used in the subsequent tuning of the cavity profile, as it was not within the scope of development in these proceedings, and the focus was on improving the cavity profile. The HM erosion and tuning of process, to increase selectivity to SiO_2 HM, is not discussed here but is addressed in other developments. Furthermore, during the over etch of the Si_3N_4 spacer, the top of the NSH is already etched ~ 15 nm. The HBr or Cl – based source/drain cavity process etches back the NSH fin until the original level of the STI oxide. This step has reasonably good selectivity to oxide, but it can lead to bowed cavities if not well tuned. The main contribution in STI oxide consumption comes from the spacer over etch step, as previously mentioned. Reducing STI oxide consumption is one of the main challenges in the CMOS CFET patterning and is currently being investigated. Loss of STI oxide leads to loss of isolation capability between several

transistors. The cavity shape is pretty much bowed due to a non-optimal passivation/etch ratio and ion angle distribution, at this early etch development stage.

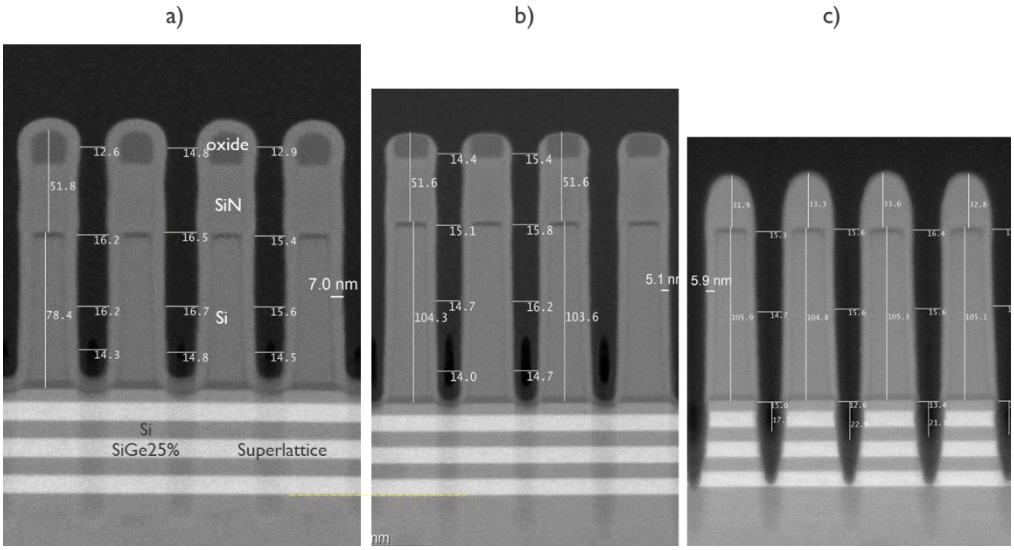


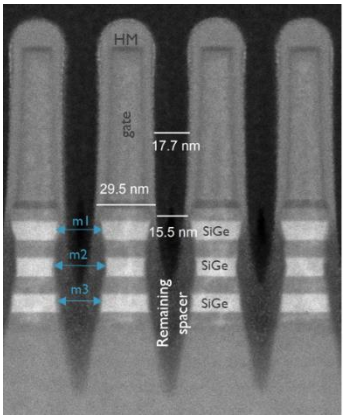
Figure 4. Etch movie picture: a) after conformal Si_3N_4 deposition, b) after spacer main etch (ME), c) after spacer over etch (OE) and preliminary cavity etch.

3. PATTERNING CHALLENGES AND METHODOLOGY

Short loop test wafers were prepared to develop the spacer and S/D recess processes. After the epitaxial growth of the superlattice structure which consists of 3 alternating 9 nm sheets of Si and SiGe 25%, the nanosheet fins are etched, targeting a depth of > 120 nm. After which the shallow trench isolation oxide (STI) is filled and the nanosheets are revealed. The amorphous Si gate material is then deposited (230 nm, nominal). The gate hard mask deposition is done after CMP of Si- dep. Gate patterning is done by single eUV lithography, targeting a gate CD of 19 nm at pitch 48 nm. The 8 nm gate spacer film is then deposited, after which the spacer and S/D etch can be performed. All dry etch experiments were performed in a conductor etch system, on 300mm wafers.

3.1 Source/Drain cavity shape bowing:

The cavity sidewalls must be straight (target = 90 deg +/-1) resulting in the most optimal profile for the subsequent S/D epitaxial growth and device performance. The assessment of the cavity shape is done by automated measurements on TEM pictures. Figure 5. shows the cavity CD (nm) measured in 3 positions: m1 = top, m2 = middle and m3 = bottom of the cavity. By plotting these measurements in a graph for variable etch plasma conditions (different wafers), the shape of the cavity can be easily visualized for the etch conditions. The straighter the cavity, the flatter the line that connects the m1, m2 and m3 measurements, unless the SiGe sheets are equally etched laterally. Concave graphs correspond to non-ideal cavity shapes and further etch plasma tuning is required.



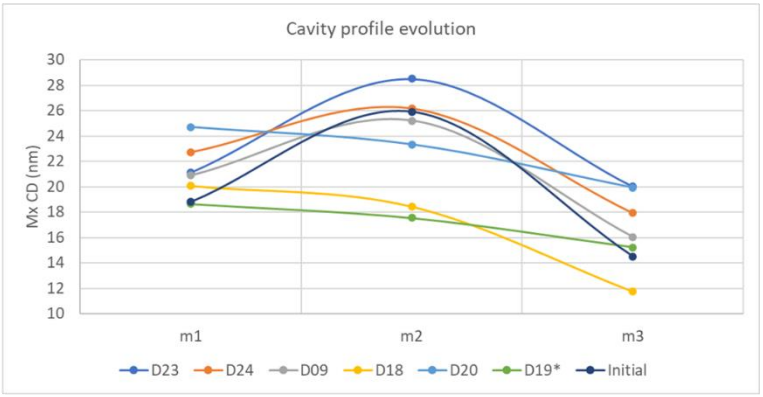


Figure 5a. (left) example TEM picture of cavity for pitch 48 nm and measurement positions m1.m2 and m3.

Figure 5b. (right) visualization of cavity shape based on measurements along the cavity depth.

The non-ideal cavity shape can be attributed mainly to the high aspect ratio (11:1) of the gate topography and the limited plasma access space in the S/D region and how this small spacing interacts with plasma etch species (ions/radicals/byproducts/etc…). The CPP (contacted poly pitch) is 48nm, with poly Si height 165 nm (including the HM), and the spacer thickness of 8 nm making the S/D space CD very narrow (about 12 nm, or less). Consequently, there is limited access for the plasma species to reach the top of the NSH and to initiate the etch of the cavity. This high AR also makes the ions easily deflect, and in combination with insufficient sidewall passivation, leading to uncontrolled lateral attack/etch of the cavity sidewalls. Both SiGe25% and Si will be laterally etched, although SiGe at a faster rate. To resolve the non-ideal cavity shape, the ion angle distribution function should be narrowed down in combination with sufficient passivation, which is typically done by using advanced process knobs such as plasma pulsing and/or mixed mode pulsing. The effect of these advanced plasma etch knobs will be discussed in paragraph 4.

3.2 Gate oxide hard mask consumption:

The consumption of gate oxide hard mask is another challenge that needs addressing, as previously mentioned. The preservation of the oxide HM is important, since whenever it is removed, the Si_3N_4 HM part starts to be consumed and gets rounded. This deformation of the Si_3N_4 HM is critical as this layer acts as a stopping boundary for the CMP process downstream in the integration flow and will create further challenges for CMP control, whenever it is deformed. There are several strategies to maintain the SiO_2 HM while fully etching the Si_3N_4 spacer back, without jeopardizing the Si_3N_4 HM, that are currently being implemented. The details of various strategies are beyond the scope of this proceeding; however, one approach is discussed below, in section 4.2.

4. RESULTS AND DISCUSSION

4.1 Source/Drain cavity shape straightening:

The first ~15nm of the cavity is etched during spacer OE, due to limited selectivity, as described previously. In the first learning cycle (LC), the ion energy was increased, the plasma-on time varied, and an O_2-based passivation step was also

added, as can be seen in figure 6. Figure 6b. shows the starting etch condition. For this condition the Si_3N_4 spacer is not fully removed, and the cavity is bowed. Ion energy increase, and plasma-on time reduction shows an improvement of the cavity profile, but it's not optimal yet. Addition of a passivation cycle after spacer ME + OE (Figure. 6d) shows a straightening at the top of the cavity, with taper in the bottom part of it. Further increasing the ion energy allows to etch a deeper cavity (Figure 6e). These iterations provided insight on critical knobs and trade-offs of each independent parameter. However, even though some improvement on cavity profile is attained, the profile is still not meeting the spec. This systematic study enabled the combination of the learning cycles and the subsequent process development.

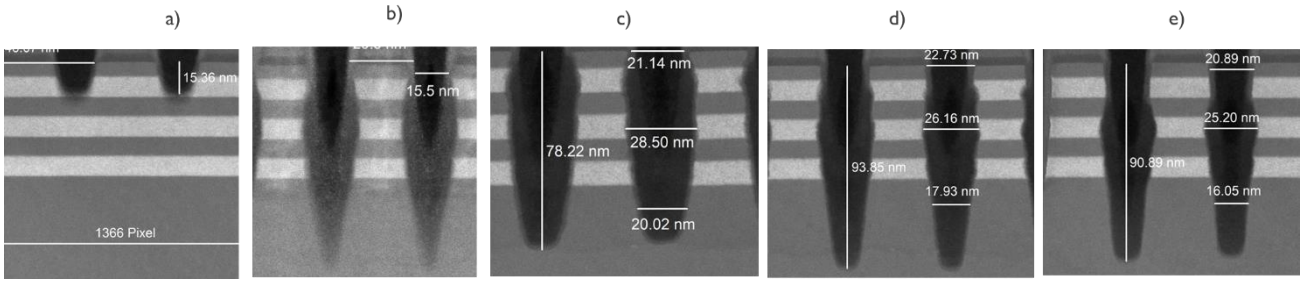


Figure 6. variations in cavity etch conditions: a) after spacer ME + OE, b) after starting cavity etch condition, C) after ion energy increase + plasma-on time reduction, d) after ion energy increase +plasma-on time reduction + increased passivation cycle, e) after further ion energy increase + plasma-on time reduction.

The combination of ion energy increase, pulsing and etch/passivation approach is shown in figure 7. This approach results in smooth and straight cavity sidewalls and a passivation oxide is present at the cavity sidewalls. Increasing the ion energy and reducing the plasma-on time no longer has the same effect on the cavity depth, compared to figure 6 approach. Increasing the number of etch/passivation cycles simply does not result in a deeper cavity etch a as strong etch stop layer is created, due to thick passivation oxide formed at the etch front (Figure 7b.). Inserting a F-based break through step did not punch through the passivation oxide at the bottom of the S/D cavity, and further increase would come at other tradeoffs. Also changing the relative time ratio between the passivation cycle and etch cycle by reducing the process time for the passivation was not enough to avoid the etch stop layer, under the specific time ratios considered in these presented data. Removing O_2 from specific S/D etch steps and replacing He with Ar allowed, to provide more ion momentum and less passivation, to punch through the passivation oxide and as a result to etch deeper in the cavity with a straight profile (Figure 7c). After cover spacer integration the profile was acceptable to continue downstream processing (Figure 7d).

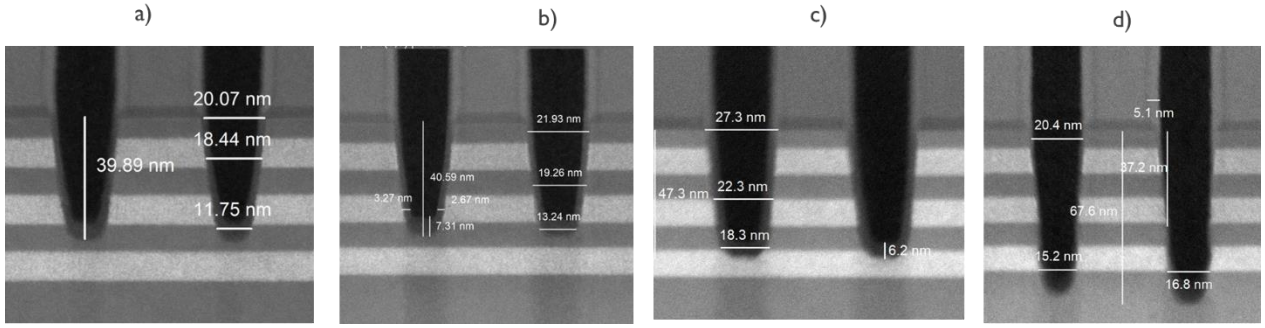


Figure 7. variations in cavity etch conditions: a) after spacer ME + OE + cyclic passivation and etch, b) after spacer ME + OE + increased cyclic passivation and etch at shorter times – etch stop, c) Removing O_2 and replacing He with Ar, d) Best result after cover spacer approach.

To investigate the nature of the passivation oxide along the cavity sidewall, an EELS EDX analysis was performed to chemically map for Si, O, Br, Ge, and N. 3- line scans were made as indicated in figure 8. Line scan 1 starts in the Si sheet

and evolves through the passivation oxide into the cavity, line scan 2 starts in the mid SiGe25% nanosheet, evolves through the passivation oxide and into the cavity. While line scan 3 (Figure 8) starts in the bottom SiGe25% nanosheet, evolves through the passivation oxide into the cavity. As can be seen in figure 9, the first line scan through the top Si sheet measures about ~ 6nm passivation oxide grown on the cavity sidewall. The passivation oxide in the cavity sidewall contains mainly Si and N and closer to the cavity it contains merely Si and O. For line scan 2, through the mid SiGe25% sheet, also about 6 nm passivation oxide is measured. Both the Si and the SiGe sheet are well protected by a passivation oxide. For line scan 3, on the bottom SiGe25% sheet, a thinner passivation oxide has formed and the atomic O- % shows lower intensity. Also, the SiGe sheet reveals some lateral attack as compared to the middle sheet due thinner passivation oxide against the cavity sidewall.

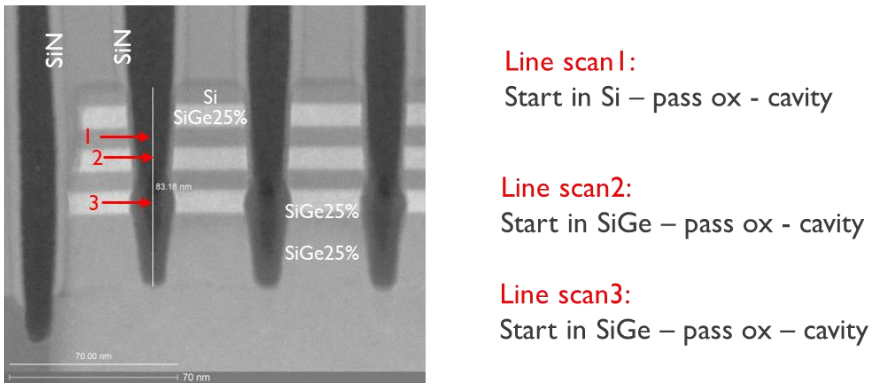


Figure 8. EELS EDX: 3 Line scans to chemically map the passivation oxide along the cavity sidewall. Checking for Si, O, Br, Ge and N.

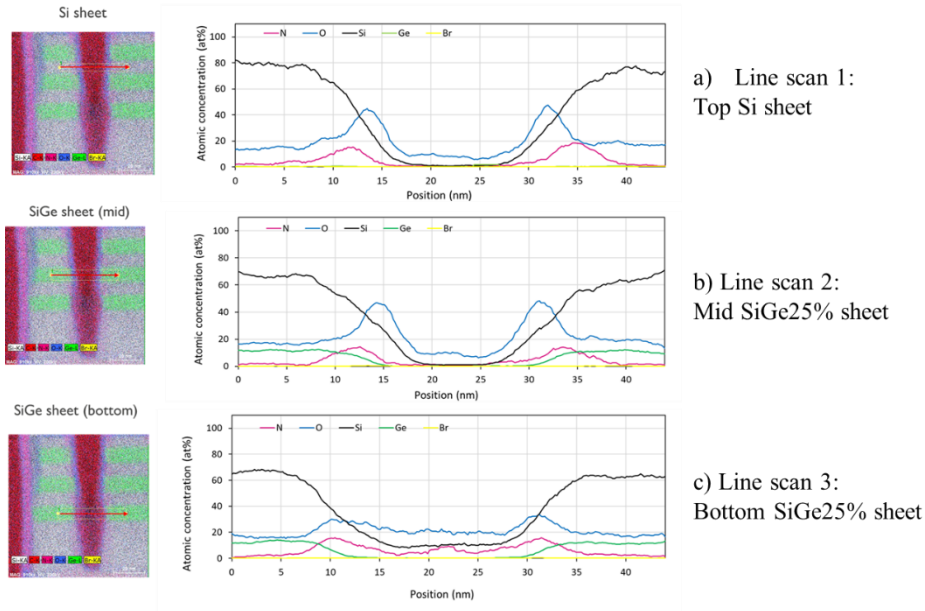


Figure 9. EELS EDX line scans in the S/D cavity

4.2 Gate oxide hard mask loss mitigation:

Figure 10 shows the consumption of the gate oxide hard mask and the STI oxide caused by the Si_3N_4 spacer OE in fin recess 1 and fin recess 2. Limited selectivity in the spacer OE shows significant oxide losses both for the gate HM as well as for the STI oxide loss.

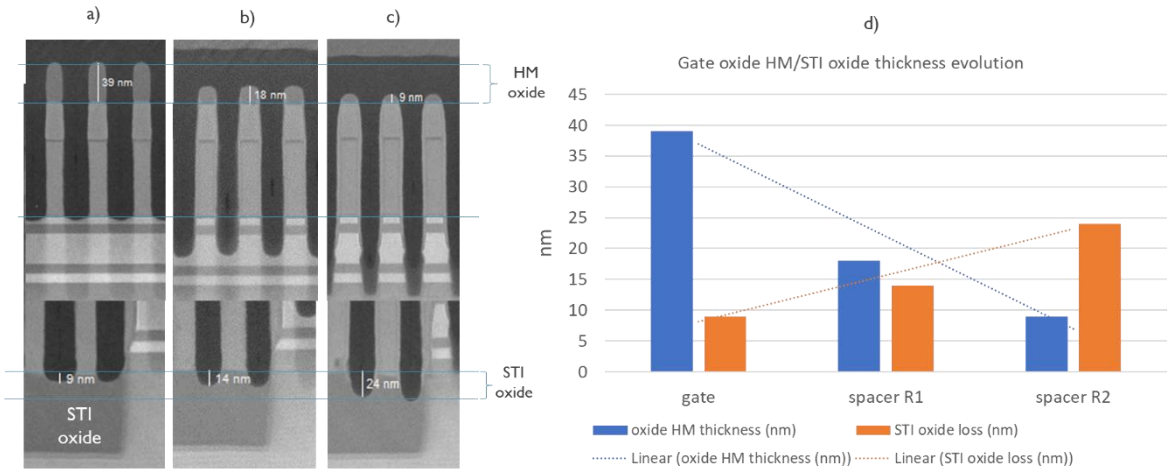


Figure 10. TEM analysis of gate oxide HM loss:

a) after spacer gate etch + diluted HF,

b) after spacer recess 1,

c) after spacer recess 2,

d) Gate oxide HM loss and STI oxide loss after gate etch, cavity recess 1 and cavity recess 2.

One approach to protect the gate HM during the spacer etch and pull back process is by depositing a C-cap layer. This cap can be selectively deposited on the top of the SiO_2 gate HM, by tuning the plasma conditions. This polymer is very resistant to the long spacer OE plasma, as it is barely consumed. The deposition rate is very linear, and the target cap thickness can be calibrated based on Figure11. b. and adjusted based on process needs. However, over-depositing the C- capping layer can lead clogging the space between the gate, which would eventually prevent the spacer and S/D cavity etch. Another advantage of this capping approach, aside from SiO_2 HM protection, is that it allows the reduction of the incoming gate HM thickness. This benefits the integration scheme and other process steps, such as the gate etch by lowering the stating aspect ratio.

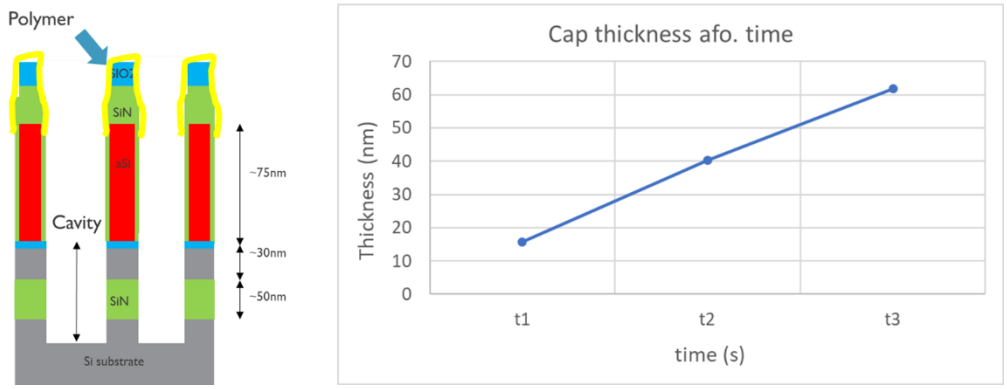


Figure 11: a) (left). Principle of top gate capping by C- polymer, b) (right) Cap thickness grows as a function of time.

Figure 12 shows TEM pictures of remaining gate SiO_2 HM after OE is applied, with and without C- top gate capping. TEM images taken after the full spacer OE etch process demonstrated that the SiO_2 HM is almost completely consumed if no capping is applied (Fig. 12a). Whereas, with the applied C-capping approach the full SiO_2 HM and spacer at the top of the gate is conserved (Fig 12.b).

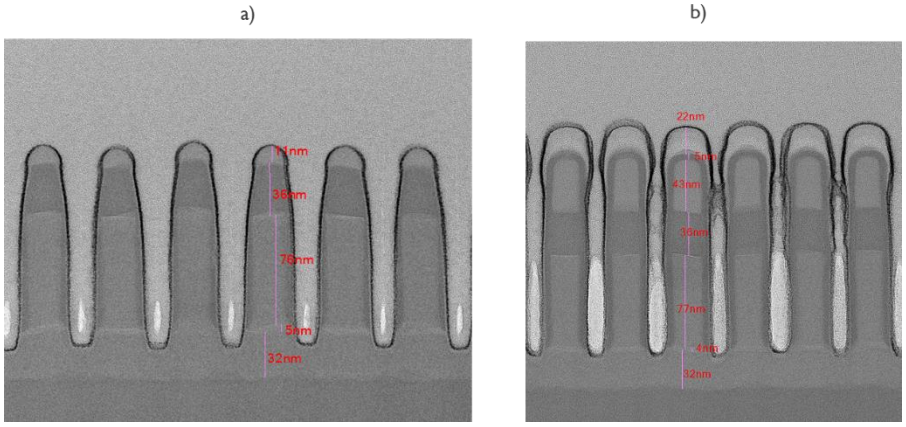


Figure 12. top gate capping: a) left) no top gate capping: gate oxide HM consumption, b) (right) 22 nm top gate capping protects the top of the gate during the SiN spacer etch.

5. SUMMARY AND CONCLUSIONS

In this work the challenges for spacer and source/drain patterning for uni-channel monolithic CFET devices were discussed. A successful demonstration of spacer and source/drain patterning to make an integrated top and bottom device was demonstrated. A need for more advanced process knobs also was demonstrated. To achieve a straight source/drain cavity profile with high selectivity to the gate hard mask and spacer film, more advanced process knobs were required. Balancing the passivation/etch ratio and controlling the ion angle distribution while etching the source/drain cavity were needed to make the cavity profile straight. Selective top gate polymer deposition can reduce the gate hard mask consumption while over etching the spacer film along the NSH fin. This capping layer deposition step should be well controlled to avoid clogging. To continue the development towards full monolithic CFET devices with multiple Si channels in a complex superlattice stack with mid-dielectric insulator (e.g., Si_3N_4), innovative patterning solutions are needed as the device architecture becomes more complicated Challenges include a further increase in aspect ratio due to the integration

of dielectric isolation between top and bottom device and increased requirements for etch selectivity's between the fin stack, gate and cover spacer, HM materials and STI oxide.

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