BEOL N2: M2 through SAxP Process from MP21 to MP26: 193i SAQP vs EUV SADP

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ABSTRACT

193i SAQP has allowed industry for continued BEOL metal pitch scaling, but as metal pitches become even tighter EUV SADP becomes an interesting alternative. In this context we have explored within our dual damascene 3ML test vehicles how the EUV SADP process compares to 193i SAQP for printing MP21 M2 lines. Our first EUV SADP results already show a better wafer CDU compared to our POR 193i SAQP process.

Keywords: multiple patterning, EUV lithography, back end of line, metal pitch 21, line edge roughness, CD uniformity

1. INTRODUCTION

Multiple patterning techniques have allowed industry to pattern beyond the resolution of 193i lithography. Various multiple patterning techniques have been explored such as litho-etch-litho-etch (LELE)[1] or directed self-assembly (DSA)[2] but one of the most acknowledged techniques is self-aligned multiple patterning (SAxP).[3] Nowadays, 193i self-aligned quadruple pattering (SAQP) is the established process for patterning fins[4] and interconnect metal lines.[5] In recent years, however, extreme ultraviolet (EUV) lithography has matured enough to become a contender for 193i multiple patterning. Nevertheless, for the N2 technology node, EUV lithography would need to adopt the multiple patterning approach as well if it wants to keep up with 193i SAQP for the tightest pitches.[6]

Within the back end of line (BEOL), simplification of the electrical wiring is key to enable further die area shrinkage. This, in turn, allows for a higher yield per wafer and, thus, a lower die cost. Die area scaling can be achieved using so-called scaling boosters. Some of the most actively explored scaling boosters include the fully self-aligned via (FSAV),[7] the supervia (SV)[8] and vertical-horizontal-vertical (VHV) routing.[9] Moreover, traditional Cu dual damascene (DD) metal filling is also challenged through the exploration of new metallization techniques such as the Ru dual damascene[10] or Ru semi-damascene process.[11] Meanwhile, traditional metal pitch scaling continues as well, which is where multiple patterning comes in. Herein, EUV self-aligned double patterning (SADP) challenges the established 193i SAQP process for reaching metal pitch 21 (MP21).

In this work, we have explored within our BEOL three-metal-layer (3ML) dual damascene test vehicles (Figure 1) how EUV SADP compares to 193i SAQP for patterning metal 2 (M2) lines up to MP21. Our first results on EUV SADP patterning already demonstrate a better wafer critical dimension uniformity (CDU) between and within metal trench populations compared to our process-of-reference (POR) 193i SAQP process. Moreover, the electrical resistance of the EUV SADP metal lines after Ru DD metal filling comes close to our 193i SAQP process.

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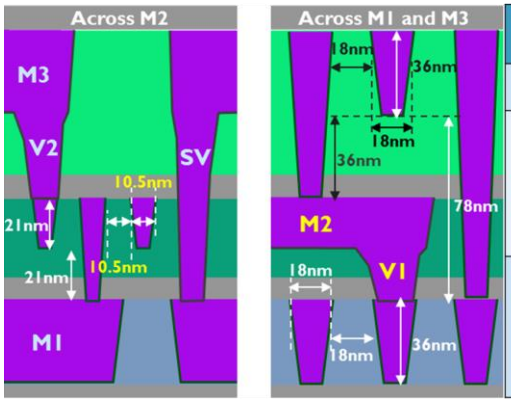


Layer	Metal Pitch	Mask	Litho
M1	36 nm	M1	EUV
M2-V1	21 nm	M2Core	193i/EUV
		M2Block	EUV
		Via 1	EUV
M3-V2-SV	36nm	M3	EUV
		SuperVia	193i
		Via 2	EUV

Figure 1: 3ML dual damascene test vehicle schematic, dimensions, and lithography steps.

2. RESULTS

2.1 M2Core: 193i SAQP vs EUV SADP: target 21 nm MP

The first step to reach the MP21 target is the processing of the M2Core module. Figure 2 shows schematically which steps are followed during the M2Core module following the 193i SAQP and EUV SADP process. In 193i SAQP a line/space pattern is printed using 193i lithography with a target CD of 35 nm and a target pitch of 84 nm. The core lines are then etched and trimmed into the amorphous carbon layer, after which the first oxide spacer is grown. After core pull, the spacer lines are transferred into amorphous silicon (a-Si), followed by the growth of a SiO_x spacer. Finally, the a-Si core will be removed, leaving behind a set of spacer lines. In this way three types of trenches are formed: core (from litho step), gap (from litho step) and spacer (from spacer 1 deposition). In EUV SADP, the EUV lithography step targets a 21 nm CD and a 42 nm pitch. Then, the core is etched and trimmed directly into a-Si. This step is followed by spacer deposition and concluded with the core pull. After EUV SADP only two trench types are formed: core and gap.

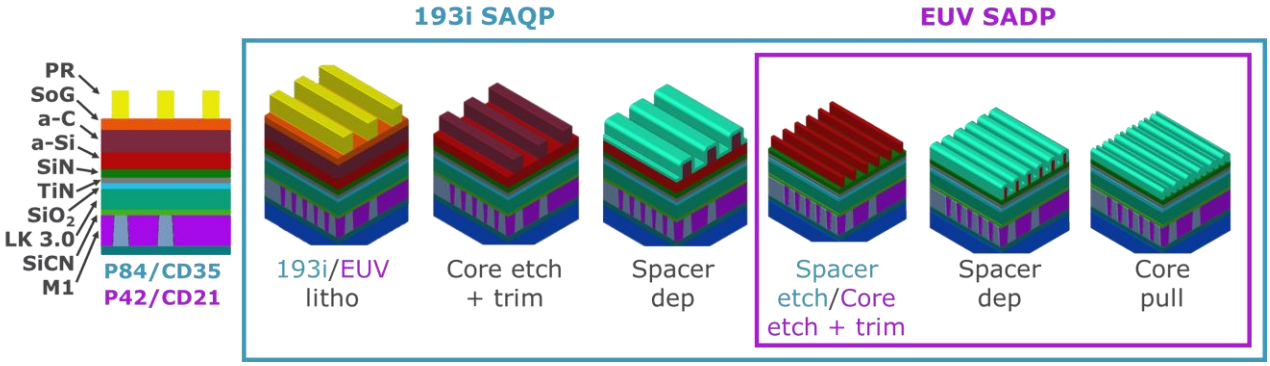


Figure 2: M2Core patterning stack and steps for the 193i SAQP and EUV SADP process.

Figure 3 shows the process windows (+/- 5%) for the 193i and EUV lithography steps. For EUV an overlapping process window is created from the P42/CD21 target up to P52/CD26, while for 193i SAQP just the P84/CD35 (+-5% CD) target is used. Whether EUV or 193i is superior cannot be concluded from these process windows considering that different sources and resists (chemically amplified resist (CAR) for 193i and metal oxide resist (MOR) for EUV) have been used. Nevertheless, both lithography processes offer a workable process window with the EUV lithography process having a somewhat higher exposure latitude (EL) and lower depth of focus (DOF) compared to the 193i lithography process.

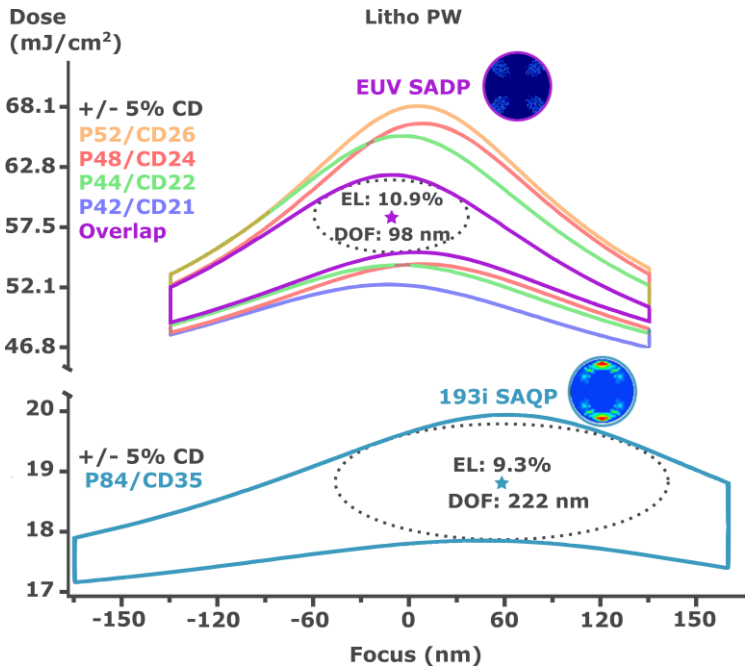


Figure 3: M2Core lithography process window for the 193i SAQP (using CAR resist) and EUV SADP (using MOR resist) process.

The Critical Dimension Scanning Electron Microscopy (CDSEM) images in **Error! Reference source not found.** show a considerably lower biased line edge roughness (LER) and line width roughness (LWR) for the EUV SADP process from the "193i spacer etch/EUV core etch + trim" step until the "core pull" step. This is a positive trend, but the actual values should be taken with a grain of salt, because the metrology component remains in biased LER and LWR values. Most measurements have been performed on the same tools under the same conditions, though.

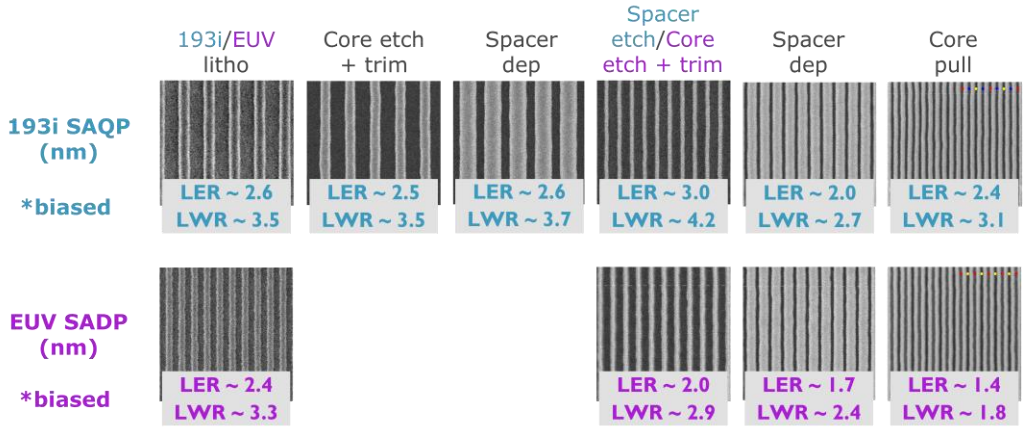


Figure 4: M2Core CDSEM images after each step in the 193i SAQP and EUV SADP process. The biased LER and LWR values shown here correspond to the core/hole populations. The CDSEM images correspond to the pitch 21 target.

The average CD boxplots across wafer in Figure 5 demonstrate a better CDU between and within trench populations for the EUV SADP process compared to the 193i SAQP process. This is a highly positive result for EUV SADP, since having a low CD variability between trenches is crucial for maintaining uniform electrical wiring.

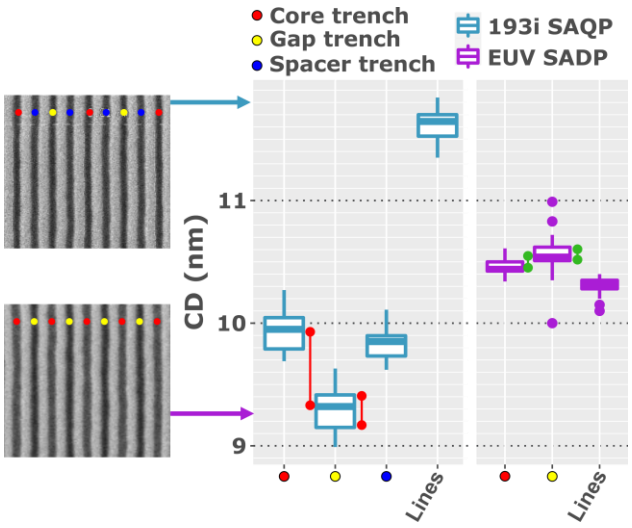
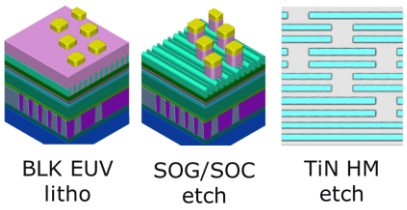


Figure 5: Average CD boxplots across wafer for the different trench populations and lines after core pull for the 193i SAQP and EUV SADP process. The CDSEM images and boxplots correspond to the pitch 21 target.

2.2 M2Block

After the M2Core module comes the M2Block module. The M2Block module has the purpose to cut away spacer line ends as well as cutting the lines at certain places. Figure 6 shows the patterning steps as well as the target dimensions for the block pattern. After the lithography step, SOG and SOC will be etched, followed by a transfer into TiN.



	Resist tonality	Min. Pitch (nm)	Target final CD (nm)	Target litho CD (nm)
193i SAQP	NTD	42 x 72	18 x 21	23 x 26
EUV SADP	NTD	108 x 126	18 x 21	23 x 26

Figure 6: M2Block patterning steps and target dimensions for the 193i SAQP and EUV SADP process.

For both the 193i SAQP and EUV SADP process flow good wafer CDU as well as good M2Block-to-M2Core overlay has been achieved as can be seen in Figure 7.

2.3 Via 1 + low k etch

The M2Block module is then normally followed by the Via 1 module. In the Via 1 module, the vias that connect M1 to M2 are printed. Then, they are transferred together with the M2 lines into the low k dielectric (Figure 8). For the EUV SADP process flow the complete M1M2V1 short loop is still under development. The Via 1 printing has, thus, been skipped for EUV SADP. Instead, the M2Core + M2Block TiN hard mask pattern is immediately etched into low k. Meanwhile, for 193i SAQP a good Via 1 wafer CDU as well as a good Via 1-to-M2Core has been obtained (Figure 9).

The CDSEM images after the low k etch (Figure 10) show that both 193i SAQP as well as EUV SADP suffer from line wiggling as well as pitch walking. Both phenomena are detrimental for uniform electrical performance and should be reduced as much as possible. The boxplots which show the average trench/line CD across the wafer still show that the CDU between and within trench populations is better for EUV SADP compared to 193i SAQP. The CDU has become worse though for both process flows compared to the “Core pull step” in the M2Core module. Additionally, the CD for the MP21 EUV SADP trenches is a bit above the aimed 11 nm target. In the next iteration, this can be solved though by depositing a slightly thicker spacer.

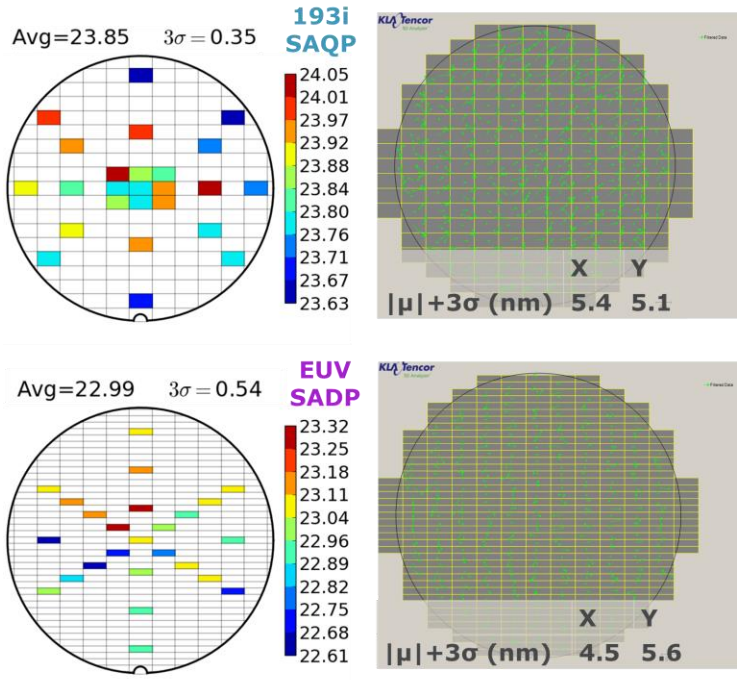
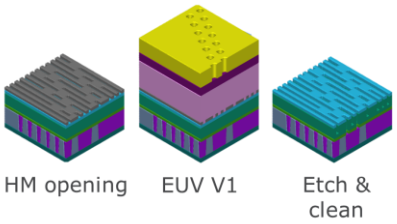


Figure 7: wafer CDU and M2Block-to-M2Core overlay wafer map after the M2Block lithography step for the 193i SAQP and EUV SADP process.



	Resist tonality	Min. Pitch (nm)	Target final CD (nm)	Target SAV CD (nm)	Target litho CD (nm)
193i SAQP	PTD	42 x 72	18 x 10.5	18 x 21	22 x 25
EUV SADP (TBD)	PTD	108 x 126	18 x 10.5	18 x 21	22 x 25

Figure 8: Via 1 patterning steps and target dimensions for the 193i SAQP and EUV SADP process.

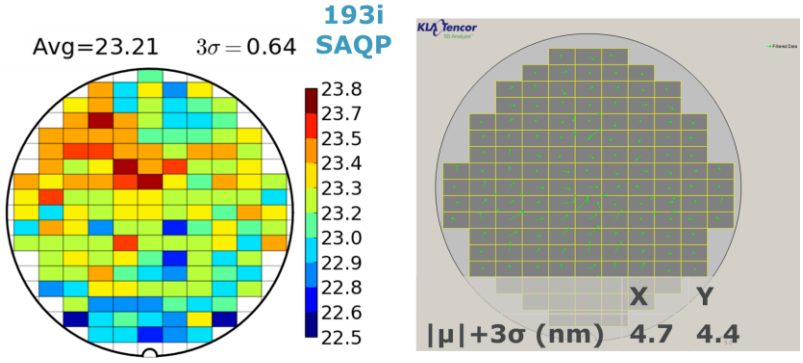


Figure 9: wafer CDU and Via 1-to-M2Core overlay wafer map after the Via 1 lithography step for the 193i SAQP process.

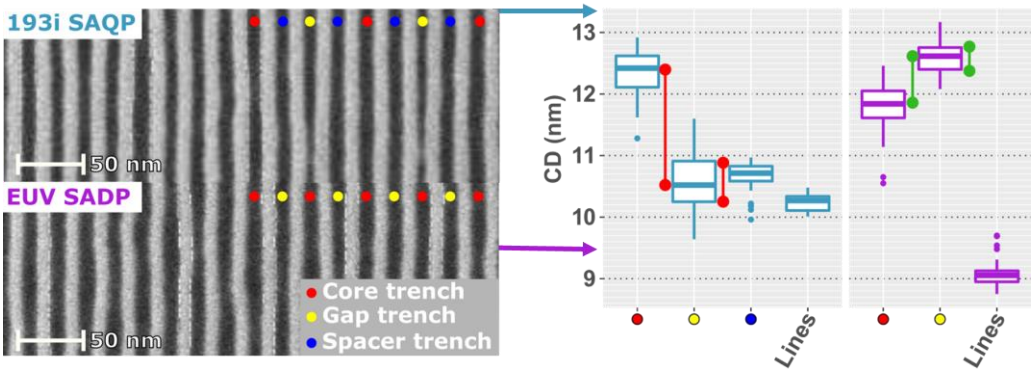


Figure 10: CDSEM images and average CD boxplots across wafer for the different trench populations and lines after low k etch for the 193i SAQP and EUV SADP process. The CDSEM images and boxplots correspond to the MP21 target.

2.4 Metallization and electrical testing

After Via 1 patterning and etching into low k, a dual damascene process is used to fill the M2 trenches and vias with Ru metal. As the Via 1 module has not yet been developed for the EUV SADP process, it's factually following a single damascene process at this point. Consequently, this limits the electrical testing to M2 metal line resistance measurements as depicted in Figure 11. Despite the EUV SADP MP21 gap trenches having a higher CD they exhibit a higher resistance compared to the 193i SAQP MP21 gap trenches. The differences are rather small though and might be chemical mechanical polishing (CMP) related or due to the observed pitch walking. For the EUV SADP process the core metal lines also have a higher resistance than the gap metal lines, which is most likely also due to pitch walking.

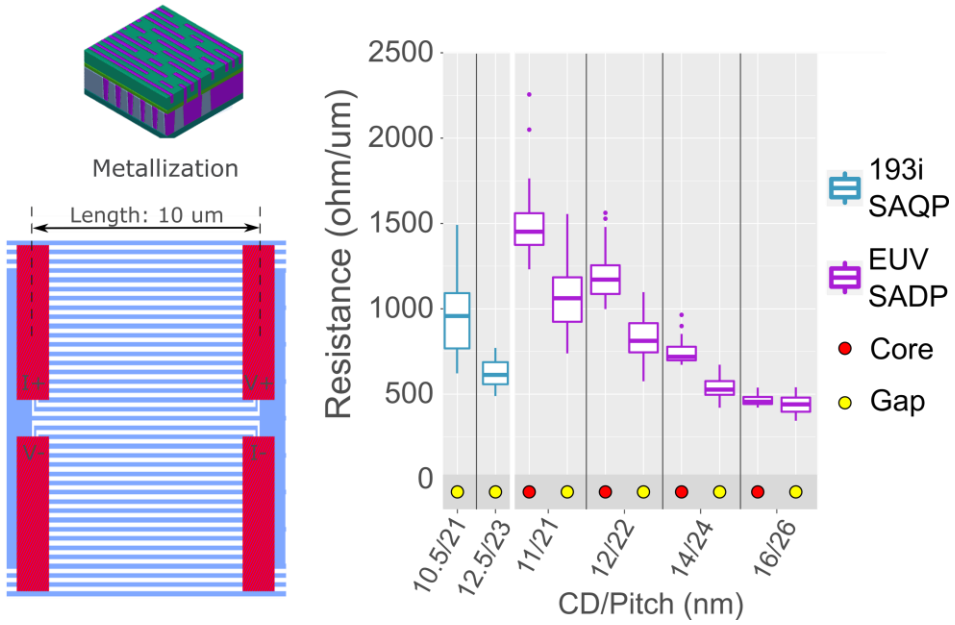


Figure 11: Schematic of dual damascene metallization step, electrical resistance test structure and electrical resistance measurements through metal CD/Pitch for different metal trench populations corresponding to the 193i SAQP and EUV SADP process.

3. OUTLOOK

Our first results for the EUV SADP dual damascene process show a better M2 wafer CDU and just slightly higher electrical resistance compared to our POR 193i SAQP process. This clearly demonstrates the ease of initiating an EUV SADP process compared to a 193i SAQP process. Additionally, we have shown a good CDU and overlay performance for our M2Block and Via 1 module. Next, the focus for improving the EUV SADP process lies in reducing line wiggling and pitch walking after low k etch as well as bringing the final CD closer to its target. Furthermore, the M2 EUV SADP module will be integrated with the M1 and M3 modules for further electrical testing. Additionally, the M2 EUV SADP module will also be used to study defectivity throughout the SADP patterning.

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