First demonstration of Two Metal Level Semi-damascene Interconnects with Fully Self-aligned Vias at 18MP

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Abstract

In this paper we demonstrate the functionality of a semi-damascene integration scheme with fully self-aligned vias (FSAV) for interconnects from 26 to 18nm metal pitch (MP), fabricated on 300mm wafers. We have developed a novel integration flow, using the principle of subtractive etching of Ru, on 2 subsequent metal levels. Using structures with programmed overlay shift, we demonstrate the functionality of a fully self-aligned via process which results in working devices with placement errors of up to 5nm. Furthermore, we show via-to-line breakdown field > 9MV/cm, confirming FSAV.

Keywords: Interconnect, Ruthenium, semi-damascene, fully self-aligned via

Introduction

Replacing Cu damascene with an alternative scheme has been a widely reported research topic in the interconnect community for many years. Ru is a strong candidate as the Cu alternative at local metal level for several reasons, not least that it requires no metal barrier to occupy precious conducting area. Both dual damascene and subtractive metal semi-damascene flows have been demonstrated using Ru [1,2]. The latter has several integration advantages: 1. The line aspect ratio can be increased without the restrictions of filling trenches, which enables resistance reductions at equivalent MP; 2. No metal CMP is needed, which means the resistance variability is governed by the more-controlled film thickness. Additionally, when comparing device performance between comparable dual- and semi-damascene schemes it has been reported that semi-damascene provides higher performance with a smaller area requirement [3].

Below 22nm MP, a fully self-aligned via is required to avoid via-to-line leakage [4,5]. The limits of EUV lithography allow a minimum print of 20nm via hole, which, combined with overlay errors, adds more EPE than is acceptable at narrow metal pitches. The semi-damascene integration scheme uses selective etching to form the via on the confines of the lower metal line. To our knowledge this is a first-time demonstration of a 2-metal level (2ML) device using subtractive metal etch with FSAV. Furthermore, the top metal is combined with air gaps.

Fabrication Scheme

Fig. 1. shows the semi-damascene integration scheme. 30nm PVD Ru on a TiN adhesion layer is deposited and annealed at 420°C before using EUV SADP to pattern 18nm pitch lines into a non-sacrificial SiN hard mask, which is where the vias will be formed. The pattern is then transferred into the Ru using a highly selective RIE etching process. After post-etch cleaning, we fill between the lines with ALD SiO_2 before applying dielectric CMP to planarise the surface. Via patterning is done with EUV lithography. The via is bottom self-aligned in the remaining SiN on top of the metal line without attacking the SiO_2 gapfill using a highly selective gas chemical etch. The second Ru layer is then deposited by CVD which fills the via and will be patterned with single-print EUV lithography and etched to create lines. Top-via self-alignment is achieved by a Ru overetch step. Fig. 2 shows the final device.

Results and Discussion

A. *Leakage current* For MP18 devices the space between the lines is ~8nm. It is important to optimise the metal etch and ensure adequate post etch cleaning to remove leakage paths, including any remaining TiN from the adhesion layer. The leakage current measured from 1.1mm fork-fork devices with 18-26nm MP is shown (Fig. 3), achieving the target of < 1E11 $A\mu m^{-1}$. A TEM with EDS of 18MP structure is shown in Fig.4, confirming no metallic residues between the lines.

B. *Line resistance and resistivity.* By measuring line resistance through increasing temperature, we can use the TCR technique to measure the resistivity and resistance vs conductive area of the Ru lines. The resistivity of the PVD Ru after annealing is 14-15$\mu\Omega$.cm, and after etching we measure 13-15 $\mu\Omega$.cm (Fig. 5) indicating a damage-free integration. Line resistance vs conducting area of Ru is plotted together with Cu (Fig. 6). Ru outperforms Cu below 268nm^2, corresponding to line CD < 12nm. Furthermore, this is calibrated to physical area by applying image processing techniques to HAADF-TEM images (Table 1, Fig. 7). The measured conductive area matches the physical to within 2%, further indicating our etching process is damage free and that using barrierless Ru is an efficient option in BEOL.

C. *Via Resistance.* Modelling software indicates the via kelvin resistance is expected to be 40 < R < 60 Ω. Programmed via overlay structures show via resistance within the expected value with overlay error up to 5nm (Fig. 8a and b).

D. *Via Reliability.* Samples with 10nm injector and vias with 180nm^2 contact area underwent packaged EM testing and were stressed for 300 hours with 10MA/cm^2 without resistance change (Fig. 9), which is the expected value for Ru-Ru systems [6]. To enhance failures due to thermal diffusion, samples were stored at 200C and after 120h we see no R change or yield drop indicating no risk of void formation (Fig. 10). Furthermore, via to line breakdown at 100°C shows a breakdown field > 9MV/cm (Fig. 11), which is expected for 16nm SiO_2.

Acknowledgements We acknowledge Lam Research for collaboration on Ru etch.

References [1] V. Vega et al, "Three-Layer BEOL Process Integration with Super via and self-aligned block options for the 3nm node", IEDM 2019; [2] Murdoch et al; "Semidamascene Interconnects for 2nm node and beyond", IITC 2020; [3] Baert et al "Interconnect Design-Technology Co-optimization for Sub 3nm Technology nodes" IITC 2020;[4] Murdoch et al "Feasibility study for fully aligned via for 5nm node", IITC 2018; [5] Chen et al "Fully self-aligned via integration for interconnect scaling beyond 3nm node", IEDM 2021 [6] V. Vega Gonzalez et al, "21 nm pitch dual-damascene BEOL process integration with full barrierless Ru metallization", IEEE IITC 2019

Table 1: Area of 9nm CD Ru Lines

Measurement	Area (nm^2)
Nominal	270
Electrical	250
Physical	257

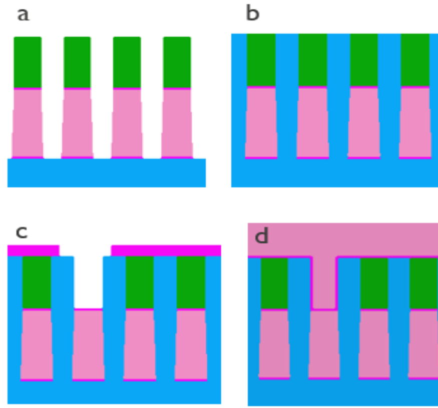

Fig 1 Semidamascene flow; a) Ru etch, b) gapfill, c) via etch, d) via fill and Mx+1 formation

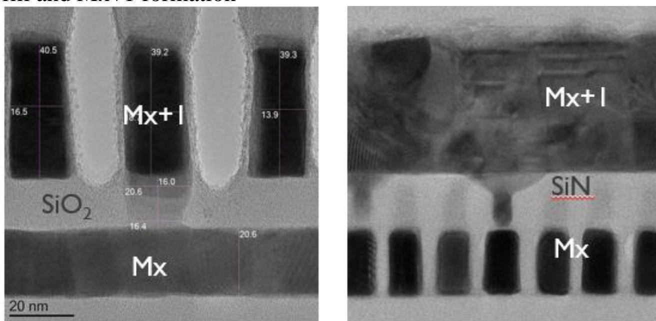

Fig 2: Self-aligned via along Mx (left) and across Mx (right)

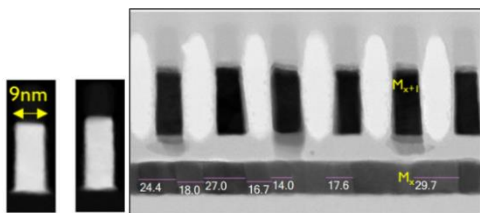

Fig 7: HAADF-TEM image of 9nm lines (left) and x-section of Mx line after 2ML integration (right)

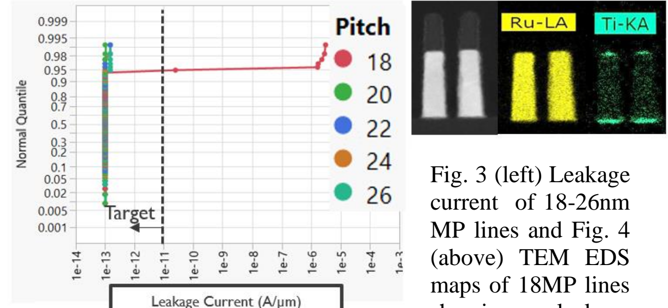

Fig. 3 (left) Leakage current of 18-26nm MP lines and Fig. 4 (above) TEM EDS maps of 18MP lines showing no leakage path.

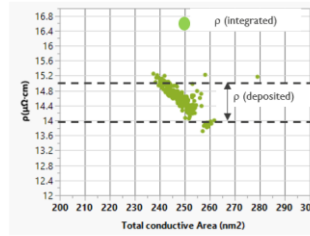

Fig. 5 Conductive area vs resistivity for 18-26MP Ru

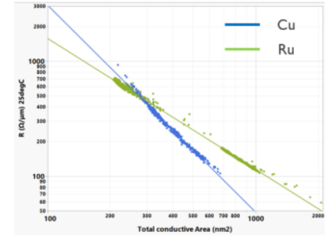

Fig. 6: Conductive area vs line resistance for Ru and Cu lines

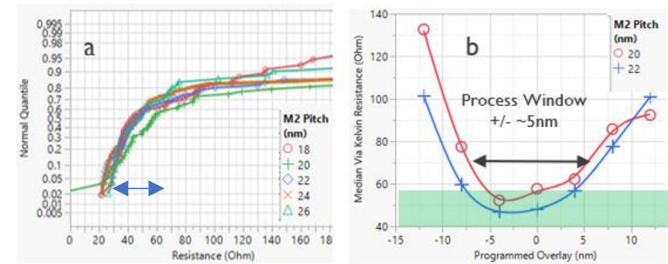

Fig 8 a) Via Resistance from 18-26nm MP and expected range and b) median via resistance vs programmed overlay for MP20 and 22nm.

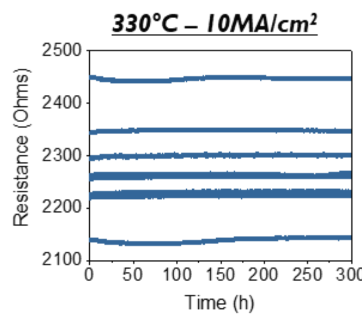

Fig. 9 left: EM measurements showing no R increase after 300 hours. Fig 10, bottom left: after 120 hours no R change or yield loss is observed; Fig 11, bottom right: Via-to-line breakdown > 16V for MP 26nm (or 16nm SiO_2)