Investigating Nanowire, Nanosheet and Forksheet FET Hot-Carrier Reliability via TCAD Simulations

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Invited Paper

***Abstract*—We report TCAD simulation studies on nanowire (NW), nanosheet (NS) and forksheet (FS) FET hot-carrier reliability. The simulations entail *i*) solving the Boltzmann transport equation to obtain the distribution of carriers over energy in the devices, *ii*) calculation of interface state generation at the channel/gate stack interface and charging of bulk defects in dielectrics, and *iii*) evaluation of how the generated/trapped charges affect the FET I-V. We discuss the models used in state-of-the-art hot-carrier simulation flows, anneal measurements to probe hot-carrier induced interface defects, the validity of the simulation models in the (V_g,V_d) bias space by comparing simulations to NW FET measurements and the conclusions the hot-carrier simulations provide for NS and FS FETs.**

***Index Terms*—Border traps, carrier energy distribution function, forksheet FETs, gate-all-around FETs, hot-carrier degradation, interface defects, nanosheet FETs, nanowire FETs, non-equilibrium BTI, non-radiative multiphonon model, recovery, Si-H bond, simulations, TCAD.**

I. Introduction

Since the formulation of Moore's law in 1965 [1], the semiconductor industry has roughly doubled the number of transistors per chip approximately every two years. While the path of simple geometric scaling [2] could be followed initially, transistor innovations like channel strain [3], high-k metal gates [4] and the finFET architecture [5] were needed in the last two decades to maintain the performance increase associated with scaling. For the upcoming technology nodes, a switch to gate-all-around devices, like nanowire (NW) and nanosheet (NS) FETs (Fig. 1a), is planned [6]–[9]. These devices offer ultimate electrostatic gate control and the potential to increase drive current by stacking multiple wires/sheets on top of each other. Also a forksheet FET architecture (Fig. 1a) was proposed [10], [11] and experimentally demonstrated [12], [13] recently. By stacking nFET and pFET sheets at opposite sites of a dielectric wall, FS FETs are more tolerant against processing inaccuracies and enable a reduction of the space between pFETs and nFETs (p-to-n separation). This allows to reduce logic cell area and/or to increase the FET width, increasing its drive current (area/effective width trade-off) [10].

Hot-carrier degradation (HCD) is a MOSFET aging mechanism active when the transistor is biased at high drain voltage.

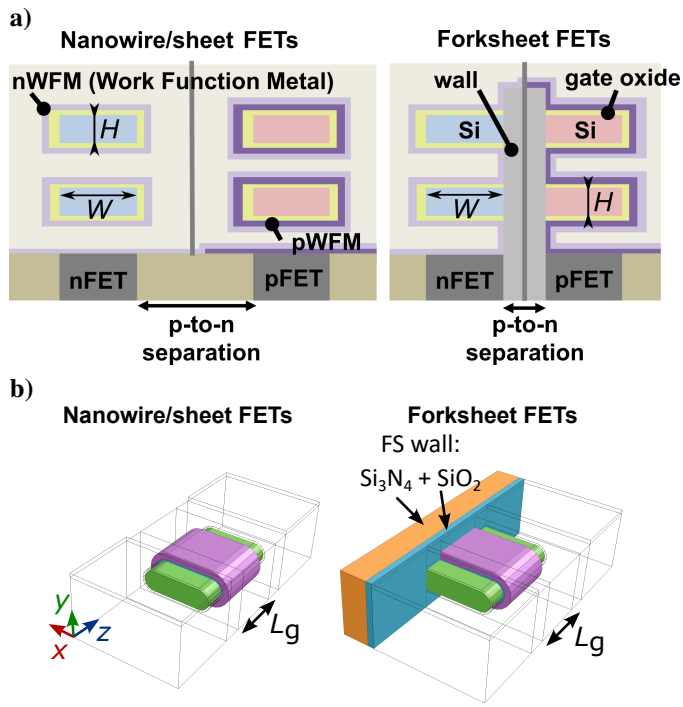

Fig. 1. a) Schematic cross-sections of the nanowire/sheet (NW/NS) and forksheet (FS) FET architectures. Due to the presence of a dielectric wall in the FS FET structure, pFETs and nFETs can be placed closer together in this architecture (reduction of the p-to-n separation). b) Simplified simulation structures used in this work containing the essential features of the NS and FS FET architecture. Only the nFET sheets are simulated.

HCD manifests itself as a gradual shift of I-V parameters (threshold voltage V_{th}, maximum transconductance $g_{\mathrm{m,max}}$, subthreshold swing SS, drain current I_{d}) during stress [14]. The performance degradation is caused by defects created by highly energetic (= hot) carriers (HCs). The defects are mostly interface defects at the Si/SiO_2 interface (P_{b}-centers or broken Si-H bonds) [14]–[18], although charging of traps in the gate dielectric has been reported too [15], [19]–[21]. Typically, the HC-induced defects are localized at the drain, as this is where the electric field peaks in saturation [15], [22], [23].

Because HCD is a reliability problem of growing concern in the latest technology nodes [24], [25], understanding HC aging is crucial. HCD simulations can help to interpret experimental data from fabricated devices and to gain insight in the HCD of future devices early on in the technology development. Here, we summarize our recent simulation activities for HCD in NW, NS and FS FETs. First, we give a brief overview of the evolution of HCD models. Then, we discuss the methodology of the HCD simulations. Next, we explain how hot-carrier anneal measurements can provide insights into the defect models used in the simulations. Finally, we discuss three HCD simulation case studies for future technologies: *i*) $(V_\mathrm{g}, V_\mathrm{d})$ maps for NW FETs, *ii*) impact of dimensions on NW/NS and FS FET HCD and *iii*) trapping of charges in the FS FET wall.

II. Evolution of hot-carrier degradation models

The most well-known HCD model is the lucky electron model (LEM) [14], [26]–[28]. It was developed in the 1980s for transistors with gate length $L_\mathrm{g} \sim 1\ \mu$m. The model describes in the first place the gate current resulting from HC injection. In order for a carrier to get injected into the gate oxide and to contribute to the gate current, it needs to be 'lucky' enough to survive a series of events. These events are: acquiring the energy needed to overcome the Si-SiO_2 barrier φ_b, undergoing a scattering event to redirect the carrier's momentum towards the interface, and traveling to the interface and in the oxide without scattering. The probabilities of these events can be estimated using the result of Shockley [29] that the probability for a carrier to travel a distance d without collisions is given by $\exp(-d/\lambda)$, with λ the scattering mean free path. The gate current I_g then becomes $I_\mathrm{g} \sim I_\mathrm{d} \exp(-\varphi_\mathrm{b}/(qF_\mathrm{m}\lambda))$, with I_d the drain current, q the elementary charge and F_m the peak electric field.

The LEM also describes the substrate current and interface state generation during HC stress using similar expressions. By relating all the formulas, one obtains the result $\mathrm{TTF} \times I_\mathrm{d}/W \sim (I_\mathrm{sub}/I_\mathrm{d})^{-\varphi_\mathrm{it}/\varphi_\mathrm{i}}$ [14]. This expression allows to extrapolate times-to-failure (TTFs) from stress to use conditions and states that the charge through the device per unit width W at device failure is a power law of the multiplication factor $(I_\mathrm{sub}/I_\mathrm{d})$. The exponent is given by the ratio of the energy threshold φ_it for interface state generation over the energy threshold φ_i for impact ionization. Another, more empirical lifetime extrapolation model was proposed by Takeda and Suzuki [30] around the same time: $\mathrm{TTF} \sim \exp(b/V_\mathrm{d})$. It states that the TTF depends exponentially on the inverse of the drain voltage V_d, with b a constant.

The scaling of the chip supply voltages accompanying the dimensional transistor scaling led to deviations from the LEM around the year 2000. In the LEM, a single carrier breaks the Si-H bond. As such, the carrier needs to have an energy $\varphi_\mathrm{it} \sim 3.7$ eV to create an interface state [14]. However, HCD continued to be observed for drain voltages below this threshold energy. Hess, McMahon and coworkers [31]–[33] argued that, besides the single particle (SP) mechanism of Si-H bond breakage, also multiple carriers can break Si-H bonds. This was motivated by STM experiments of H desorption [34]. In the multiple particle (MP) mechanism, many less energetic carriers collide with the bond and induce its vibrational excitations. When the bond vibrational energy is sufficiently high, the bond eventually breaks.

Rauch and co-workers [35], [36] argued instead that interface state generation at low voltages still occurs through bond breakage by a single carrier. However, this carrier can gain an energy exceeding the supply voltage through electron-electron scattering (EES) and in this way reach the threshold energy for Si-H bond breakage. Rauch and La Rosa [37] further changed the paradigm of HCD. They argued that at reduced operating voltages, HCD is energy-driven, contrary to being field-driven, as in the LEM. Instead of the peak electric field, integrals of the carrier energy distribution function multiplied by the appropriate interaction cross section govern HCD.

Guérin, Bravaix and co-workers [38], [39] combined the SP mechanism, the MP mechanism, EES and the energy-driven paradigm in an updated lifetime extrapolation model. The model (or small variations thereof) was shown to successfully describe HCD in many scaled technologies, including 40 nm planar FETs [40], 28 nm planar FETs [41] and NW FETs [42], [43]. In the model, TTF's determined by the SP mechanism of interface state generation (possibly with the help of EES) show an exponential dependence on $(V_\mathrm{d} - V_\mathrm{d,sat})^{-1}$, with $V_\mathrm{d,sat}$ being the saturation drain voltage. The TTF's determined by the MP mechanism of interface state generation show a power-law dependence on the drain current [39], [42].

The above models describe HCD using macroscopic quantities, e.g. the substrate and drain currents. These macroscopic quantities serve as proxies for internal transistor variables, e.g. the peak electric field in case of the LEM. Another class of models, here called 'microscopic' HCD models, consider the same physical effects as the above 'macroscopic' models, but directly calculate the microscopic quantities (e.g. electric fields, carrier energy distribution functions, defect profiles) governing HCD. Microscopic HCD models (usually) rely on Technology Computer-Aided Design (TCAD) software. Recent contributions to TCAD simulations for HCD were made by e.g. Bottini *et al.* [44], Jech *et al.* [45], Makarov *et al.* [46], [47], Randriamihaja *et al.* [48], Reggiani *et al.* [49], Sharma *et al.* [50] and Tyaginov *et al.* [51], [52]. The simulations reported here are part of the 'microscopic' HCD models.

III. Methodology

A TCAD simulation flow for HCD consists of three steps (Fig. 2). First, the Boltzmann transport equation (BTE) is solved for the $(V_\mathrm{g}, V_\mathrm{d})$ stress conditions under consideration. As input of the first step, a simulation structure (Fig. 1b) of the transistor is needed, together with a modeling of the time-0 I-V curve. The result of the first step is the carrier energy distribution function (DF) $f(E)$, which gives for every point in the device the probability of finding a carrier there at energy E (Fig. 3). We solved the BTE using the GTS NDS solver [53] (Section V) and using the ViennaSHE solver [54] (Sections VI

and VII). All devices simulated in this work are nFETs. For the FS FET, the pFET on the other side of the dielectric wall is not considered (Fig. 1b).

In the second step, the degradation is calculated. We consider interface defects at the Si/SiO$_2$ interface and in Section VII also charging of defects in the gate and (FS FET) wall dielectrics. The evolution as function of time t and at every position $\vec{r}$ of the fraction $P_{\rm it}(\vec{r},t)$ of created interface defects and the occupancy $P_{\rm ot}(\vec{r},t)$ of the dielectric traps is governed by first order kinetics [55], [56]:

$$P_{\rm it}(\vec{r},t) = 1 - \exp\left(-k_{\rm d}(\vec{r})t\right) \quad (1)$$

$$P_{\rm ot}(\vec{r},t) = \frac{k_c(\vec{r})}{k_e(\vec{r}) + k_c(\vec{r})}\left(1 - \exp[-(k_e(\vec{r}) + k_c(\vec{r}))t]\right), \quad (2)$$

with $k_{\rm d}$ the Si-H bond dissociation rate and k_e (k_c) the electron emission (capture) rates. Note that the formula for $P_{\rm ot}$ is for acceptor traps (negatively charged upon charge capture), and that we assume no interface defects or bulk trap occupation at $t = 0$ s. The rates $k_{\rm d}$, k_e and k_c are calculated from the DF and the defect properties, as will be explained next.

The interface defect precursors are Si-H bonds. As explained in Section II, two modes of Si-H bond breakage are observed in current technologies, namely the SP and the MP mechanism. The Si-H bond vibrational states are modeled using a truncated harmonic potential (Fig. 4a). The vibrational energy of the bond can increase or decrease with the rates $k_\uparrow$ and $k_\downarrow$, respectively. From each vibrational state i, bond breakage is possible with a rate $r_{\rm i}$. The total bond breakage rate $k_{\rm d}$ is then simply the weighted sum of the rates $r_{\rm i}$:

$$k_{\rm d} = \frac{1}{M}\sum_{i=0}^{N-1}\left(\frac{k_\uparrow}{k_\downarrow}\right)^i r_{\rm i} \quad \text{with} \quad M = \sum_{i=0}^{N-1}\left(\frac{k_\uparrow}{k_\downarrow}\right)^i, \quad (3)$$

with N the number of vibrational states (levels). The rates $k_\uparrow$, $k_\downarrow$ and $r_{\rm i}$ are the sum of the acceleration integral (AI), representing the contribution to the rate by incident (hot) carriers, and an Arrhenius term, representing the lattice or thermal contribution to the rate. The AIs I are calculated from the DF:

$$I(\vec{r}) = \sigma_0 \int_{E_{\rm th}}^{\infty} f(\vec{r},E)v(E)D(E)\left(\frac{E - E_{\rm th}}{1\ \text{eV}}\right)^p {\rm d}E, \quad (4)$$

with σ_0 the scattering cross section, $E_{\rm th}$ the minimum energy a carrier needs to contribute to the rate, v the carrier velocity, D the density-of-states (DOS) and p an exponent ($p = 1$ for $k_\uparrow, k_\downarrow$ and $p = 11$ for $r_{\rm i}$). We refer to Tyaginov *et al.* [55] and Vandemaele *et al.* [57] for all details on the interface state generation model.

For the bulk dielectric traps, a two-state non-radiative multiphonon (NMP) model is used (Fig. 4b). We explain the model from the viewpoint of acceptor traps capturing or emitting an electron. The energy landscape between the state q_1 with the electron trapped on the defect and the state q_2 with the electron in the carrier reservoir (e.g. the conduction band) is approximated by two parabolas. The parabolas are parametrized by the energy difference ΔE_{12} between their minima, the relaxation energy S and the curvature ratio R. To get trapped in (emitted from) the defect, the electron does not need to overcome the energy difference ΔE_{12} between the reservoir and the defect site, but rather the barrier $\epsilon_{\rm c}$ ($\epsilon_{\rm e}$), which includes the phonon-mediated deformation of the lattice and subsequent relaxation to equilibrium upon charge capture (emission). The rates k_e and k_c are given by [60]:

$$\left.\begin{matrix} k_e \\ k_c \end{matrix}\right\} = v_{\rm th}\sigma_0 \int_{E_c}^{\infty} {\rm d}E\ D(E)\theta(E) \times \exp\left(-\frac{\epsilon_{\rm e/c}}{k_{\rm B}T}\right)\left\{\begin{matrix}(1 - f(E)) \\ f(E)\end{matrix}\right., \quad (5)$$

with $v_{\rm th}$ the electron thermal velocity, σ_0 the electron capture

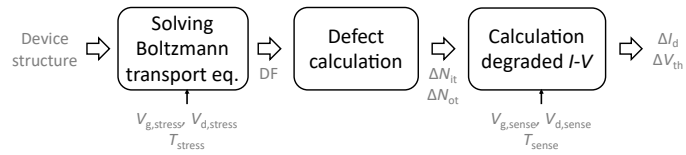

Fig. 2. TCAD simulation flow for HCD simulations.

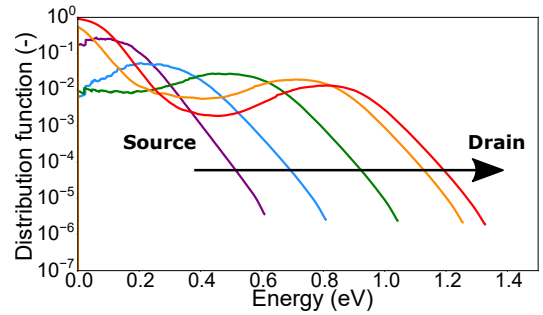

Fig. 3. Example of carrier energy distribution functions for an n-channel NW FET with $L_{\rm g} = 28$ nm stressed at $V_{\rm g} = 1.9$ V and $V_{\rm d} = 1$ V. The different colors represent different positions along the channel. When moving from source to drain, carriers reach higher energies (from [58]).

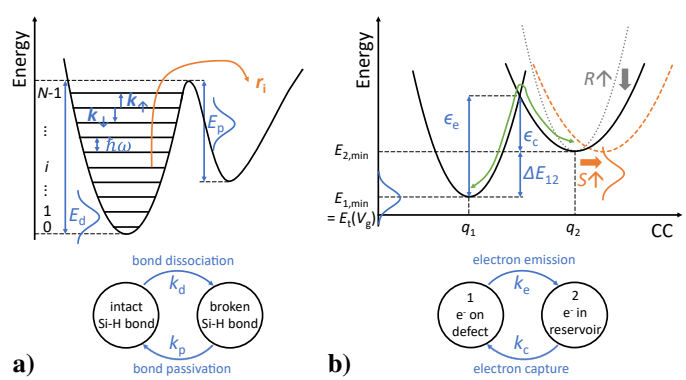

Fig. 4. Model for a) interface state generation through Si-H bond breakage and b) charging of bulk defects in the gate or FS FET wall dielectrics through non-radiative multiphonon transitions.

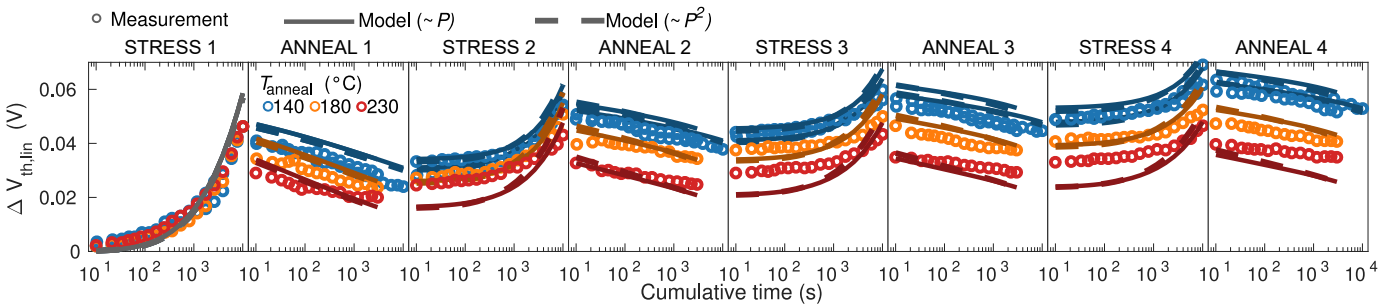

Fig. 5. Multiple HC stress/anneal cycles repeated on the same devices for three anneal temperatures. The measured data is modeled assuming distributed Si-H bond dissociation and passivation energies. Two variants of the model are considered [namely with a passivation term during stress linearly ($\sim P$) and quadratically ($\sim P^2$) depending on the fraction of created defects P], but no difference between the two models could be observed based on the available data. Note that the fits (solid and dashed lines) were done on five stress/anneal time scenarios together (i.e. on four extra scenarios compared to the one shown here) and that stress was always done at room temperature (from [59]).

cross section, E_c the conduction band edge, $\theta(E)$ the tunneling probability (using the Wentzel–Kramers–Brillouin approximation), k_B the Boltzmann constant and T the temperature. We refer to Rzepa *et al.* [61] and Jech *et al.* [62], [63] for all further details on the model.

The charged interface (bulk) defect density N_it (N_ot) is then $N_\mathrm{it} = P_\mathrm{it} N_\mathrm{T,it}$ ($N_\mathrm{ot} = P_\mathrm{ot} N_\mathrm{T,ot}$), with $N_\mathrm{T,it}$ ($N_\mathrm{T,ot}$) the maximum interface defect density (maximum density of pre-existing traps in the dielectric). Instead of being single valued, some defect properties (the bond breakage energy E_d in case of interface defects, and the trap energy level E_t and relaxation energy S in case of bulk defects, see Fig. 4) follow a Gaussian distribution. The density of generated/charged defects is then obtained by taking the weighted average over all possible values of the defect property, e.g. for interface defects:

$$N_\mathrm{it}(\vec{r},t) = N_\mathrm{T,it} \int_0^\infty g_\mathrm{d}(E_\mathrm{d}) P_\mathrm{it}(E_\mathrm{d},\vec{r},t) \mathrm{d}E_\mathrm{d}, \qquad (6)$$

with $g_\mathrm{d}(E_\mathrm{d})$ the Gaussian distribution of bond dissociation energies with mean $\mu(E_\mathrm{d})$ and standard deviation $\sigma(E_\mathrm{d})$.

In the third step (i.e. the post-stress simulation), the interface and bulk dielectric defect profiles are placed back in the device structure and their influence on the I-V curve (compared to the time-0 I-V) is calculated. We consider the electrostatic impact of both interface and bulk defects by including them in the Poisson equation. Mobility degradation is only taken into account for the interface defects.

IV. Probing Hot-Carrier Induced Defects Using Anneal Measurements

The defects involved in HCD and modeled in the second step of the simulation flow of Fig. 2 can be studied separately using HCD anneal measurements. In these experiments, HCD can be (partially) recovered by a treatment at elevated temperatures [64]–[67]. At room temperature, HCD is normally quasi-permanent. We performed high-temperature HCD anneal on custom-built chips containing arrays of nFETs and designed in a commercial bulk 40 nm CMOS technology. The temperature increase was obtained using on-chip poly-Si heaters. The

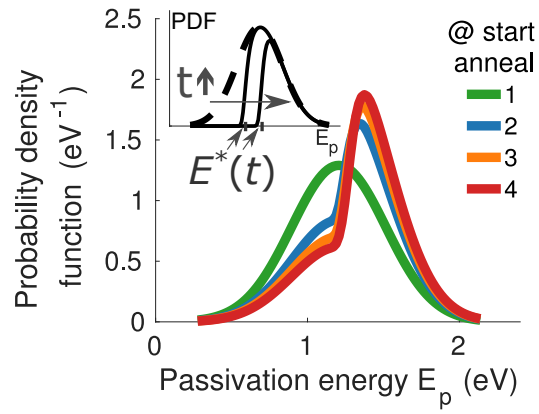

Fig. 6. Distribution of the bond passivation energies at the start of every anneal phase ($T_\mathrm{anneal} = 180$ °C) for the measurement in Fig. 5 as derived from the model fit. At the start of the first anneal phase, the distribution is Gaussian, but not at the start of later anneal phases. The inset shows the evolution with time of the bond passivation energy distribution during the first anneal phase, implying that the lowest passivation energies are annealed first (from [59]).

devices were stressed so that the damage consists of interface defects. We can thus probe the return path with passivation rate k_p in the oscillator model of Fig. 4a using the anneal measurements. We refer to [59], [68] for all details.

We focus on *multiple* HC stress and anneal cycles which are repeated (up to four times) on the same device (= cycled HCD anneal, Fig. 5) [59]. Pobegen *et al.* [64] and de Jong *et al.* [66] showed that *single* cycle HCD anneal can be described using the model of Stesmans [69] for passivation of P_b-defects (dangling Si-bonds) in molecular H_2. This suggests that the recovery of HCD during the anneal is due to a repassivation of the Si-H bonds which were broken during stress. In the Stesmans model, the Si-H bond passivation energy is not single-valued, but follows a Gaussian distribution. This passivation energy distribution is caused by the underlying spread in atomic defect configurations and is similar to the distribution in dissociation energies as described in (6). For the cycled HCD anneal measurements, we extended the Stesmans model to also describe the stress phases, resulting in a bivariate

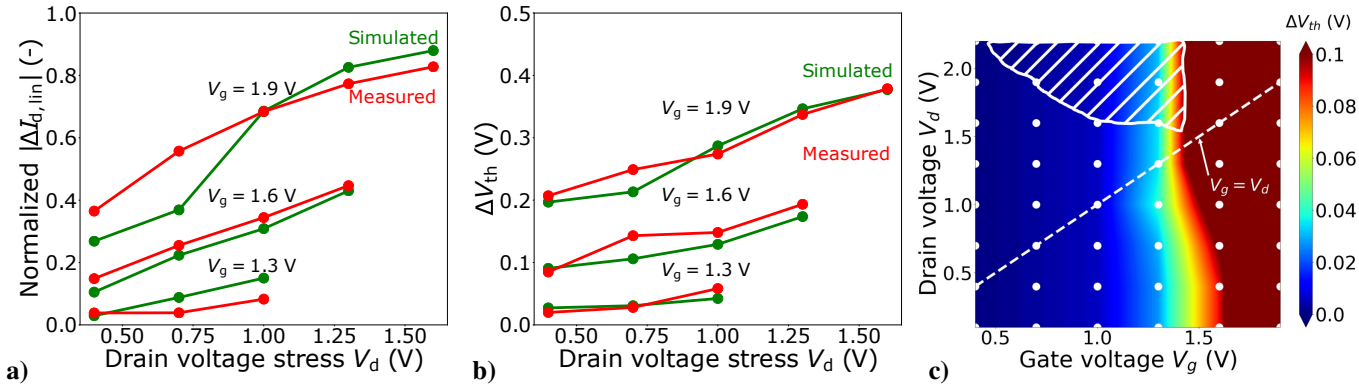

Fig. 7. a)-b) Comparison between the simulated and measured HCD for a fabricated NW FET for stress conditions with $V_g > V_d$. The simulations follow the scheme in Fig. 2 and do not include impact ionization. Good agreement between measurements and simulations is obtained in the bias region $V_g > V_d$. c) Simulated HCD for the same NW FET and using the same settings as in a)-b), but now over the full (V_g, V_d) stress bias space. For $V_g < V_d$, discrepancies between the measurements and simulations appear. In particular, the hatched region shows degradation in the measurements and this degradation is missing in the simulations (from [58]).

Gaussian distribution for both the dissociation and passivation energies (Dissociation/Passivation Energy (DPE) map model, see [59]).

From the DPE map model fit to experimental data (Fig. 5), we obtain two insights on the HC-induced interface defects and their Si-H bond precursors. First, we observe that there is no correlation between Si-H bond dissociation energies E_d and passivation energies E_p (correlation factor $\rho < 10^{-2}$) [59]. This means that bonds which are easy to dissociate can be equally easy or hard to passivate. Second, we observe that the distribution of bond passivation energies (obtained after integrating out the bond dissociation energies from the DPE map distribution) is Gaussian at the start of the first anneal phase (as in the Stesmans model for *single* cycle HCD anneal), but not anymore at the start of later anneal phases (Fig. 6). The explanation is that during the HCD anneal, the bonds are passivated from low to high passivation energies (inset of Fig. 6). Consequently, there is a demarcation energy $E^*(t)$ which increases with time t and below (above) which all bonds are passivated (unpassivated). During the stress following the anneal, the same happens with the bond dissociation energies, i.e. the weakest bonds are dissociated first. However, as there is no correlation between bond dissociation and passivation energies, both low ($E_p < E^*$) and high ($E_p > E^*$) passivation energies are added to the passivation energy distribution. Together with the remaining high ($E_p > E^*$) passivation energies from the previous anneal phases, this results in an asymmetric (non-Gaussian) passivation energy distribution from the second anneal phase on.

V. (V_g, V_d) maps for nanowire FETs

As the first case study, we simulate HCD for fabricated NW FETs over the full (V_g, V_d) stress bias space using the flow of Fig. 2 and we compare the simulations to the measured degradation. The goal is to study which physical effects need to be considered in which part of the (V_g, V_d) bias space. We consider interface defect generation through the models discussed in Section III. We include oxide defects, but we

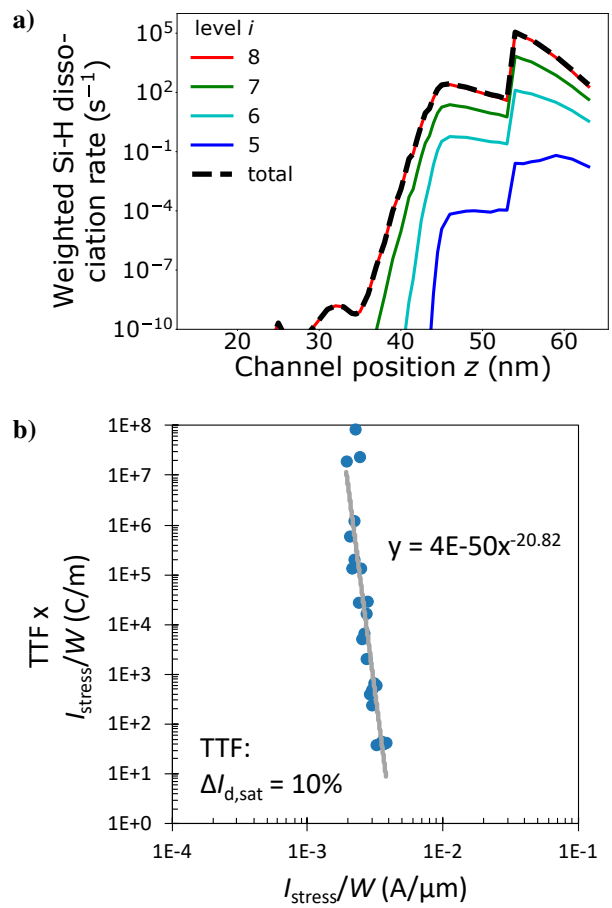

Fig. 8. a) Si-H bond dissociation rate r_i from every vibrational state i of the bond weighted by the occupancy of the vibrational state for the NW FET of Fig. 7 in the $V_g > V_d$ bias region ($V_g = 1.9$ V, $V_d = 1$ V). Dissociation occurs from the highest ($i = 8$) vibrational state (from [70]). b) Simulated dependence of the times-to-failure (TTFs) for the NW FET of Fig. 7 in the $V_g > V_d$ bias region. The TTFs line up as function of the stress current. Both a) and b) show that the NW FET degradation for the stress condition $V_g > V_d$ is due to the MP mechanism.

calibrate their occupancy to the measured ΔV_{th} at $V_{\mathrm{d}} = 0.1$ V for the simulated stress time, i.e. we do not include their charging kinetics. We account for phonon, ionized impurity and surface roughness scattering in the calculation of the DF, but not for impact-ionization (I/I) as this effect was not implemented yet in the BTE simulator at the moment of the simulations below. We refer to [58], [70] for all simulation details. The experimental data was measured by Chasin *et al.* [43].

For $V_{\mathrm{g}} > V_{\mathrm{d}}$, good agreement between the simulated and measured degradation could be obtained without considering I/I for the solution of the BTE (Fig. 7a-b). The degradation in this stress region is due to the MP mechanism. This can be concluded from the internals of the simulations when plotting the total Si-H bond breakage rate and the contributions to it from the different vibrational states (Fig. 8a). Since the total Si-H bond breakage rate coincides with the bond breakage rate from the highest vibrational level, the MP mechanism dominates. When simulating the times-to-failure (TTFs) for different bias points with $V_{\mathrm{g}} > V_{\mathrm{d}}$, the TTFs align as a function of stress current (Fig. 8b). This behavior is also experimentally observed for the MP mechanism [42] and is another indication that the MP mechanism dominates the degradation for $V_{\mathrm{g}} > V_{\mathrm{d}}$.

For $V_{\mathrm{g}} < V_{\mathrm{d}}$, the simulations underestimate the measured HCD (Fig. 7c). The high V_{g} (≥ 1.3 V) points in this region show partially missing degradation in the simulations, while the low V_{g} points show no degradation at all in the simulations, in contrast to the measurements (see hatched region in Fig. 7c). Analysis of the interface defect profiles [70] for low V_{g} values shows that defects are generated in the simulations for these stress conditions, but that they are located in the drain extension region. As the extension regions are not covered by the gate, defects there have little influence on the I-V.

We hypothesized that the missing degradation in the simulations is due to the absence of I/I in the DF calculation. The holes generated by I/I will travel to the source and can create defects deeper in the channel (away from the drain), leading to I-V degradation. This hypothesis was tested by including in the simulations interface defects generated by holes from I/I with an analytical, heated Maxwellian hole DF [70]. The hole DF was constructed using hole temperature profiles obtained from hydrodynamic simulations. Although being a strong simplification, the approach gave good agreement between measured and simulated degradation for selected bias points in the region of missing degradation. A more rigorous approach consisting of numerically solving the BTE for holes (combined with the one for electrons) over the full $(V_{\mathrm{g}}, V_{\mathrm{d}})$ bias space gave degradation in the region where degradation was missing originally, but an exact quantitative agreement between measurements and simulations could not be obtained yet (not shown).

We conclude from the simulations in this section that the simulation flow of Fig. 2 without I/I can model HCD for stress conditions with $V_{\mathrm{g}} > V_{\mathrm{d}}$.

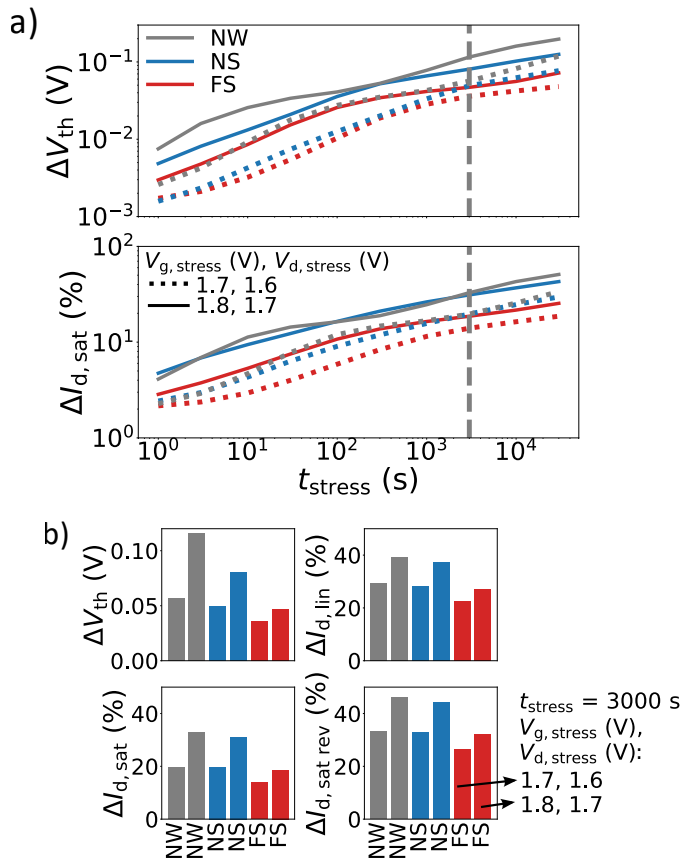

Fig. 9. I-V degradation due to interface defect generation by HC stress for a NS and a FS FET with dimensions from the *imec* roadmap a) as function of stress time and b) for a fixed stress time. In the roadmap, the FS FET is wider ($W = 21$ nm) compared to the NS FET ($W = 14.5$ nm) due to the reduced p-to-n separation of FS FETs. A NW FET with a diameter typical of fabricated NW FETs was added to the comparison (from [57]).

VI. Impact of Dimensions on Nanowire/Nanosheet and Forksheet FET Hot-Carrier Degradation

As the second case study, we simulate the impact of changing the NW/NS and FS FET width W on the HCD of these architectures using the simulation flow of Fig. 2 (see Fig. 1a for the definition of the sheet width W). This is of relevance as the reduced p-to-n separation of the FS FET allows for a cell area versus effective width trade-off [10]. We consider stress biases $V_{\mathrm{g}} \sim V_{\mathrm{d}}$ (with still $V_{\mathrm{g}} > V_{\mathrm{d}}$) as they constitute the worst case HC stress condition for scaled technologies [71]. Including interface state generation by electrons only is sufficient for these conditions, as explained in Section V. We refer to [57] for all details.

We first compare one NS and one FS FET with dimensions from the *imec* roadmap. There, the FS FET is wider ($W = 21$ nm) compared to the NS FET ($W = 14.5$ nm) because of the reduced p-to-n separation of the former. We observe a lower degradation of the FS FET compared to the NS FET (Fig. 9). When looking into the internals of the simulations, we see that the curved part of the FET cross-section (CS) shows a higher density of generated interface

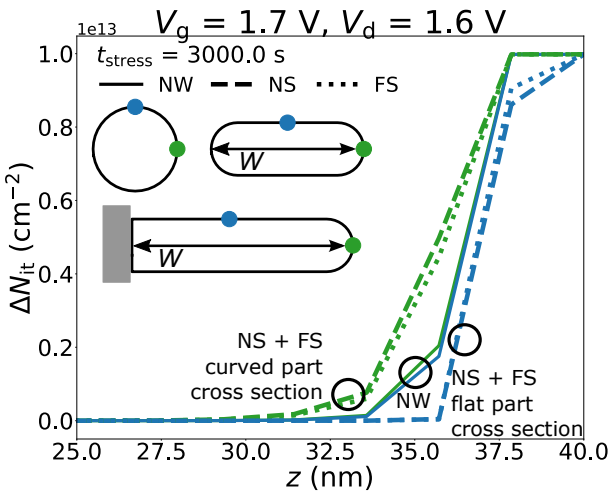

Fig. 10. Interface defect profiles causing the I-V degradation in Fig. 9. For both the NS and FS FET, the curved part of the cross section (green curves) has a higher density of generated defects compared to the flat part of the cross section (blue curves). As the FS FET is wider than the NS FET, the less degrading flat part of the cross-section contributes relatively more for the FS FET. The generated interface defect density of the NW FET is independent of the position along the cross-section, as the NW FET has cylindrical symmetry (from [57]).

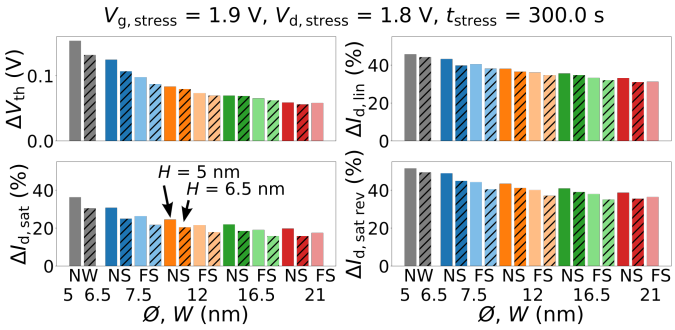

Fig. 11. I-V degradation due to interface defect generation by HC stress as in Fig. 9, but now for NS and FS FETs of varying widths and two heights, allowing to compare NS and FS FETs of the same width. Note that the devices (e.g. EOT, doping profile) are different as compared to the ones in Fig. 9 (from [57]).

states compared to the flat part of the CS (Fig. 10). This higher density of generated interface defects in the curved part of the CS could be explained by the higher oxide electric field and corresponding higher carrier concentration and bond preheating there [57]. Since the FS FET is wider than the NS FET, the less degrading flat part of the CS contributes relatively more for the FS FET, explaining its lower I-V degradation. We also included a NW FET with a radius typical for fabricated NW FETs in the comparison (Fig. 9). Since this device has cylindrical symmetry, the interface defect profile is independent of the position along the CS (Fig. 10). When comparing NS and FS FETs of the same width (Fig. 11), the degradation is very similar for both device types. The FS FET has slightly lower degradation than the NS FET and this difference disappears with increasing width.

VII. Trapping in the Forksheet FET Wall

As the third case study, we simulate the spatial profile of charges trapped in the FS FET wall after HC stress and the resulting I-V degradation. Since the intended material for the FS FET wall is SiN, a material currently used as charge trapping layer in non-volatile memories [73], FS wall trapping is a potential concern. We again consider stress bias points $V_g \gtrsim V_d$ and model the charge trapping using the two-state NMP model discussed in Section III. Because not all charge trapping data for SiN are known in the literature, we use the values of SiO_2 for the relaxation energy S (both its mean value $\mu(S)$ and standard deviation $\sigma(S)$) and for the curvature ratio R. We then estimate the sensitivity of the I-V degradation to these parameters by varying them $\pm$ 20% around the SiO_2 value. The SiN trap energy E_t (both its mean value $\mu(E_t)$ and standard deviation $\sigma(E_t)$) and the trap density $N_{T,ot}$ could be fixed using SiN data from charge trap flash memories [74]. We refer to [72] for all details on the simulations.

Fig. 12 shows the simulated occupancy profile of traps in the FS FET wall after HC stress at $V_g = 1.7$ V and $V_d = 1.6$ V. *First*, we observe that charge trapping above ($y > 2.5$ nm) and below ($y < -2.5$ nm) the horizontal projection of the sheet in the wall is possible. *Second*, we see that the maximum of the occupancy profile (in the depth = x-direction) is not necessarily at the channel/wall interface, but can be at a certain distance away from the interface. Both observations can be explained from the band bending profile in the FS FET wall [72]. *Third*, the defect occupancy is higher at the drain compared to the source side. This is a consequence of the HC stress (non-zero V_d), which is known to result in degradation localization at the drain [15], [22], [23]. *Fourth*, we find the occupancy profile to be independent of the sheet width.

Fig. 13a shows I-V degradation caused by the occupancy profiles in Fig. 12. We observe that I-V degradation due to FS FET wall charging decreases with increasing width (Fig. 13a), despite the occupancy profiles being independent of the width. This can be understood considering that wider FETs have a larger part of the channel further away from the wall and hence are less affected by the same FS FET wall charge. The I-V degradation is larger for the taller sheet height. From Fig. 12d, we see that the defect occupancy is highest at the drain and is height-independent there. This implies that the taller height has more defects in the wall, leading to larger I-V degradation.

Finally, we also compare I-V degradation due to trapping in the FS FET wall with I-V degradation due to trapping in the gate stack under the same stress conditions (Fig. 13b). For the largest FS FET wall I-V degradation (smallest $W = 7.5$ nm, tallest $H = 6.5$ nm), the gate stack charging is still $\sim 4\times$ higher than the FS wall charging, under the assumption that the unknown SiN charge trapping parameters are 20% worse than the ones of SiO_2. For the FS FET with dimensions from the *imec* roadmap ($W = 21$ nm, $H = 5$ nm), the difference between gate stack charging and wall charging under the same assumption is approximately one order of magnitude.

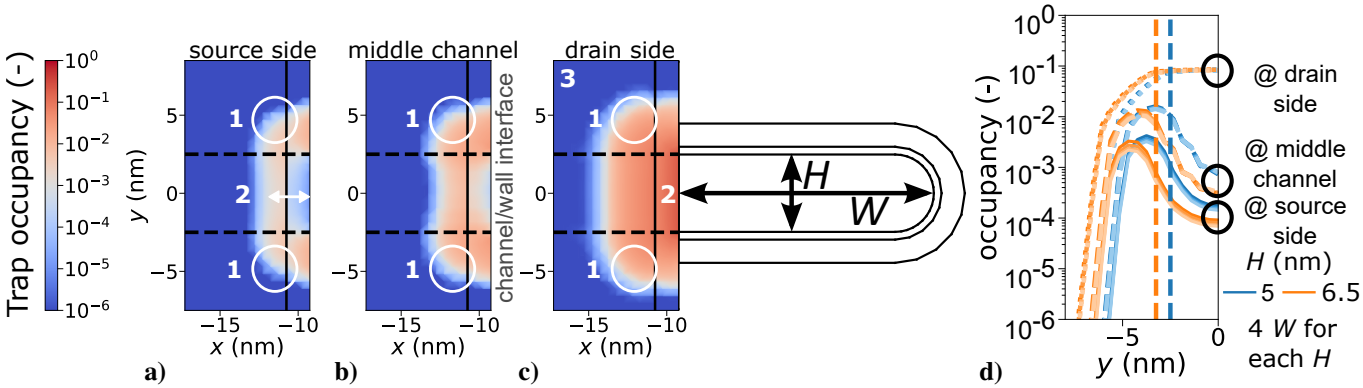

Fig. 12. a)-b)-c) Trap occupancy profile in the FS FET wall after HC stress at $V_g = 1.7$ V, $V_d = 1.6$ V and $t = 1$ ks for three positions along the channel and one W, H combination ($W = 21$ nm, $H = 5$ nm). The silicon sheet is always to the right of the cross-section, but is only shown for cross-section c). The numbers refer to peculiarities of the profile discussed in the text. d) Cutline of the trap occupancy profile along the y-axis at a depth of 1 nm in the wall for two sheet heights ($H = 5, 6.5$ nm, blue and orange colors, resp.), four sheet widths ($W = 7.5, 12, 16.5, 21$ nm, different shades of the colors, lines are overlapping) and the same stress condition as in a)-b)-c). Note that the profile is symmetric around $y = 0$ nm. The occupancy profile is independent of the sheet width (from [72]).

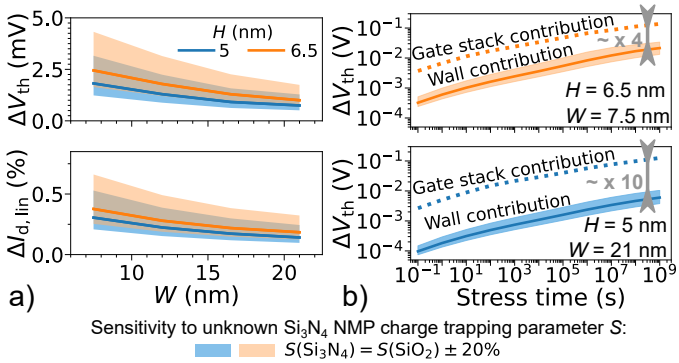

Fig. 13. I-V degradation due to the FS FET wall trap occupancy profiles in Fig. 12d. The shaded bands indicate the change in I-V degradation for the case of the unknown SiN charge trapping parameter S having a value which is 20% smaller or larger than the value for SiO_2. The sensitivity of the I-V degradation to the unknown SiN charge trapping parameter R was smaller than the sensitivity to the parameter S and is therefore not shown (from [72]).

Therefore, we do not expect charging of defects in the FS FET wall to be a serious reliability concern for FS FETs.

The limited contribution of FS FET wall charging to the total HCD observed here in simulations is consistent with the experimental work of Bury *et al.* [75] and Ritzenthaler *et al.* [76]. Both authors assessed the reliability of FS FETs and NS FETs co-integrated on the same wafer, with Bury *et al.* focussing on bias temperature instabilities (BTI) and HCD, and Ritzenthaler *et al.* on BTI and time-dependent dielectric breakdown (TDDB). They found no significant differences in reliability between both device types. This suggests that FS FET wall charging does not have a major impact on the total degradation, as the wall is the main difference between both (co-integrated) architectures.

VIII. Conclusions

We performed HCD simulations in the energy picture of devices in future technology nodes. The simulations relied on numerically solving the Boltzmann transport equation (BTE) to obtain the carrier energy distribution function. For the defects, a truncated harmonic oscillator model for the interface state precursors and a two-state non-radiative multiphonon model for bulk dielectric traps were used. We also showed how high temperature HCD anneal measurements can give insights on the interface state defects.

By comparing the simulated degradation to measured HCD for fabricated NW FETs, we conclude that solving the BTE without the inclusion of impact ionization is sufficient for the bias conditions $V_g > V_d$. The FS FET architecture shows lower HCD in comparison to the NS FET geometry when considering roadmap dimensions and the worst-case hot-carrier stress condition. We do not foresee FS FET wall charging during hot-carrier stress to be a serious reliability concern, as concluded from the comparison of the magnitude of trapping in the FS FET wall versus trapping in the gate stack.

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