Calibrated fast thermal calculation and experimental characterization of advanced BEOL stacks

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Abstract— **In this work, we present a fast evaluation methodology to aid the thermal-aware BEOL design with a quick estimation of out-of-plane layer equivalent thermal properties based on design rules for dimensions and densities. The method is calibrated with a detailed FE thermal simulation and is applicable to realistic back-end-of-line (BEOL) connectivity. With this method, a breakdown analysis is performed on an advanced 3 nm 14-layer BEOL stack. Thermal contributions of individual layers and impacts of dielectric and metallization choices are benchmarked. Furthermore, a dedicated multi-layer BEOL test vehicle is designed in a 28nm foundry CMOS technology. The out-of-plane thermal coupling is experimentally characterized, and consistent measurement and modeling results are obtained.**

Keywords— back-end-of-line, thermal resistance, prediction, modeling, experimental characterization

I. INTRODUCTION

The thermal resistance of the BEOL stack when dissipating the front-end-of-line (FEOL) power and the Joule heating inside the interconnects are the two main thermal bottlenecks for advanced BEOL stacks. They increase for scaling technology nodes [1], [2] mainly due to the smaller interconnect dimensions, the lower thermal conductivity of low permittivity dielectrics (low-κ) and scaled metals, and the increasing BEOL layer number. Both thermal metrics are closely related to the BEOL out-of-plane thermal resistance. Meanwhile, in 3D technology, the thickness of the inter-die bonding interface shrinks with developing integration technology [3], making BEOL the dominant contributor to the overall thermal resistance in advanced packages [4] (> 90% of the total inter-die resistance for hybrid bonding [5]). Consequently, a high interconnect temperature can lead to a large interconnect lifetime degradation [6]. Therefore, it is important to predict the BEOL out-of-plane thermal resistance accurately. Several studies have focused on finite element (FE) modeling and experimental measurements of this property. The reported resistance is very design-specific [7] and requires dedicated analysis of a specific design. Furthermore, the existing analytical models either ignore the impact of via connectivity or only apply to regular connectivity, and the experimental out-of-plane thermal resistance characterization is only discussed for old technology nodes.

In this work, a fast evaluation methodology is developed based on test cases mimicking actual BEOL connectivity. It is further applied to an advanced 14-layer BEOL stack for detailed breakdown thermal analysis. Experimental characterization of the out-of-plane thermal coupling for a multi-layer 28nm BEOL test vehicle is then performed and calibrated with FE modeling.

II. THERMAL MODELING

A. Modeling methodology

As the Fourier-based continuum approach for heat conduction breaks down for sub-micron dimensions, a hybrid modeling approach shown in Fig. 1 is applied. For nano-scale interconnect lines and vias, due to the internal and interfacial scattering of the heat carriers, the effective thermal conductivity decreases for smaller dimensions, which has been extracted as a function of dimensions from dedicated Monte Carlo Boltzmann transport equation (BTE) simulations [8]. These material property relations are further imported into the micro-scale BEOL stack FE model to solve the continuum-based Fourier model with reasonable computational time. The effective thermal resistance per BEOL layer is further extracted.
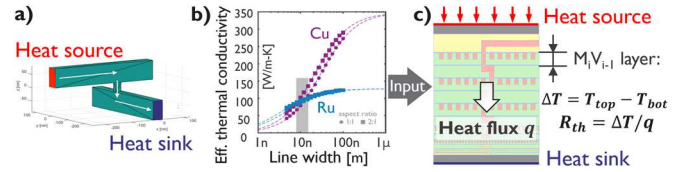

Fig. 1. a) Dedicated BTE simulation; b) extracted dimension-dependent effective thermal conductivity of metal lines; c) BEOL stack FE modeling

B. Thermal resistance prediction per M_iV_{i-1} layer

A 3D FE modeling is first conducted on a simplified BEOL stack with three prototypical connectivity types [9]. As shown in Fig. 2, the change from stacked-via to isolated-via brings a significant resistance increase, highlighting the unignorable connectivity impact and the impossibility of using one simple equation to describe all connectivity cases. Our strategy to tackle such uncertainty is to describe the stacked-via BEOL resistance $R_{th,sv}$ with an analytical model and extrapolate to randomized connectivity using a connectivity factor f: $R_{th,rand} = f \cdot R_{th,sv}$.
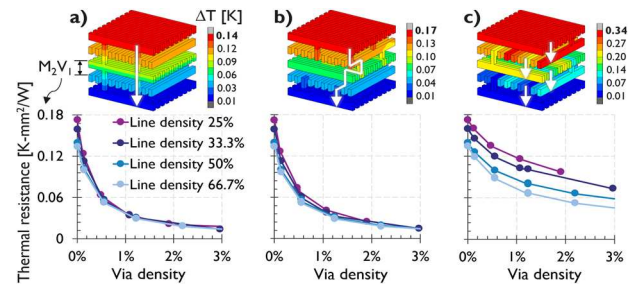

Fig. 2. 3D FE modeling on a simplified BEOL stack (Cu width 20nm, AR=2, and low-k 3.0) with three prototypical types of via connectivity configuration: a) stacked-via; b) connected-staggered-via; c) isolated-via

Several analytical models are available to predict the $R_{th,sv}$. The prediction errors are plotted in Fig. 3. b): (1) 1D conduction model: this widely used model assumes metals in a parallel connection with dielectrics and ignores the in-plane heat spreading. It underpredicts the $R_{th,sv}$ by around 30% and even up to 20% for the simplest no-via case R_{no-via}. (2) Wire-ground capacitance model: reported by Jiang. L. et al. [10], it synergizes thermal analysis with electrical analysis by using a well-calibrated wire-to-ground electrical capacitance equation to predict the R_{no-via}. A perfect match is obtained at 0 via density. This model further assumes the R_{no-via} part is connected in parallel with vias together with part of metal wires on top of the vias. An increasing overprediction is observed with increasing via density. Therefore, we further modified this model by allowing heat spreading inside the wires on top of vias thus reducing the predicted $R_{th,sv}$ and obtained good agreement with the FE modeling. Notably, this $R_{th,sv}$ prediction model directly applies to any interconnect structures with stacked-via, for example, power delivery network (PDN) and backside PDN.

Next, 3D geometries of simplified BEOL test cases with randomized interconnect layouts and randomized via locations are generated, as shown in Fig. 3. a). They exhibit a similarity to signal line routings surrounded by dummy fills and thus can be more representative of realistic BEOL connectivity. The test cases are modeled with detailed FE modeling for single-layer thermal resistance R_{rand} for various line/via densities. The extracted via connectivity factor $f = R_{rand}/R_{th,sv}$ is plotted in Fig. 3. c) as a function of via density and line density. As the actual line density after adding dummy fills is around 50% and the normal via density is 1% or higher, the via connectivity factor at this density range ($f \approx 2$) will be used for section II.C.
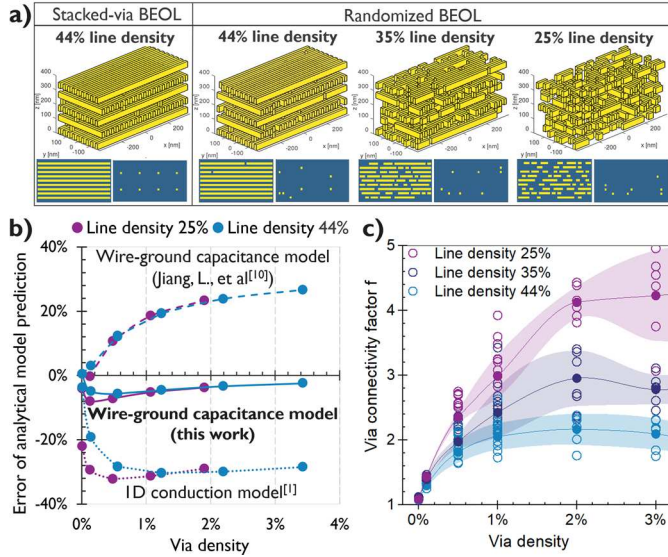

Fig. 3. a) 3D geometries and 2D layouts of stacked-via and randomized test cases; b) stacked-via BEOL: prediction errors of analytical models compared to the FE modeling; c) randomized BEOL: extracted via connectivity factor f

C. BEOL stack thermal resistance breakdown analysis

The fast evaluation methodology is applied to an advanced BEOL stack example representative of the 3 nm logic technology node with 14 layers. The technical details are listed in Fig. 4. a). Barriers are added at the via bottom with a literature-reported effective conductivity of around 3 W/m-K [11][12]. 50% line density and 1% via density are assumed throughout the stack. By further assuming the M_x-M_y layers are dominated by randomized connectivity while the M_z layers have a good vertical via connectivity for power supply, each layer's thermal resistance is calculated and plotted in Fig. 4. b).

When using SiO_2 as the dielectric in the M_y layers, the total out-of-plane thermal resistance of this 4.47 μm thick BEOL stack is 1.37 K-mm²/W. As shown in Fig. 4. c), thermal resistance is co-determined by thermal conductivity and thickness. Therefore, even though the thermal conductivity of the M_x layers is much smaller than the other layers due to the relatively low thermal conductivity of confined metals, the low thermal conductivity of low-k 3.0, and the random-like via connectivity in such layers, the M_x layers only contribute 24% of the total thermal resistance. The highest thermal contribution comes from the M_z layers due to their high thickness. However, when applying low-k 3.0 as the dielectric in the M_y layers, the dominancy shifts from M_z to M_y. The M_y layers contribute the highest 41% resistance in total, even though they only occupy 24% thickness of the whole stack. This dominancy shift emphasizes the significant impact of dielectric thermal conductivity.
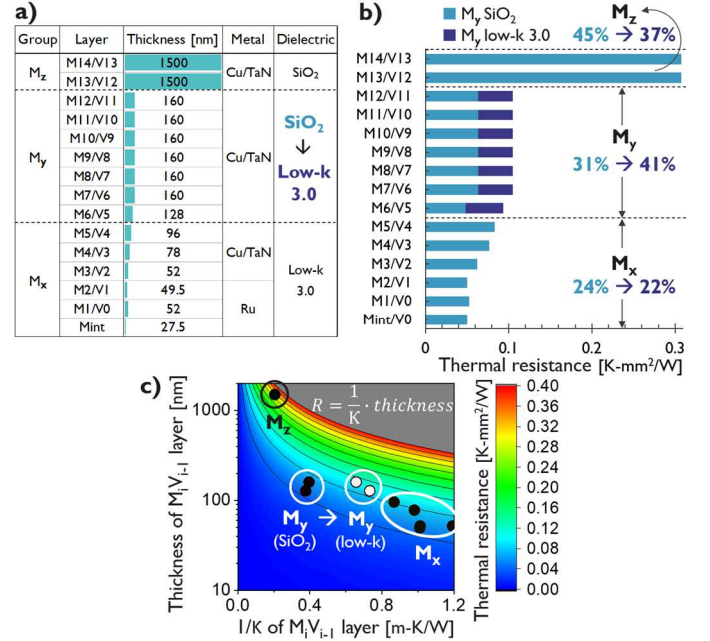

Fig. 4. a) Technical details of the BEOL stack example; b) thermal resistance contribution of each layer; c) visualization of thermal resistance of each layer co-impacted by layer thickness and layer thermal conductivity

To further compare the thermal contributions of line layers and via layers, we further performed a FE modeling enabling us to split the resistance per line/via layer, and the extracted resistance is plotted in Fig. 5. The via layers contribute 86% of total thermal resistance, while the line layers only give 14%. It explains why via density significantly affects the BEOL thermal resistance, while the line density has a relatively small impact. The existence of the barriers increases the total BEOL thermal resistance by 5% and slightly differentiates the thermal resistance of Cu/TaN and Cu metallization by 17.8% when comparing M_3/V_2 and M_1/V_0 layers.
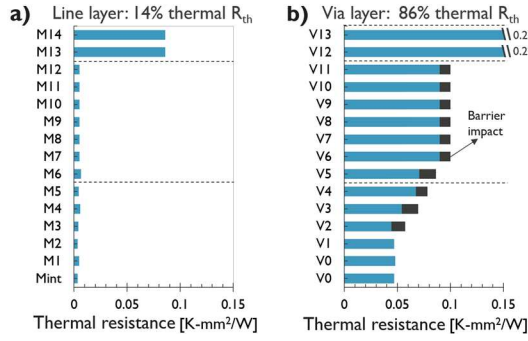
Fig. 5. Separated thermal R_{th} contributions of a) line layers and b) via layers

III. EXPERIMENTAL CHARACTERIZATION

A dedicated 8-metal-layer BEOL test vehicle is designed in a 28nm foundry CMOS technology to experimentally characterize the out-of-plane thermal coupling inside the BEOL stack. Meander metal lines in M_2, M_5, and M_7 layers with 0.5 μm line width are designed as both heaters and sensors to in-situ measure the temperature in different BEOL layers (split into two modules due to the pad limit). The total area of the meander heater/sensor is designed to be large enough (40×40 μm^2) to ensure the heat conduction inside the stack is an almost 1D vertical flow to reduce heat loss in the in-plane direction and improve the measurement sensitivity to out-of-plane properties. A diode (P+/NWEL) is placed in the FEOL as a temperature sensor.
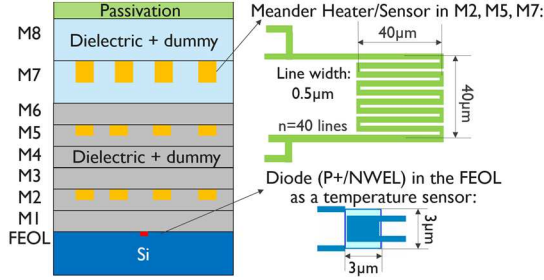

Fig. 6. Schematic of the multi-layer BEOL test vehicle

Temperature readings are conducted by measuring the electrical resistance change of heaters/sensors during Joule heating: $R = R_0[1 + \alpha(T - T_0)]$, where T_0 is room temperature, R_0 is the resistance at room temperature, and the α is the temperature coefficient of resistance (TCR). As the TCR is dimension-dependent, calibration is required for sensors with different dimensions. By tuning the power level injected in the heater, the temperature measured on heaters/sensors is plotted as a function of the power density. An example with the heater in M_7 is shown in Fig. 7, where the curve slopes can be interpreted as the self-heating thermal resistance of the heater ($R_{th, M7}$ = 2.18 mm^2-K/W) and the coupling thermal resistance of the sensors ($R_{coupling, M7-M5}$ = 1 mm^2-K/W, $R_{coupling, M7-M2}$ = 0.58 mm^2-K/W).
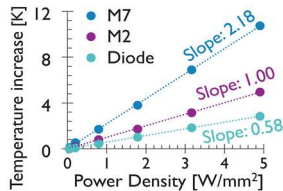

Fig. 7. Temperature-Power density curve with the heater in M_7

The measured self-heating/coupling thermal resistance of all three heating scenarios is plotted in Fig. 8. With the advantage of heat sources available in multiple locations, a 3D FE model for parameter extraction is successfully calibrated with the measurements to clarify the unknown boundary conditions and the heat loss impacted by boundary conditions. Consistent measurement and modeling results are obtained, as shown in Fig. 8. The three heating scenarios show similar temperature drops below the heater and slight temperature drops above the heater, indicating that the desired almost 1D out-of-plane heat flow is achieved. Furthermore, the heating at different locations can express the thermal coupling (%) to different layers, and the thermal coupling is labeled in percentage for different layers in Fig. 8.
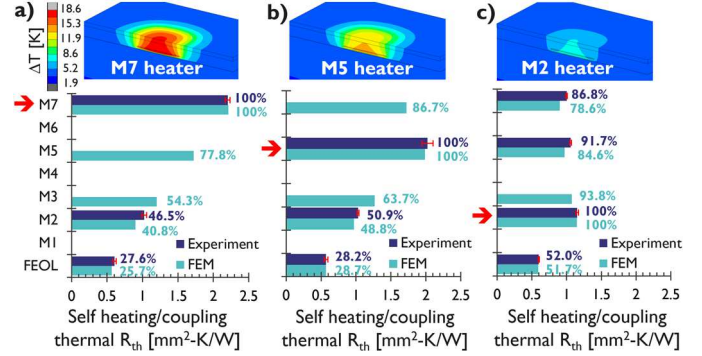

Fig. 8. Consistent measurement and modeling results of heating scenarios with the heater in: a) M_7, b) M_5, and c) M_2

IV. CONCLUSIONS

In this work, a fast evaluation methodology is developed to aid the thermal-aware BEOL design with a quick estimation of out-of-plane layer equivalent thermal properties based on design rules for dimensions and densities. The method is calibrated with a detailed FE thermal simulation and is applicable to realistic BEOL connectivity. With this method, a breakdown thermal analysis is performed on an advanced 3 nm 14-layer BEOL stack. The M_z/M_y layers dominate the total thermal resistance, depending on the thermal conductivity of the M_y dielectric, and the via layers contribute 86% of total thermal resistance, while the line layers only represent 14%. A significant thermal impact is observed for the M_y dielectric, while the thermal difference between Cu and Ru metallization at the tested metal width is small and is mainly contributed by the barrier. Next, a dedicated multi-layer BEOL test vehicle is designed in a 28nm foundry CMOS technology. The out-of-plane thermal coupling is experimentally characterized, and consistent measurement and modeling results are obtained.

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