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Sequential 3D standard cell 4T architecture using design crenellation and self-aligned MOL for N2 technology and beyond.

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ABSTRACT

As traditional pitch scaling is losing steam, 3D logic is being explored to further extend density scaling as an alternative to continued standard cell scaling. This paper will discuss standard cell architectures to be used in a Sequential 3D process where the SoC is comprised out of 2 or more tiers of active CMOS with a given BEOL metal stack per tier. Using backside interconnect metals as standard cell power rails, a smart partitioning of the metal usage within standard cells can be obtained leading to 4 track cell height scaling. A design abstraction using crenelated design is however needed at block level to mitigate via and metal line end conflicts.

Keywords: Standard Cell Design, SoC Technology Co-Optimization (STCO), Advanced technology node, Patterning options, buried power rail, Scaling boosters, FinFET, Nanosheet, Forksheet, 3D, Sequential 3D, crenellation

1. INTRODUCTION

As logic scaling is losing steam due to limitations in patterning [1] and device performance [2], standard cell scaling is achieved by track height reduction driven by fin depopulation [3], self-aligned gate contacts [4-6] and gate cut last in replacement metal gate[7-8]. Furthermore, the introduction of buried power rails allows to scale down to a 5T standard cell architecture. More recently, 3D logic is being explored to further extend density scaling as an alternative to continued standard cell scaling [9]. However, moving to a 3D architecture, SoC-technology co-optimisation will be required where technology hybridization becomes the key element to partition the SoC (Fig. 1).

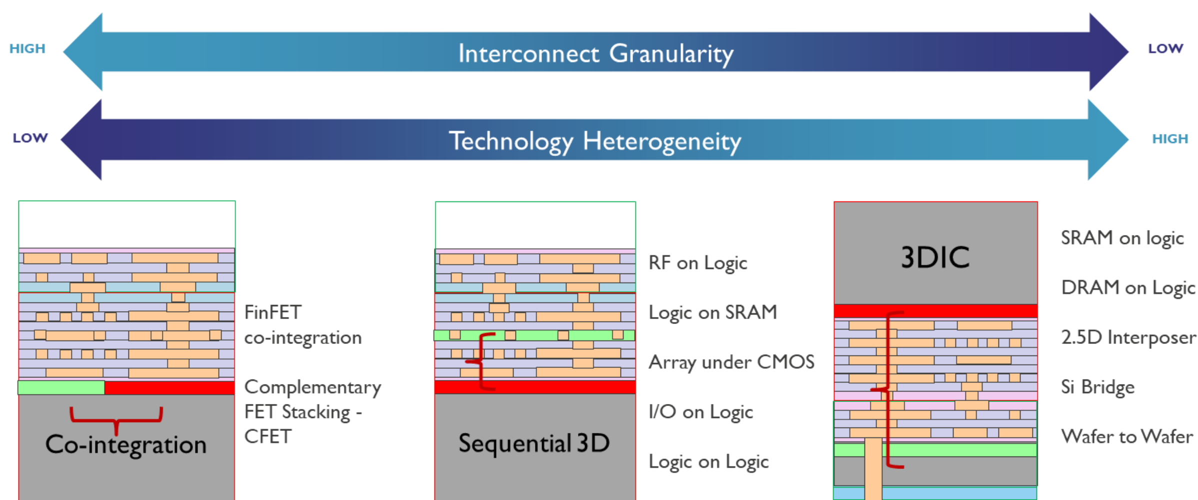

Figure 1- Technology hybridisation becomes the key in SoC-technology co-optimisation. SoCs with a high interconnect granularity and low technology heterogeneity can be cointegrated in the same technology platform. SoCs with a low interconnect granularity and high technology heterogeneity are better fabricated using 3D IC approaches where chips of different platform technologies are stacked. SoCs in the middle of this spectrum however require smart partitioning to optimise the technology needed for the entire SoC

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2. BACKSIDE INTERCONNECT FOR LOGIC

This paper will discuss standard cell architectures to be used in a Sequential 3D process where the SoC is comprised out of 2 or more tiers of active CMOS with a given BEOL metal stack per tier. The interconnect of a bottom tier (w.r.t the logic tier) can effectively be used as a backside interconnect and aid standard cell scaling (Fig. 2).

Using backside interconnect a smarter partitioning of the metal usage of standard cells can be obtained. The standard cell methodology used in ASIC design allows for VLSI by placement of "standardized" blocks and allows for independent optimization of standard cell layouts and gate level design. However, this split in design abstraction does not coincide completely with the Front and Back End of Line (FEOL/BEOL) integration split. A better partitioning of the BEOL connectivity can be achieved by splitting the signal wires from the power as shown in Fig. 2.

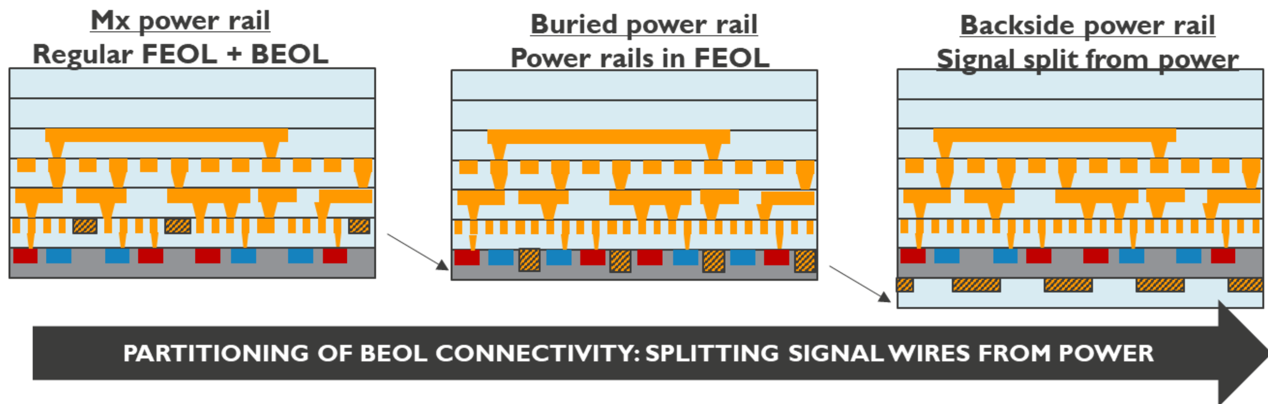

Figure 2- Efficient use of backside interconnect by moving the power rail from frontside to the FEOL and to the backside.

To achieve such backside interconnect for logic two main options can be considered (Fig. 3). In the sequential 3D process the top tier containing logic is fabricated on top of a bottom tier containing e.g. memory cells. Here the top prefabricated metal interconnect of the bottom tier is used as a backside interconnect for the top tier. An alternative option is the use a so-called backside reveal process [10]. Here the logic tier is fabricated and its top is bonded to a carrier wafer. By flipping the logic wafer and using the bonding wafer the backside can be accessed for further processing. Interconnect is fabricated on the thinned backside.

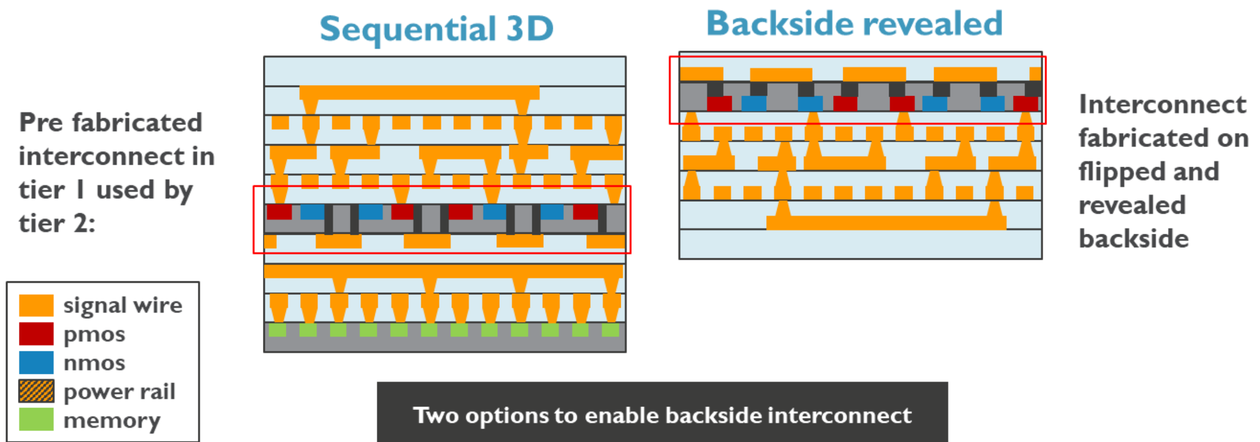

Figure 3- Besides using sequential 3D process, backside reveal process can also enable backside interconnect to be used as power rails.

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3. STANDARD CELL ARCHITECTURE

By moving the power delivery from the frontside to the backside, standard cells can be scaled from 6T using Mx power rail to 5T using buried, and 4.5T using backside power rail (Figs 4,5). Moreover, by staggering via and metal patterns along the power rail scaling to 4T is achieved under the same design rules (Fig. 5).

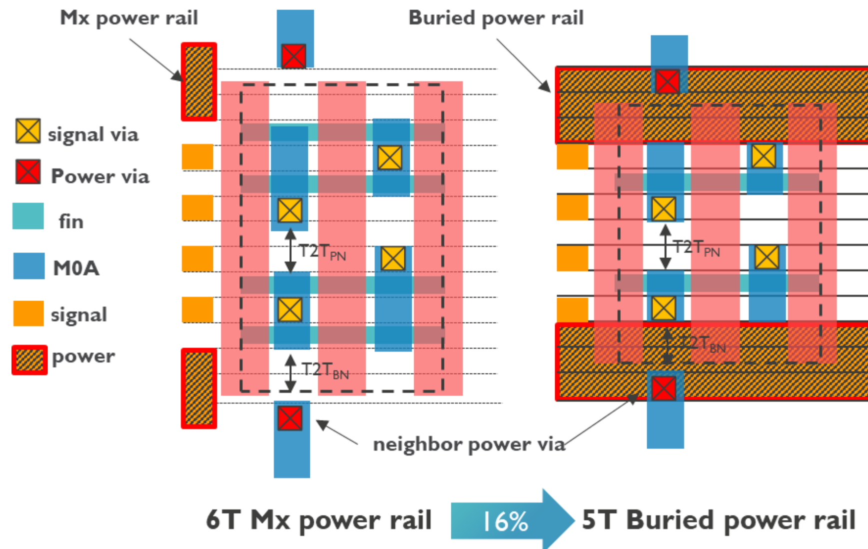

Figure 4- Standard Cell scaling from 6T down to 5T using buried power rail.

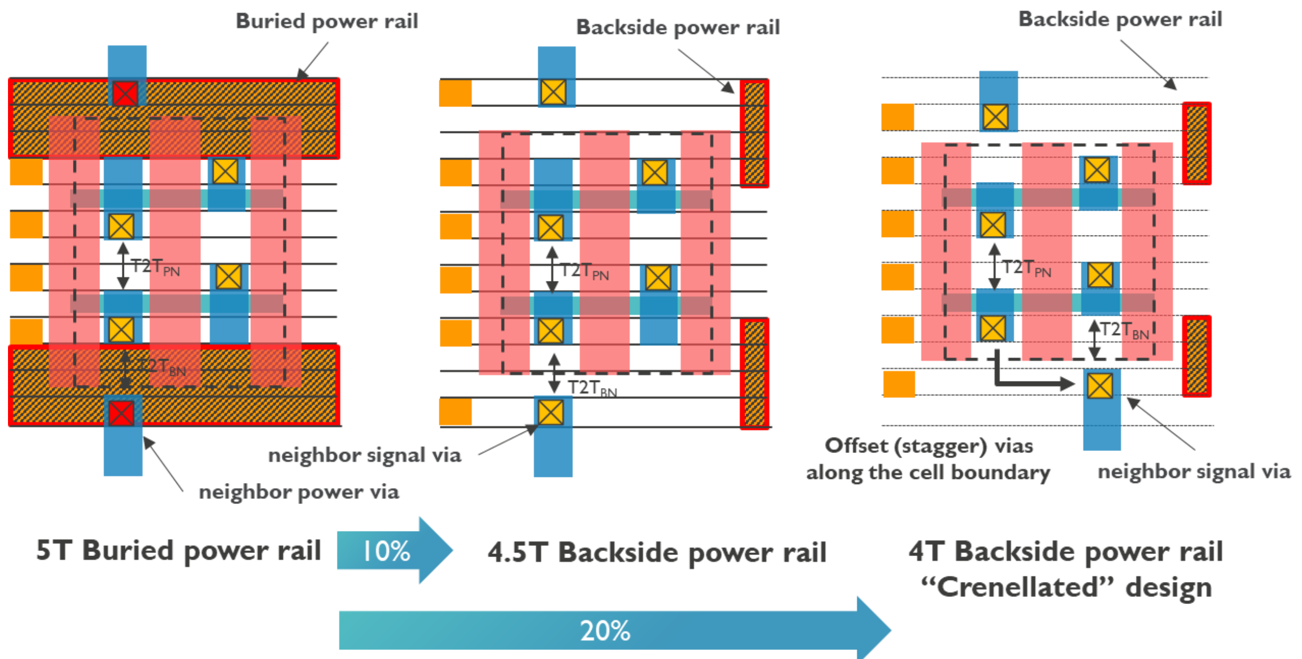

Figure 5- Standard Cell scaling from 5T down to 4T using backside power rail and design crenellation for contacts (M0A).

This 'crenellation' [11], allows for design abstraction at the standard cell level which simplifies place and route at the block level. Individual standard cells will need to have chirality cells where vias are staggered differently accordingly to a

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crenellation phase which equals the layer pitch. Additionally, crenellation needs to be maintained for all intra-cell routing metals. However, with only 4 routing tracks, crenellation cannot be maintained for both M0A/VINT and M1/V0 layers without increasing dummy poly count and/or M1 and M2 resources. Also, gate pickup using the outer tracks is difficult as this requires a gate cut width of only one metal half pitch. On the other hand, gate crenellation is not desired as it is restricted by variability impact due to gate cut proximity effects. Consequently, crenellation can only be absorbed in 1 routing layer and a solution is found where M1/V0 is crenelated and M0A and gate needs to maintain 4 track routing freedom.

4. SELF-ALIGNED S/D TRENCH CONTACTS AND GATES

This M0A 4-track routing freedom is achieved by introducing spacer defined separations between S/D trench contacts and gates. This device topology is analogous to the Forksheet [12] design (Fig. 3).

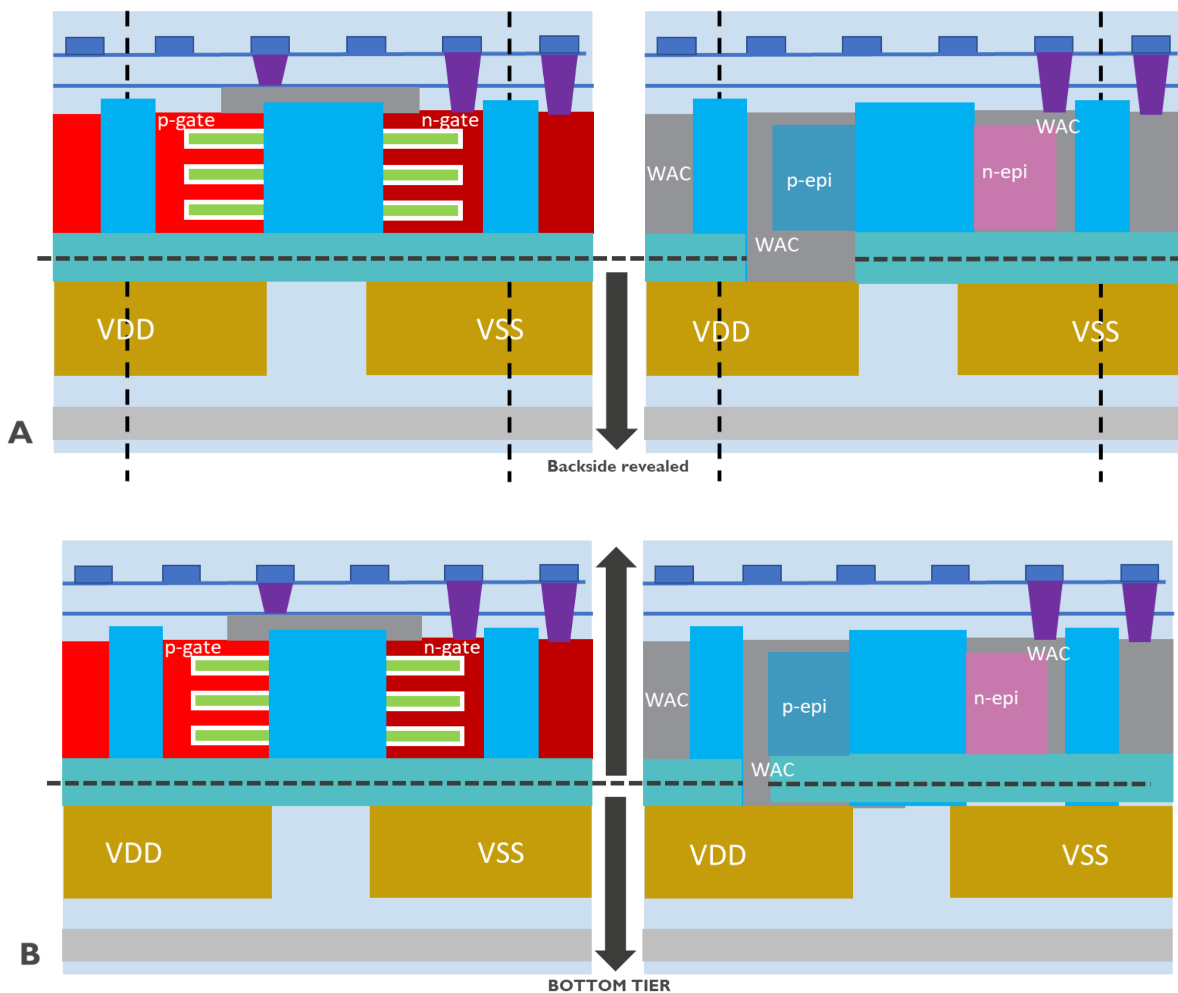

Figure 6- A) Backside revealed and B) Sequential 3D with fork sheet device along gate and S/D trench using via self-alignment and merged litho via to maintain 4 track routing.

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The routing freedom for gate and active contacts is achieved by exploiting self-alignment using via etch through the MINT trench and guidance by the spacer wall topology. Independent track pick-up is achieved using litho-merge via printing.

5. CRENNELATED DESIGN ABSTRACTION

Using crenellated design, cell will have different chirality depending on the position of the staggered vias and metal line ends as shown in Fig. 7. Tiling cells at the power rails can be done for same or different type chirality by offsetting with one phase. Tiling at the gate boundary needs the same chirality for even poly and different chirality for odd poly cells (Fig. 8). Using these rules, tiling at block level can be achieved by always following the same crenellation phase along the power rail boundaries (Fig. 9).

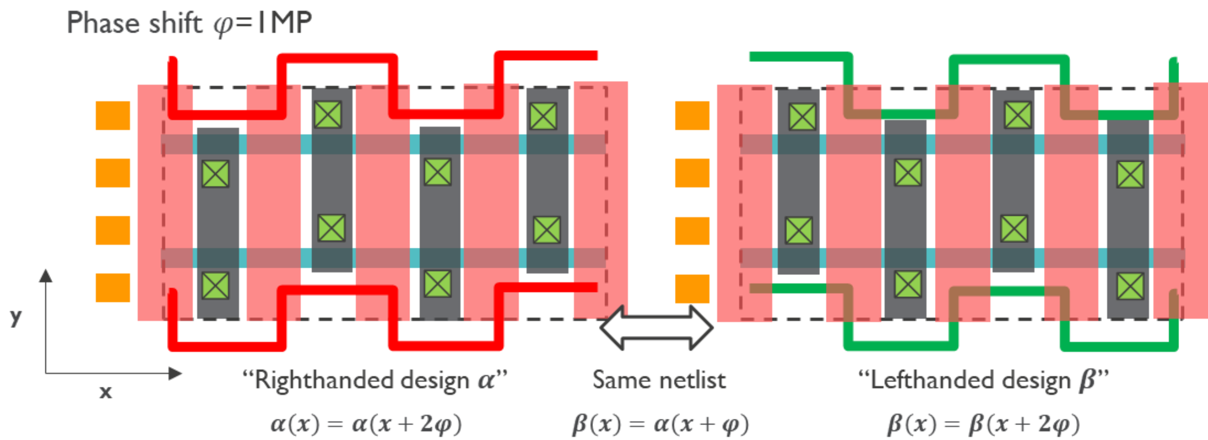

Figure 7- Cell chirality is displayed using a crennelation phase.

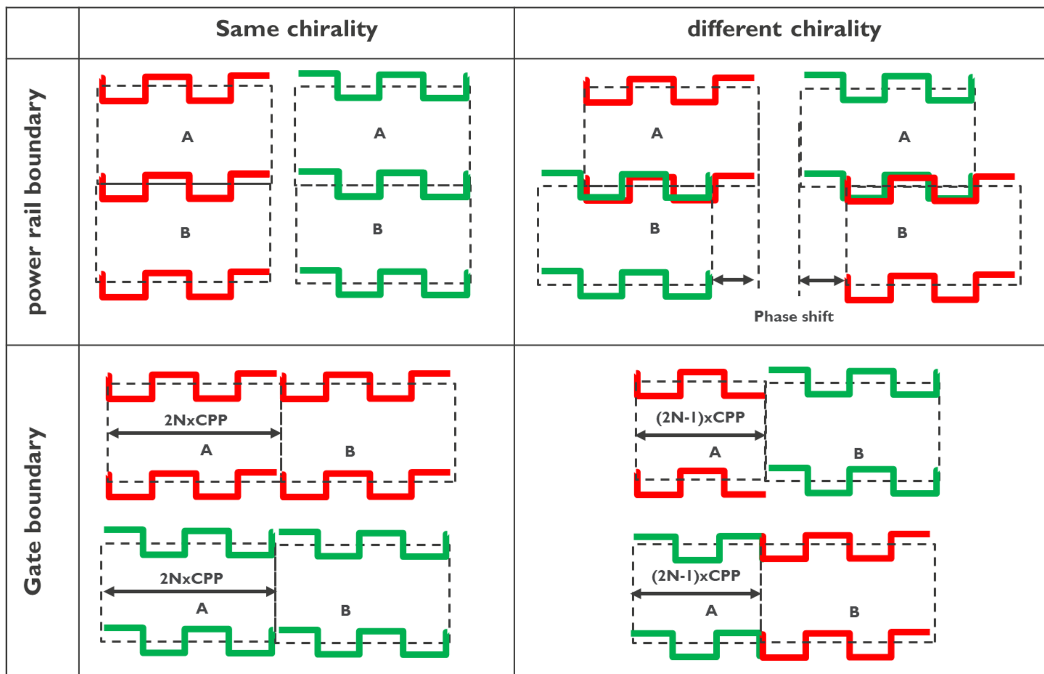

Figure 8- Crenellation design abstraction requires place and route rules for tiling cells at the power rails boundary and gate boundary.

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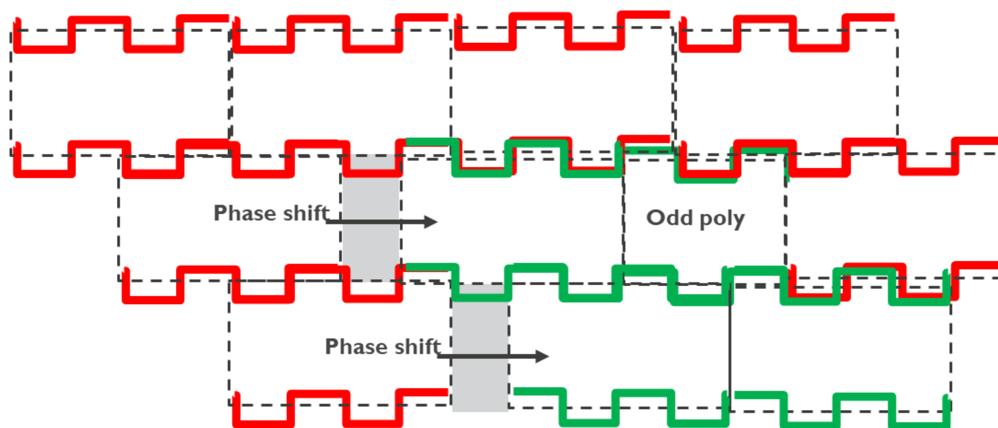

Figure 9- Block level tiling by maintaining crenellation phase.

SUMMARY

A standard cell architecture for Sequential 3D logic is proposed. The interconnect of a bottom tier can be used as a backside power rail to enable scaling down to 4T. This is achieved by staggering via and metal patterns along the power rail in the so-called crenellation fashion. It is argued that crenellation can only be absorbed in the M1/V0 layer and MOL needs to maintain 4 track routing freedom. This is achieved by Forksheet device design and via self-alignment. Tiling cells at block level can be achieved by always following the same crenellation phase along the power rail boundaries.

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