Advanced Current-Voltage Model of Electrical Contacts to GaAs- and Ge-Based Active Silicon Photonic Devices

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***Abstract*—A new compact model, incorporating bias-dependent Schottky barrier height, is developed to precisely describe the forward-biased current-voltage characteristic of electrical contacts to Ge and GaAs layers in active silicon photonic (SiPho) components. This generic model enables direct evaluation of both the contact doping concentration and the effective barrier height of any semiconductor diode with a single-sided Schottky contact. Extracted parameters greatly agree with spreading series resistance microscopy (SSRM) results and literature reports. Process variabilities and design impacts were studied, insights brought by the model enlightens future device improvements to realize Ohmic contacts.**

***Index Terms*—Current-Voltage Characteristic, Diodes, Schottky Contact, Silicon Photonics, Thermionic Field Emission.**

I. Introduction

SILICON photonics (SiPho), leveraging its scalability and manufacturability, has emerged as a crucial platform for telecom/datacom applications [1], [2]. Fig. 1(a) shows the essential building blocks of a SiPho transceiver. Many active components require co-integration of different material systems. For instance, semiconductor lasers are mostly fabricated by III-V materials such as (In)GaAs or InP [3]–[5]; Ge-on-Si photodetectors are nowadays mainstream for C-band and O-band telecommunication [6]–[8]; and last but not least, Ge based electro-absorption modulators (EAM) are potential candidates to meet the low power and high bandwidth targets [9]. Although optical, electrical, and thermal properties can be separately optimized by taking most appealing parts from different materials, making efficient electrical contacts on III-V or Ge remains a nontrivial, sometimes even a challenging task, especially when CMOS compatible technology is strictly demanded.

While non-optimal electrical contacts have negligible impact in reverse bias (and therefore are not considered in this work), they give rise to poor current injection efficiency, eventually resulting in higher power consumption and reliability issues in forward bias. A classical single-diode model is generally used for describing experimental I-V characteristics (e.g., solar cells [10]–[12], photodetectors [13], [14], LEDs/lasers [15], [16] etc.). As depicted in Fig. 2(a), the lumped circuit model encompasses two parasitic resistors connected in series or shunt with the diode. Nevertheless, a noticeable discrepancy between the classical model (red dashes) and the measured I-V (black dots) of active SiPho diodes is observed in this study, as shown in Fig. 3(a) and (b). Such discrepancy is discussed in this paper and proved to originate from non-Ohmic contact properties, thus the series resistance can no longer be treated as a constant.

Schottky barrier heights (SBH) at III-V and Ge contacts are relatively stubborn to the change of metal work functions, which is notorious as 'pinning' of the Fermi level by either surface states [17] or metal induced gap states (MIGS) [18]. Recently, a more comprehensive, quantum-mechanical-based picture of interface dipole formation has been constructed [19]. From an engineering perspective, benchmarking the contact resistivity with the effective SBH and the doping concentration is beneficial for defining device specifications. Several attempts have been made based on the thermionic field emission (TFE) model of carrier transport [20]–[22]. However, existing models rely on inputs from test vehicles (e.g., circular transfer length method in [21] and cross-bridge Kelvin resistor in [22]), which demand extra measurements and sometimes show an offset with actual working devices because of dissimilar designs. In addition, doping concentration needs to be quantified by other techniques in order to obtain effective SBH, or vice versa. Finally, Ohmic-like behavior within a small current/voltage interval is usually assumed for convenience, which presumes that the contact resistivity is independent of the operating conditions, which we show is not the case. Ergo, a new I-V model which considers voltage-dependent series resistance is of major significance, as it will bring clearer illustrations of contact physics and can point paths toward Ohmic contact realization.

In this work, a diode's I-V compact model which considers a single-sided Schottky contact is presented. The model allows

This work was carried out as part of imec's industry-affiliation R&D program on "Optical I/O". This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101017194 (SIPHO-G).

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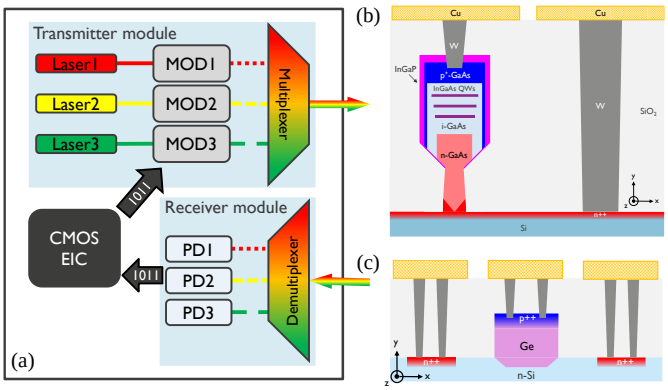

Fig. 1. Schematics of (a) fundamental building blocks of a silicon photonics transceiver. (b) a GaAs-on-Si nano-ridge PIN diode for laser/amplifier application. (c) a Ge-on-Si vertical PIN photodetector.

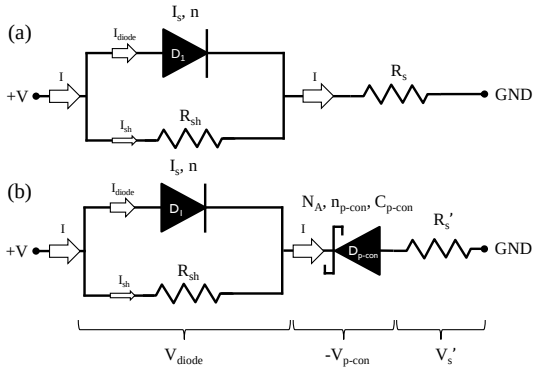

Fig. 2. Lumped circuit views of (a) the classical one-diode model and (b) the single-sided Schottky contact model developed in this work.

direct extraction of both SBH and doping concentration from working SiPho devices. The extracted SBH agrees well with the literature data and the doping concentration is benchmarked with scanning spreading resistance microscopy (SSRM) results. Device properties, variability and the impact of a sintering process step are studied using this model. Lastly, an example of applying the model as a guideline for contact optimization is discussed.

II. Device Description and Measurement Setup

GaAs nano-ridge PIN diodes (Fig. 1(b)) and Ge Vertical PIN photodetectors (Fig. 1(c)) were chosen for model demonstrations. Their process flows and properties were detailed in previous publications [6], [7], [23], [24]. Devices were fabricated by fully CMOS compatible processes: monolithic integration of GaAs- or Ge-on-Si were achieved by nano-ridge engineering (NRE) and selective area epitaxy, respectively, growing from the Si layer at the bottom of SiO_2 trenches; conventional W-plug and Cu-interconnect metallization were employed for electrical connections. Current-voltage characteristics were measured at room temperature by a Keysight B1500A semiconductor device parameter analyzer.

SSRM is a scanning probe microscopy technique in which a sharp conductive tip is scanned over the surface of a semiconductor sample [25]. While scanning, the local topography and resistance of the sample are recorded at the nanometer scale. The active carrier concentration in a GaAs

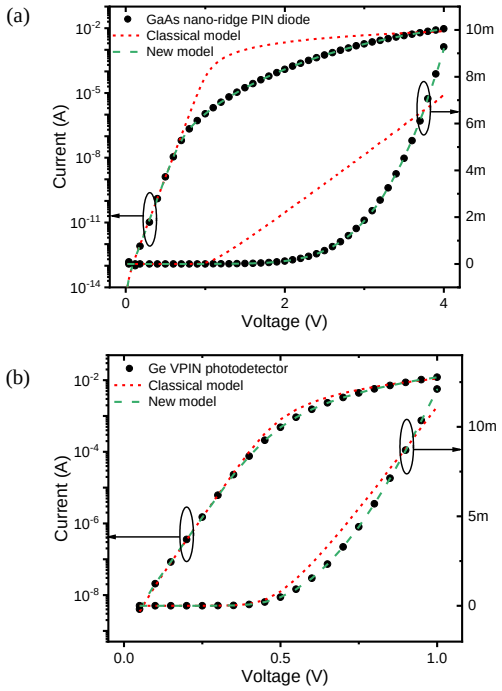

Fig. 3. Current-voltage characteristics of (a) a GaAs nano-ridge PIN diode and (b) a Ge vertical PIN photodetector. Red dashes show fittings of the classical model and green dots represent results from the new model of this work.

sample can be extracted from the measured resistance map by performing a calibration measurement on a GaAs reference stack. This calibration sample has multiple layers with known carrier concentrations, determined by electrochemical capacitance-voltage (ECV) profiling.

III. Development of the New I-V Model

In this section, the problem of employing the classical single-diode model is discussed. Next, a new model is developed, considering the bias-dependent series resistance stemming from a single-sided Schottky contact. The methodology and fitting procedures are elucidated in detail.

A. Classical Single-Diode Model

The classical model assumes that series and shunt resistances are invariant in full operating range, and the current-voltage relationship is written as

$$I = I_s\left(\exp\left(\frac{V-IR_s}{nV_T}\right)-1\right)+\frac{V-IR_s}{R_{sh}} \quad (1)$$

I_s is the saturation current and n is the ideality factor of the diode; $V_T=k_BT/q$ is the thermal voltage with k_B the Boltzmann constant, T the temperature and q the elementary charge; R_s and R_{sh} are the lumped series and shunt resistance respectively. The measured I-V can be fitted to determine I_s, n, R_s and R_{sh}, by solving (1) iteratively to minimize the residual. As stated in the introduction (Fig. 3), the classical model poorly portrays the measured I-V of two indicative SiPho components: a GaAs nano-ridge PIN diode in Fig. 3(a) and a Ge Vertical PIN photodetector in Fig. 3(b).

To grasp the root cause, (1) is simplified by taking $R_{sh}\rightarrow\infty$. This is an appropriate approximation since the shunted

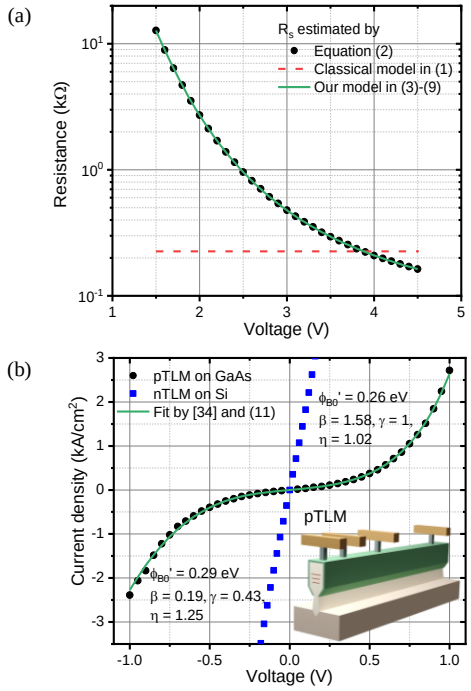

Fig. 4. GaAs nano-ridge PIN diode: (a) Series resistance as a function of applied voltage, constant R_s assumed in the classical model is incorrect for Schottky contacts. (b) Current-voltage relations of transfer length method (TLM) structures: pTLM shows a Schottky behavior while nTLM is an Ohmic contact.

leakage current is non-detectable throughout the measuring range, for all devices investigated in this article. Therefore,

$$R_s \sim \frac{V}{I} - \frac{nV_T}{I}\ln\left(\frac{I}{I_s}+1\right) \tag{2}$$

Using (2), R_s of the GaAs nano-ridge PIN diode is plotted against applied bias in Fig. 4(a). The substantial reduction of R_s with voltage originates from Schottky behavior at the metal/p-GaAs contacts, as shown by the transfer length method (TLM) measurement in Fig. 4(b). The higher voltage applied at the metal/p-GaAs contacts increases the gradient of interface potentials, leading to more pronounced TFE and effectively lower the barrier heights. On the other hand, n-type contacts on Si show a linear Ohmic behavior. Similar Schottky contact behavior was observed at the metal/p-Ge contacts of the Ge vertical PIN photodetector. Evidently, the classical model needs to be revisited to accommodate the bias-dependent series resistance.

B. I-V Model Describing the Bias-Dependent R_S

A lumped circuit view of the new diode model is displayed in Fig. 2(b). R_s in the classical model is now substituted by the combination of a reversely connected Schottky barrier diode $D_{p\text{-}con}$ and a constant resistor R_s'. The former embodies the bias-dependent resistivity of the p-contact, whereas the latter includes all other series resistances arising from n-contact, back-end-of-line, probes, and wires etc. Equation (1) is modified as

$$I = I_s\left(\exp\left(\frac{V - IR_s(V)}{nV_T}\right) - 1\right) + \frac{V - IR_s(V)}{R_{sh}} \tag{3}$$

To solve (3), one needs to resolve two relations: a) Voltage division at the diode (V_{diode}), p-contact ($V_{p\text{-}con}$), and other parts (V_s') and b) p-contact resistance ($R_{p\text{-}con}$) as a function of applied voltage.

$$V = V_{diode} + V_{p-con} + V_s' = V_{diode} + V_{p-con} + IR_s' \tag{4}$$

$$R_s(V) = R_{p-con}(V) + R_s' \tag{5}$$

The voltage at each component can readily be computed, as R_s' follows Ohm's law and V_{diode} is obtained from the diode equation (6). Since $R_{sh} \gg R_{D1}$ in the voltage range considered here, $I_{diode} \sim I$

$$V_{diode} = nV_T \ln\left(\frac{I_{diode}}{I_s}+1\right) \sim nV_T \ln\left(\frac{I}{I_s}+1\right) \tag{6}$$

Alternatively, if $R_{sh} \leq R_{D1}$ at low voltage, I_{diode} can be estimated by fitting at higher bias ($I_{diode} \sim I$) and extrapolating to lower bias. Finally, $V_{p\text{-}con}$ can be deduced by subtracting V_s' and V_{diode} from the total voltage drop.

The resistance of the Schottky p-contact requires further elaboration. Semiconductors are typically highly doped at the metal interface, hence follow the TFE model [26], [27].

$$R_{p-con}(V) = C_{p-con}\frac{k_B}{qA_{p-con}A^{**}T}\exp\left(\frac{\phi_B'}{E_{00}\coth\left(\frac{E_{00}}{k_BT}\right)}\right) \tag{7}$$

where $A_{p\text{-}con}$ is the contact area and A^{**} is the practical Richardson constant. E_{00} is the characteristic energy related to the tunneling probability [27], given by

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_A}{\varepsilon_s\varepsilon_0 m_{tun}^*}} \sim 1.86\times10^{-11}\sqrt{\frac{N_A(cm^{-3})}{\varepsilon_s\left(m_{tun}^*/m_0\right)}} \tag{8}$$

with $\hbar$, ε_s, ε_0, N_A, m_{tun}^* and m_0 the reduced Plank constant, the dielectric constant, the vacuum permittivity, the doping concentration, the tunnelling effective mass and the electron rest mass, respectively. $C_{p\text{-}con}$ is a coefficient related to interface dipole potentials, which is manipulated by contact geometry, surface treatments, metal work functions and the presence of impurities/dopants. To finish, ϕ_B' is the effective SBH, which is a function of the applied voltage. Direct calculation of the SBH is fairly intricate, as the potential barrier at the contact is shaped by the electric field, the image force potential and the local 'saddle-point' potentials induced by local interface inhomogeneity, the accurate quantum description cannot be formulated into simple analytic equations [19], [22]. Fortunately, the effective value of SBH can be acquired by utilizing the continuity of the total current. Applying the Schottky diode equation,

$$\phi_B'(V) = V_T \ln\left(\frac{A_{p-con}A^{**}T^2\left(1-\exp\left(\frac{-V_{p-con}}{n_{p-con}V_T}\right)\right)}{I}\right) \tag{9}$$

TABLE I
PARAMETERS EXTRACTED FROM THE NEW MODEL

Symbol	GaAs nano-ridge PIN (Values ± stderr)	Ge VPIN (Values ± stderr)	Unit
I_s	1.57E-14 ± 2E-11	2.26E-9 ± 1E-10	A
n	1.74 ± 0.01	1.46 ± 0.01	-
$n_{p\text{-}con}$	13.38 ± 0.03	1.23 ± 0.08	-
$C_{p\text{-}con}$	134.55 ± 0.08	32.43 ± 0.17	-
N_A	6.14E18 †	7.19E19 †	cm^{-3}
R_s'	25.29 ± 0.39	7.08 ± 0.16	Ω
ϕ_{B0}'	0.27 †	0.13 †	eV

† The last significant digit exceeds the standard error by a factor of 10.

for a diode with a single-sided Schottky contact, device and contact parameters can be accurately determined by solving (3) to (9). It is noteworthy that by exploiting similar derivations, a diode with dual-sided Schottky contacts can also be evaluated.

Diode and contact parameters are separately modeled in three steps: To begin with, diode parameters (I_s and n) are extracted in the exponentially increasing current region where the diode resistance is much higher than the series resistance, so that the voltage is assumed fully applied at D_1. Secondly, using the previously obtained I_s and n values, the current across the entire voltage range is fitted to determine contact parameters (N_A, $n_{p\text{-}con}$, $C_{p\text{-}con}$ and R_s'). In the end, a recursive computation is created to simulate a self-consistent solution of the I-V relationship. Physical constants (A^{**}, ε_s, and m_{tun}^*) are taken from [22], [28], [29].

IV. RESULTS

The current-voltage datasets of the two devices in Fig. 3 were modelled by using the methodology outlined in section III; simulated curves are represented by green dots, and extracted parameters are summarized in TABLE I. A nearly perfect fit of the experimental data is demonstrated, in both linear and semi-logarithm scales. Standard errors of fitting are negligible for most of the parameters except for I_s of the GaAs nano-ridge PIN diode, where the accuracy is limited by the measurement noise level (~10fA). In contrast, I_s of the Ge Vertical PIN photodetector can be precisely decided thanks to its higher value (2.26±0.1nA) resulting from the narrower bandgap. It is worthwhile to note that the p-contact doping concentration (N_A) gained from the model is in great agreement with our design targets.

The carrier concentration contour of a GaAs nano-ridge PIN diode is quantified by SSRM and shown in Fig. 5(b). The doping of the p-GaAs layer shows two distinct regions. The carrier concentration in the thin outer layer (top border and two sidewalls) ranges from 1 to 2E19cm^{-3}, whereas it is around 3E18cm^{-3} in the interior zone. The metal plug is located in p-GaAs with a recess of about 100nm (50nm InGaP and 50nm p-GaAs recess), as indicated by high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) in Fig. 5(a). The metal plug, in particular, comes into contact with a doping concentration gradient along the vertical direction (shown in Fig. 5(c)); N_A obtained from

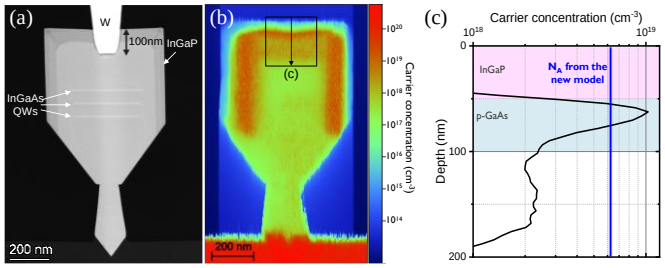

Fig. 5. (a) HAADF-STEM of a GaAs nano-ridge PIN diode cross section, the recess of the W plug is around 70nm. (b) a contour map of carrier concentration scanned by SSRM. (c) a vertical profile close to W plug region shows that N_A extracted from the new model is an effective value of the contact doping.

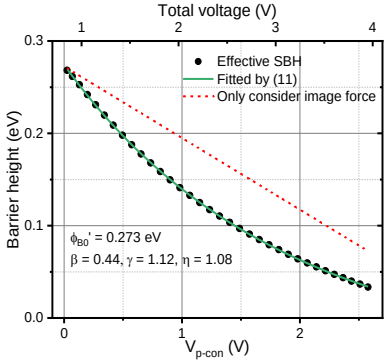

Fig. 6. The effective SBH of a GaAs nano-ridge PIN diode decreases with reverse voltage, an empirical model in (12) describes the joint impacts of image force, tunneling and local contact inhomogeneity.

the model represents an effective value that falls within the interval defined by SSRM.

The effective SBH is calculated as described in equation (9); Fig. 6 displays its voltage dependence. When the reverse bias at the p-contact is increased, the barrier reduction is often described by the effective SBH at zero bias ϕ_{B0}' and a lowering factor η [29], [30];

$$\phi_B'(V) = \phi_{B0}' - \left(1 - \frac{1}{\eta}\right) V_{p-con} \tag{10}$$

This expression only considers the lowering induced by the image force, and clearly does not match the measured data in Figure 6. Nevertheless, in highly doped semiconductors the change in tunneling probability and local barrier minima (saddle-point potentials) leads to much faster lowering. To illustrate the joint effects, (10) is rewritten as

$$\phi_B'(V) = \left(\phi_{B0}' - \left(1 - \frac{1}{\eta}\right) V_{p-con}\right) \cdot \frac{1}{1 + \left(\beta V_{p-con}\right)^{\gamma}} \tag{11}$$

The pre-factor β represents the correlation between the applied voltage and the tunneling probability. Besides, the exponent γ denotes the spread of interface potentials. The expression, although empirical, seamlessly fits the effective SBH curve. ϕ_{B0}' of p-GaAs and p-Ge attained from (11) are listed in TABLE I and are consistent with literature findings [20], [22].

A current-voltage model for metal-semiconductor-metal (MSM) devices with double Schottky barriers has recently been derived [31]. Exploiting their methodology and (11), the pTLM structure in Fig. 4(b) can be fitted. It is evident that ϕ_{B0}'

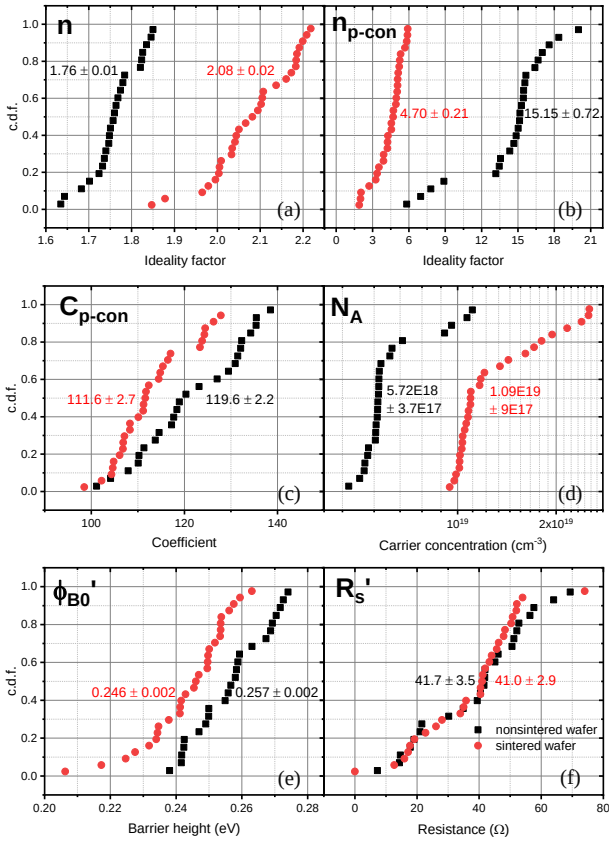

Fig. 7. Cumulative distribution functions of sintered (red dots) and non-sintered wafers (black squares), values in the graph indicate median ± standard error: (a) n, (b) $n_{p\text{-}con}$, (c) $C_{p\text{-}con}$, (d) N_A, (e) ϕ_{B0}' and (f) R_s'. The sintered wafer demonstrated a higher diode ideality factor and improved p-contact parameters.

obtained from pTLM (0.29eV and 0.26eV, with negligible standard errors) is analogous to results gained from our actual devices (0.27eV, with negligible standard errors), which consolidates the cogency of the proposed model in this work.

V. Discussion

Following development and validation, the model is implemented as a powerful tool for analyzing device properties and process impacts. Furthermore, a case study of its applications towards contact optimization is provided.

A. Impact of a Sintering Process Step

A 420°C sintering step of 20 minutes has been shown to decrease series resistance and improve electrical stability of the GaAs nano-ridge PIN diode [24]. The study was carried out by measuring and extrapolating many devices of various designs that had to deal with multiple causes of variability (device, design, fitting, and extrapolation). Even so, firm conclusions about the cause of this reduction could not be drawn, as the contact parameters were not accessible.

The proposed model provides a more inclusive understanding of the impact of sintering. The previously obtained I-V characteristics were fitted with this model, and the extracted fit parameters, measured on more than 50 devices (both with and without sintering) are summarized in Fig. 8. The cumulative distribution function (c.d.f.) of diode and contact parameters are compared in Fig. 7. The increase in

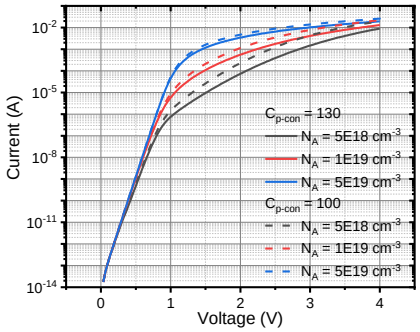

Fig. 8. Simulated I-V of the GaAs nano-ridge PIN diode with variations in N_A and $C_{p\text{-}con}$.

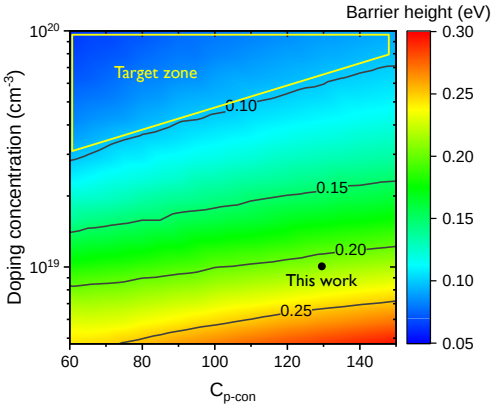

Fig. 9. The contour map of the effective SBH at p-GaAs contacts, the new model speculates an Ohmic-like contact behaviors when N_A approaches 7E19 cm^{-3}.

diode ideality factor (Fig. 7(a)) with sintering is accompanied by prominent improvements in p-contact parameters (Fig. 7(b)-(d)), in particular a factor of two increase in N_A compared to non-sintered counterparts. It is worth noting that, ϕ_{B0}' (Fig. 7(e)) declines slightly while R_s' (Fig. 7(f)) remains nearly unchanged. Finally, standard errors of all parameters of the sintered devices are akin to those of the non-sintered ones. In summary, modeling results signify that sintering increases active dopant concentration at the p-contact without deteriorating device variability, whereas higher n indicates an unexpected defect generation in nano-ridges which degrades crystal quality.

B. Toward Ohmic Contact Realization

The above results demonstrate that the developed model accurately matches measured data. In this section, we use this model in a predictive mode, to scan the impact of N_A and $C_{p\text{-}con}$, on the nature of the contact. Fig. 8 shows simulated I-V curves of the GaAs nano-ridge PIN diode with variations in N_A and $C_{p\text{-}con}$. By adopting (9) and (11) ϕ_{B0}' can be retrieved, and the contour map can be obtained as exemplified in Fig. 9. In comparison to arduous interface engineering (in a bid to reduce $C_{p\text{-}con}$), increasing doping appears to be a straightforward and more efficient way to diminish effective SBH; when N_A~7E19cm^{-3} is reached (the target zone in Fig. 9, ϕ_{B0}'<0.1eV), current transport at the p-contact is equivalent to the Ohmic behavior. On top of that, $C_{p\text{-}con}$ is expected to slightly decrease with higher N_A, as the barrier is thinner and more local barrier minima are exposed. In this region, ϕ_{B0}' is less sensitive to doping variations, thereby delivering an

adequate process window for variability-tolerant contact design. While the target doping is achievable, dedicated NRE is required to control the diode geometry and prevent defect generation [3], [32].

VI. Conclusion

A new diode current-voltage model is developed to tackle the voltage-dependent series resistance deriving from non-Ohmic contact behavior to GaAs- and Ge- based silicon photonics devices in forward-biased operation. This model comprises of 6 parameters, combining the impact of the diode, series resistance, and contact related parameters, which include bias-dependent barrier geometry and local interface inhomogeneity that have not been considered in previous works. Modeling results agree with the experimental data and the literature, it can thus be employed to examine device properties and process impacts, both being instrumental in design optimizations.

This study focuses on monolithically integrated active silicon photonic components, while the generic methodology can be extended to incorporate any diode characteristic with non-ideal contacts.

Acknowledgment

The authors would like to thank participants of imec's Monolithic III-V ART for OIO Meeting and members of the REL group for invaluable input.

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