CMOS Device Scaling by Nanosheet Channel Architectures and New Channel Materials

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***Abstract* — CMOS device scaling by nanosheet is started. Nanosheet architecture evolutions (nanosheet, forksheet and complementary FET (CFET)) with new channel materials (Si, high mobility materials and atomic channel) will drive future CMOS device scaling.**

I. Introduction

CMOS scaling by FinFETs is coming to the end. We are entering to nanosheet era for CMOS scaling [1]. Nanosheet architectures have several advantages as compared to FinFETs: 1) wider channel width/footprint due to stacked nanosheet channels, 2) better electrostatics due to gate-all-around channel architecture, and 3) design flexibility due to flexible nanosheet width. In this paper, we will discuss how to extend nanosheet architectures for CMOS scaling by using new nanosheet architectures and new channel materials.

II. Nanosheet architecture evolutions

A guideline for nanosheet architecture extension is to increase total channel width/footprint (fig. 1, 2), which improves drive current in limited area by track scaling and slow pitch scaling [2].

Nanosheet was proposed to increase total channel width/footprint in single fin standard cell to improve drive current and variability (fig. 3) [3, 4].

To extend nanosheet architecture, Forksheet is proposed, which has a dielectric wall between neighboring devices [5, 6]. The dielectric wall reduces space between neighboring devices [7], which enables nanosheet width increase. The dielectric wall also improves performance by Millar capacitance reduction (fig. 4).

CFET is proposed as ultimate nanosheet architecture, which has stacked NMOS-PMOS architecture [8-10]. CFET enables CMOS with single device footprint. CFET could have different channel materials and/or orientations in top and bottom devices by wafer bonding, which improves device performance (fig. 5) [11-13]. Although CFET is attractive for area scaling and performance improvement, its process integration is much more complex than nanosheet due to its N-P stacked architecture [14].

III. Nanosheet channel materials

High mobility channel materials and channel orientations are critical to improve nanosheet device performance (fig. 6) [11, 15, 16]. Channel thickness scaling is critical to improve switching characteristics at short gate length in nanosheet devices. However, conventional group IV or III-V semiconductor channels suffer mobility degradation at scaled channel thickness [17]. Atomic channel materials, such as MoS_2 or WS_2, have potential to enable high mobility with extremely thin channel thickness (fig. 7, 8) [18-20]. To enable nanosheet devices with 2D material channels, innovations are required in 2D material growth, doping, gate stack and contact.

IV. Summary

Nanosheet architectures enable future CMOS device scaling by architecture evaluations from nanosheet to forksheet and CFET, and new nanosheet channel materials from group IV semiconductors to atomic channel materials.

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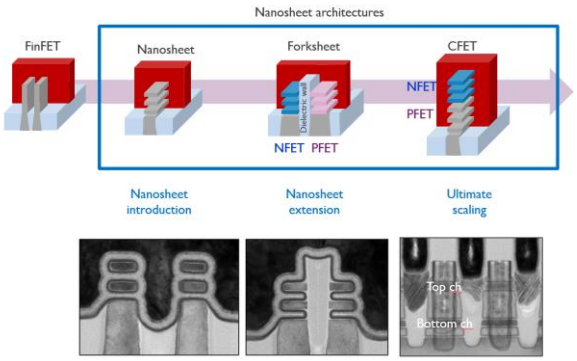

Fig. 1 Nanosheet architecture evolutions from nanosheet, to forksheet and CFET.

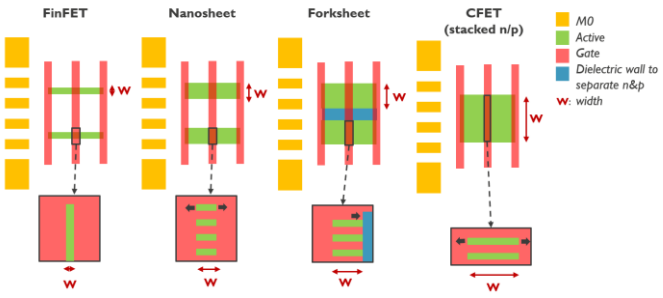

Fig. 2 Nanosheet architecture evolution guideline. Total channel width/footprint is increased by nanosheet due to stacked nanosheet channel, forksheet due to small device space with dielectric wall and CFET due to stacked NMOS-

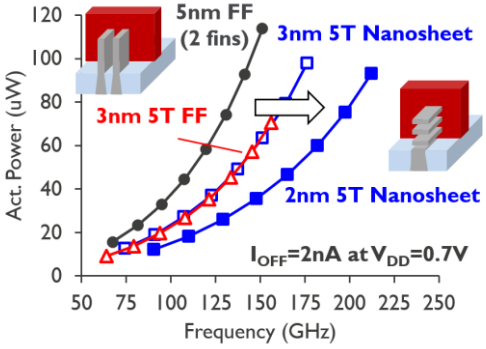

Fig. 3 Nanosheet outperforms FinFET in single fin standard cell architecture due to larger total channel width.

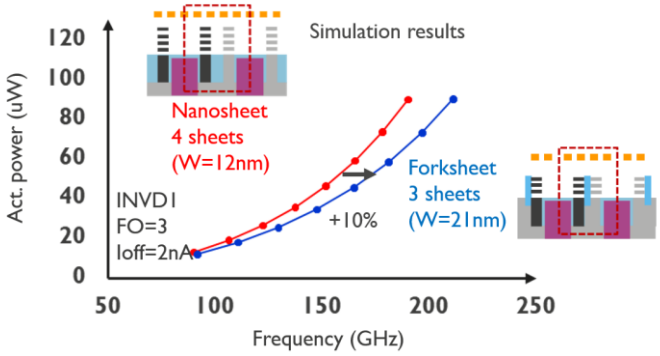

Fig. 4 Forksheet outperforms nanosheet due to larger total channel width and Millar capacitance reduction by dielectric wall [6].

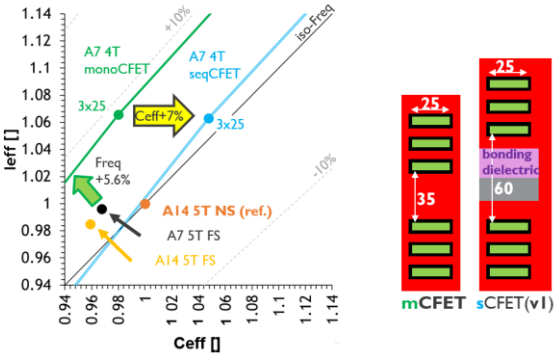

Fig. 5 CFET performance comparison with nanosheet and forksheet. Monolithic CFET outperforms nanosheet and forksheet in scaled dimensions [13].

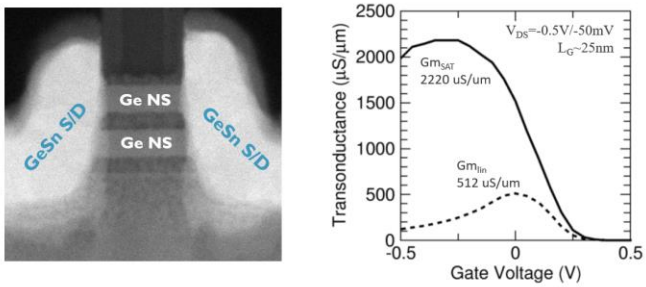

Fig. 6 pGe nanosheet cross-section and transconductance. pGe channel outperforms Si channel at low Vdd [16].

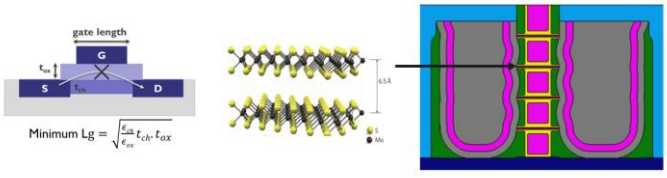

Fig. 7 Nanosheet device with atomic channel material [19].

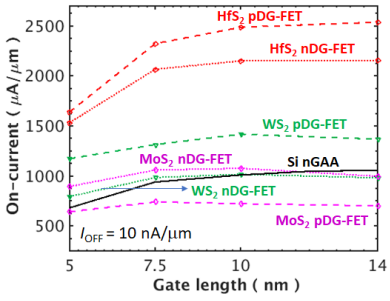

Fig. 8 Gate length-On-current comparison between Si channel and atomic channel materials (simulations) [18].