A D-band 20.4 dBm OP_{1dB} Transformer-Based Power Amplifier With 23.6% PAE In A 250-nm InP HBT Technology

Senne Gielen[$#], Yang Zhang[#], Mark Ingels[#], Patrick Reynaert[$]
[$]MICAS, KU Leuven, Belgium
[#]imec, Belgium
{senne.gielen, patrick.reynaert}@kuleuven.be

***Abstract* — This paper presents a high-efficiency transformer-based D-band power amplifier (PA) in 250-nm InP HBT. The PA has a saturated output power of 21 dBm and peak power-added efficiency (PAE) of 23.6 %. The small-signal gain and bandwidth are 19.8 dB and 24.4 GHz respectively. Careful design of the biasing networks results in a record OP_{1dB} and associated PAE of 20.4 dBm and 23% respectively. To the authors best knowledge this is the highest PAE ever reported at P_{1dB} for D-band power amplifiers, resulting in record output power and efficiency during modulated measurements up to 20 Gb/s.**

***Keywords* — D-band, InP, III-V, millimeter-Wave, high-efficiency, power amplifiers, transformers**

I. Introduction

The ever-increasing demand for higher data-rates keeps pushing the operating frequency of communication circuits in order to obtain more bandwidth. While historically CMOS-based technologies were preferred due to their high level of integration and low cost, the performance of CMOS technologies at millimeter-wave frequencies is generally subpar due to a combination low f_{max}, limiting the gain, and the low supply voltage, limiting the output power of circuits in these technologies.

III-V based technologies have shown higher gain and better power handling capabilities than CMOS-based technologies at millimeter-wave frequencies due to their higher f_{max} and breakdown voltage respectively. Especially InP-based technologies have shown the highest f_{max} while also maintaining decent power handling capabilities, making it an excellent candidate for millimeter-wave power amplifier design [1].

Typical III-V-based circuits are generally single-ended transmission line based due to their model accuracy the available metal-stack in these technologies [2]. In mm-wave CMOS on the other hand, differential transformer-based designs are very common [3], [4].

This paper presents a power amplifier (PA) that combines the design principles of millimeter-wave CMOS passives with InP HBT active devices. While previous transformer-based designs in InP HBT utilized the common-emitter topology at lower frequencies [5], in this work they are used at D-band in combination with the common-base topology. The result is a PA with a combination of both record PAE and record OP_{1dB} of $23.6\,\%$ and $20.4\,\mathrm{dBm}$ respectively. Additionally the PA achieves record PAE_{avg} and P_{avg} with modulated measurements up to $20\,\mathrm{Gb/s}$

II. Circuit Implementation

The power amplifier is designed in a 250-nm InP DHBT technology that offers four Au metal layers, MIM capacitors with a density of $0.3\,\mathrm{fF/\mu m^2}$ and thin film resistors of $50\,\Omega$/sq. The HBTs have a BV_{CEO} of $4.5\,\mathrm{V}$, a peak f_{max} of $650\,\mathrm{GHz}$ and a maximum current density of $12\,\mathrm{mA/\mu m^2}$.

A. PA Topology

The schematic of the PA is shown in figure 1. The common-base topology is chosen instead of the typical common-emitter topology as this provides a higher G_{max} without any neutralization [2]. Common-base amplifiers also show better power handling capabilities due to their increased breakdown voltage as the low base impedance allows avalanche current to flow freely out of the base [6]. The drawback of the common-base stage is that it requires accurate modelling of the base inductance for stability and gain. An additional benefit is low-Q input impedance of the common-base stage as it allows for a broadband input match of the PA.

A differential topology is chosen for this design as this naturally doubles the output power of the amplifier. The differential topology also allows the use of the virtual ground to connect to the base of the common-base stages. The layout of the driver stages and the PA core is shown in figure 2. Positioning the base terminals in a differential pair as close as possible to each other lowers the base inductance and therefore increases the gain and stabilizes the amplifier. At the output stage, multiple transistors are used in parallel, increasing the minimum distance between the base terminals. In order to stabilize the output stage, a small base resistor is added in shunt with a bypass capacitor to cancel out the resulting base inductance.

Transformers are used to implement area-efficient and low loss matching networks. This is especially beneficial for differential designs where the virtual ground at the center tap can be used to connect the power supply and provide a second harmonic short. The high resistivity of the InP substrate, the availability of multiple thick metal layers and the low dielectric constant of interlayer dielectric allow for high-Q transformers with a high self-resonant frequency. In order to increase the low input impedance of a common-base stage, a LC-network is placed after the transformer. A ground plane in the lowest metal layer is used to provide a well modelled return path for common-mode currents and for easy distribution of the

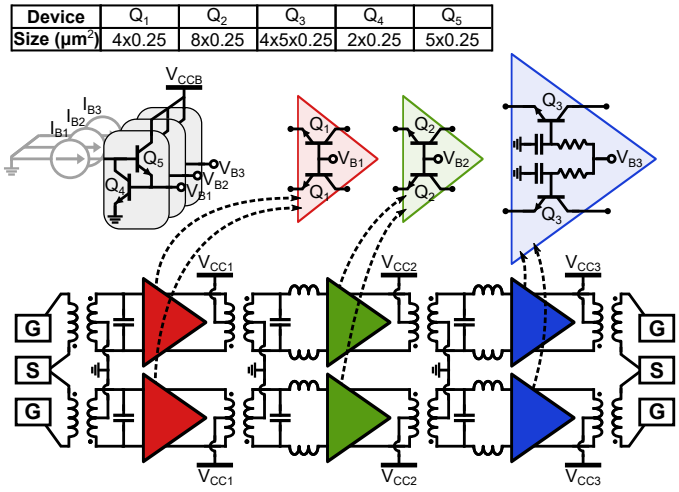


Fig. 1. Schematic of the power amplifier

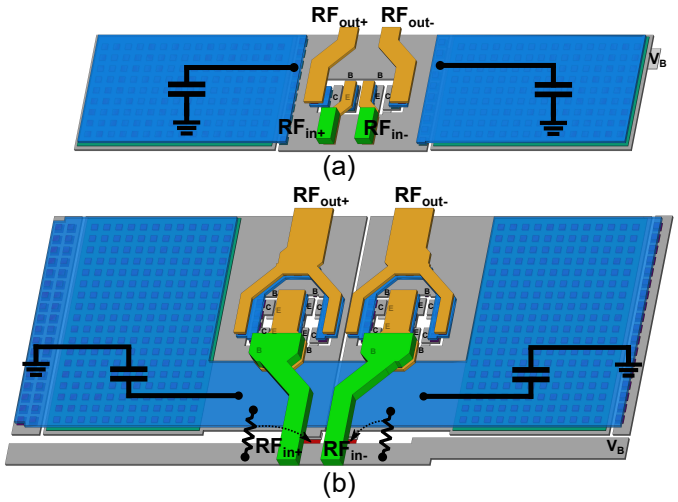


Fig. 2. Core layout of (a) the driver stages and (b) the PA stage

DC ground. Through-substrate vias and ground plane slots are used to suppress substrate modes.

The input stage is biased in moderate class AB and is sized big enough to avoid compression while providing a broadband input match for the PA. The second stage is biased in deep class AB and sized such that the resulting gain expansion increases the OP_{1dB} of the PA.

B. Biasing Network

In order to achieve higher PAE at power backoff (PBO), the PA and driver stages are biased in deep class AB. Therefore the collector current increases with the input power. At the same time, the low β ($\sim$ 25) in this technology induces a considerable amount of base current that also increases with the input power. As the base should be able to pull this current from its basing network in order to prevent early gain compression of the PA, it should provide a low output impedance [7]. Figure 3 shows the simulated gain compression of the PA stage when it is biased with either a current mirror with emitter follower, a voltage source and a $50\,\Omega$ resistor

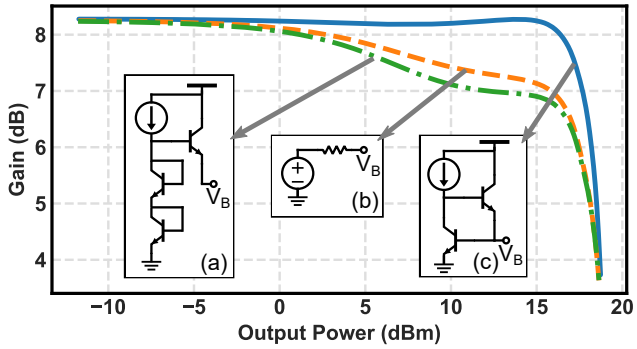


Fig. 3. Simulated gain compression of a PA stage when biased with (a) a current mirror with emitter follower , (b) a voltage source with resistor and (c) a buffered current mirror biasing network.

or a buffered current mirror. The buffered current mirror outperforms the other presented biasing networks as it provides the lowest gain compression for the PA, and thus it is used for all stages in the design. Due to the linearity enhancement of the biasing network, the driver stages can be sized more aggressively to increase the efficiency without compromising the linearity of the PA. The PA further benefits from the differential design as it allows this biasing network to be easily connected to the virtual ground nodes formed between the base terminals of the common-base stages.

The supply voltage of these buffers can be much lower than the rest of the PA in order to minimize the impact on efficiency. The base biasing network only consumes $5.5\,\%$ of the total power consumption of the PA at P_{1dB}.

C. Power combiner-divider

Current combining naturally increases the load-impedance seen by the power amplifier, making it an excellent match for the high load-line impedance originating from the high supply voltage in this technology. The designed PA uses a two-way transformer-based power combiner. The power combiner and GSG pads have a combined simulated insertion loss of a maximum $0.8\,\mathrm{dB}$ across the entire operating bandwidth of the PA. At the input, a similar transformer-based parallel power divider is used with an additional MIM capacitor to tune out the reactive part of the impedance. Combined with the common-base topology, this results in a very broadband input match, as seen in the measurement results.

III. Measurement Results

The amplifier is fabricated in a 250-nm InP HBT process, and figure 4 shows the die photo. The dimensions of the chip are $682\,\mu\mathrm{m} \times 900\,\mu\mathrm{m}$. The chip is mounted on a standard FR4 PCB and is wire bonded to provide the supplies and bias currents. Wire bond capacitors are used on the supply lines to handle the high dynamic current consumption caused by the deep class AB operation of the PA. The input and output of the PA are probed using GSG probes with a pitch of $50\,\mu\mathrm{m}$. The PA and second driver stage supplies are set to $2.9\,\mathrm{V}$ for maximum linearity, while the input stage has a supply of $2.65\,\mathrm{V}$ for better overall efficiency. The bias buffer devices have a supply $2.0\,\mathrm{V}$.

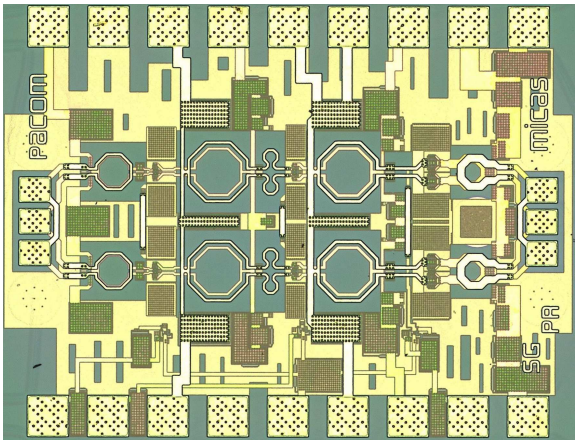


Fig. 4. Die photo of the power amplifier

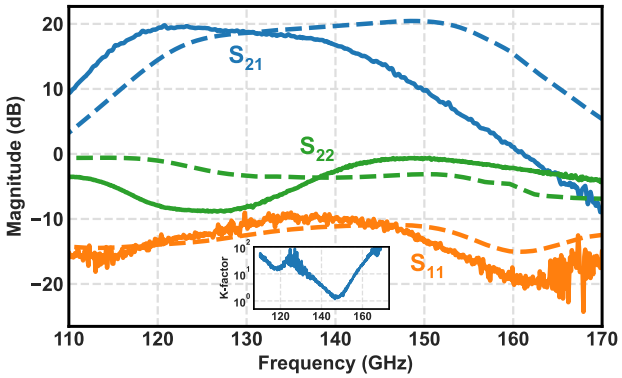
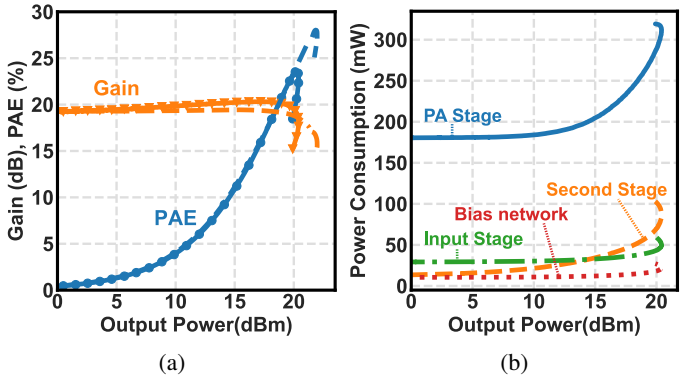


Fig. 5. Measured (solid) and simulated (dashed) S-parameters of the PA



(a) (b)

Fig. 6. (a) Measured (solid) and simulated (dashed) CW performance of the PA at 125 GHz (simulated at 140 GHz). (b) Measured DC power consumption of the PA stages at 125 GHz

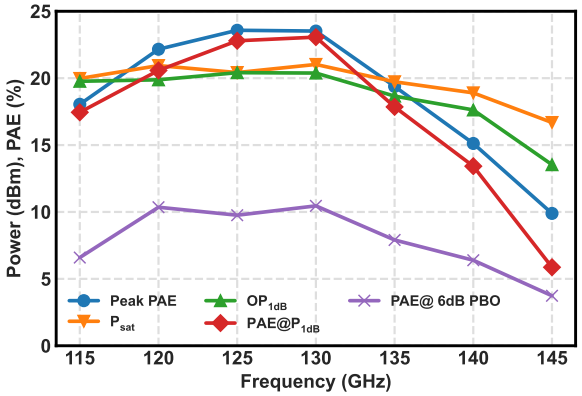


Fig. 7. Measured CW performance of the PA across frequencies

A. *Small-signal*

This small-signal S-parameters are measured using a R&S VNA in combination with D-band R&S VNA extenders. The VNA is calibrated using a CS-15 calibration substrate and LRRM calibration. The measured and simulated S-parameters are presented in figure 5. As shown in the figure, there is a frequency shift which can be attributed to errors in the model of the device parasitics. The PA has a peak gain of 19.8 dB and a 3-dB bandwidth of 24.4 GHz. The input match of the PA is better than −9.9 dB across the entire D-band. The K-factor of the PA is always greater than 1, indicating that the PA is unconditionally stable.

B. *Large signal*

For large signal measurement, the GSG probe loss is measured and the R&S D-band extenders are power calibrated using an Erickson PM5B power meter with the reference plane at the GSG probe mounting points. The measured probe loss and power calibration of the extenders allow the VNA to sweep the input power of the PA by varying the input power for the extenders.The measured large-signal S-parameters are used to calculate the output power of the PA. A waveguide attenuator is used at the output to prevent the PA from damaging the frequency extenders. The DC power consumption is measured using a combination of the R&S and Keysight PSU's built-in current measurements and a Keithley multimeter. The measured and simulated gain and PAE at 125 GHz is shown in figure 6a. In order to account for the shift, the simulated frequency is 140 GHz. The PA achieves a OP_{sat} of 20.4 dBm and a peak PAE of 23.6 %. The power consumption of the different PA stages is shown in figure 6b, showing that both the PA and second driver stage are operating in deep class AB. The large-signal performance over frequency is shown in figure 7. The PA maintains a OP_{1dB} and associated PAE of greater than 19.5 dBm and 16 % respectively from 115 GHz to 135 GHz.

C. *Modulated Signal Measurements*

The modulated signal measurement setup is shown in figure 8. The PA's average output power and input power are measured with a PM5B at the S-bend flanges. The EVM is measured without any predistortion and is normalized to the RMS value of the constellation point magnitudes. The average output power of the PA is set to the value that results in an EVM corresponding to a BER of $\sim 10^{-3}$ for the selected modulation type. The resulting constellation diagrams for 16-QAM, 32-QAM and 64-QAM modulated data are shown in figure 9. For 10 Gb/s 16-QAM, the PA achieves a record P_{avg} and PAE_{avg} of 16.3 dBm and 11.9 % respectively. Using frequency domain equalization, the PA achieves 24 Gb/s with −16 dB EVM for an average output power and PAE of 15.7 dBm and 10.6 % respectively. Thanks

Table 1. Comparison between state-of-the-art D-band PAs

Reference	**This work**		IMS'20 [2]	ISSCC'20 [3]	JSSC'22 [4]	JSSC'22 [8]	
Technology	**250-nm InP HBT**		250-nm InP HBT	16-nm FinFet	45-nm CMOS SOI	130-nm SiGe	
Frequency (GHz)	**115 - 140**		125 - 150	114 - 136	130 - 151	107 - 135	
Gain(dB)	**19.8**		20.3	20.5	24.8	21.8	
P_{sat}/OP_{1dB} (dBm)	**21/20.4**		20.5/17	15/9.2	18.5/13.5	22.6/17.1*	
PAE @ OP_{1dB} (%)	**23**		14*	5*	1.1*	12.7*	
PAE @ 6dB PBO (%)	**10.4**		2.4*	1.2*	<1*	11.7	
Modulation scheme	**16-QAM**	**64-QAM**	-	-	-	16-QAM	64-QAM
Data rate(Gb/s)	**10 (20[§])**	**6**	-	-	-	8	4.8
EVM (%)	**15.7(15.9[§])**	**7.95**	-	-	-	11.6[‡]	10.9[‡]
P_{avg} (dBm)	**16.3(15.7[§])**	**12.9**	-	-	-	13.7	13.8
PAE_{avg} (%)	**11.9(10.6[§])**	**6.5**	-	-	-	7.8	7.9
Area (mm^2)	**0.61(0.286[†])**		0.68	0.062(0.041[†])	0.46[†]	1.11(0.58[†])	

*= Graphically estimated. [†]= Core area not including DC and RF pads. [‡]= Measured using postdistortion.[§]= Measured using equalization

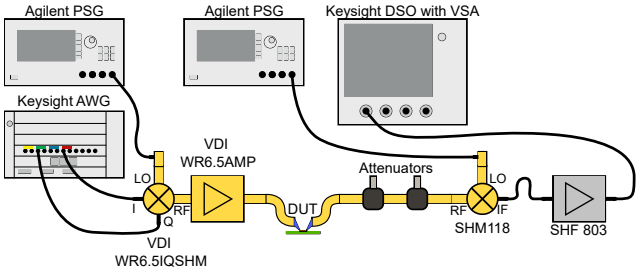


Fig. 8. EVM measurement setup

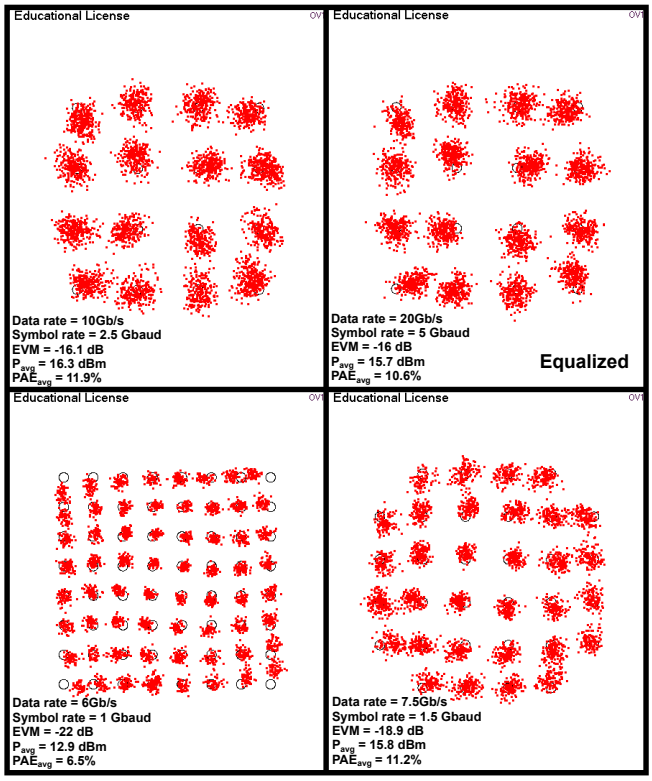


Fig. 9. Constellation diagram, EVM, P_{avg}, PAE_{avg} and data rate for 16-QAM, 32-QAM and 64-QAM modulation

to the high OP_{1dB} of the PA, it is able to operate very close to P_{sat} and still achieve reasonable EVM performance. For 64-QAM modulation, the PA has to operate very deep into PBO, mainly due to the AM-PM distortion that can be seen by the rotation of the outer points in the constellation diagram.

IV. Conclusion

This paper presentated a high-power, high-efficiency D-band amplifier in a 250-nm InP HBT technology. The use of transformers in combination with the common-base stages results in high efficiency and high output power. Moreover, the OP_{1dB} is very close to the P_{sat} thanks to the biasing network and deep class AB operation of the PA, allowing the PA to operate very close P_{sat} while still maintaining reasonable EVM. In comparison with other state-of-the-art D-band PAs in table 1, this PA provides the highest OP_{1dB} and the highest associated PAE. In modulated data measurements, the PA shows record P_{avg} and PAE_{avg}, making it suitable for D-band communication systems.

References

[1] M. J. W. Rodwell, J. Rode, H. W. Chiang, P. Choudhary, T. Reed, E. Bloch, S. Danesgar, H.-C. Park, A. C. Gossard, B. J. Thibeault, W. Mitchell, M. Urteaga, Z. Griffith, J. Hacker, M. Seo, and B. Brar, "THz Indium Phosphide Bipolar Transistor Technology," in *2012 IEEE Compd. Semicond. Integr. Circuit Symp. CSICS*, Oct. 2012, pp. 1–4.

[2] A. S. H. Ahmed, M. Seo, A. A. Farid, M. Urteaga, J. F. Buckwalter, and M. J. W. Rodwell, "A 140GHz power amplifier with 20.5dBm output power and 20.8% PAE in 250-nm InP HBT technology," in *2020 IEEEMTT- Int. Microw. Symp. IMS*, Aug. 2020, pp. 492–495.

[3] B. Philippe and P. Reynaert, "24.7 A 15dBm 12.8%-PAE Compact D-Band Power Amplifier with Two-Way Power Combining in 16nm FinFET CMOS," in *2020 IEEE Int. Solid- State Circuits Conf. - ISSCC*, Feb. 2020, pp. 374–376.

[4] S. Li and G. M. Rebeiz, "High Efficiency D-Band Multiway Power Combined Amplifiers With 17.5–19-dBm Psat and 14.2–12.1% Peak PAE in 45-nm CMOS RFSOI," *IEEE J. Solid-State Circuits*, vol. 57, no. 5, pp. 1332–1343, May 2022.

[5] Z. Liu, T. Sharma, C. R. Chappidi, S. Venkatesh, and K. Sengupta, "Transformer-based Broadband mm-Wave InP PA across 42-62 GHz with Enhanced Linearity and Second Harmonic Engineering," in *2020 IEEEMTT- Int. Microw. Symp. IMS*, Aug. 2020, pp. 1295–1298.

[6] C. M. Grens, J. D. Cressler, J. M. Andrews, Q. Liang, and A. J. Joseph, "The Effects of Scaling and Bias Configuration on Operating-Voltage Constraints in SiGe HBTs for Mixed-Signal Circuits," *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1605–1616, Jul. 2007.

[7] Y. Yang, K. Choi, and K. Weller, "DC boosting effect of active bias circuits and its optimization for class-AB InGaP-GaAs HBT power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 5, pp. 1455–1463, May 2004.

[8] X. Li, W. Chen, H. Wu, S. Li, X. Yi, R. Han, and Z. Feng, "A 110-to-130 GHz SiGe BiCMOS Doherty Power Amplifier With a Slotline-Based Power Combiner," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3567–3581, Dec. 2022.