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Impact of Nitridation on Bias Temperature Instability and Hard Breakdown Characteristics of SiON MOSFETs

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Abstract: We study how nitridation, applied to SiON gate layers, impacts the reliability of planar metal-oxide-semiconductor field effect transistors (MOSFETs) subjected to negative and positive bias temperature instability (N/PBTI) as well as hard breakdown (HBD) characteristics of these devices. Experimental data demonstrate that p-channel transistors with SiON layers characterized by a higher nitrogen concentration have poorer NBTI reliability compared to their counterparts with a lower nitrogen content, while PBTI in n-channel devices is negligibly weak in all samples independently of the nitrogen concentration. The Weibull distribution of HBD fields extracted from experimental data in devices with a higher N density are shifted towards lower values with respect to that measured in MOSFETs, and SiON films have a lower nitrogen concentration. Based on these findings, we conclude that a higher nitrogen concentration results in the aggravation of BTI robustness and HBD characteristics.

Keywords: bias temperature instability; hard breakdown; nitridation; nitrogen content; nitrided oxide; ramped voltages stress; SiON; SiO_2; transistor lifetime; defects

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1. Introduction

The breath-taking development of micro- and nanoelectronics relies on the rapid scaling of the metal–oxide–semiconductor field effect transistor (MOSFET) based on silicon. To meet requirements dictated by mobile/portable electronic products and applications for long battery lifetimes and hence reduced OFF-currents and optimized ON/OFF-current ratio, novel transistor architectures—starting from planar devices and going to 3D geometries such as finFETs [1,2] and continuing to nanosheet [3,4], forksheet [5–7], and complementary FETs [8,9]—have been introduced. However, before the launching of any new transistor node, its reliability characteristics should be carefully assessed together with the performance, power consumption, etc. Among reliability issues featured by modern MOSFETs, the most detrimental ones are bias temperature instability (BTI) [10,11], time-dependent dielectric breakdown/hard breakdown (TDDB/HBD) [12,13], and hot-carrier degradation (HCD) [14–16]. Although HCD has been repeatedly flagged as a very severe degradation concern in confined 3D transistor architectures [17,18], it lies outside the scope of this paper. The reason for that is that BTI and HBD are intimately linked with the gate stack quality, while HCD is rather related to carrier acceleration by the electric field, which is determined by the voltage partition in the transport (i.e., source-drain) direction [19–24]. Therefore, rather than focusing on the device architecture optimization aiming to mitigate HCD, the focus of this work is put on optimization of SiON layers to suppress such reliability issues as BTI and HBD.

Among various techniques aimed at alleviating BTI and improving breakdown characteristics of the gate stack, nitridation of the gate dielectric layers has been the subject of extensive studies performed by several groups. Regarding the impact of nitridation on TDDB/HBD, to the best of our knowledge, there are a very limited number of publications addressing this subject. Among them, are the papers by Joo et al. [25] and Mazumder et al. [26], which analyzed how nitridation in NO_2 ambient impacts TDDB and concluded that low-pressure nitridation results in the improvement of TDDB robustness, while nitridation at an increased pressure leads to poorer TDDB characteristics. A TDDB lifetime improvement due to annealing in the NO ambience was reported by Chen et al. [27], while Lee et al. [28] demonstrated that ex situ N annealing has a very weak impact on TDDB. Therefore, one can summarize these studies, and depending on nitridation conditions, this fabrication step can either improve TDDB/HBD robustness or aggravate it.

Very similar to the case of TDDB/HBD, a consensus regarding the impact of nitridation on BTI reliability has not been reached so far. On the one hand, several groups suggest that the incorporation of N into a gate stack suppresses BTI. Thus, O'Sullivan et al. demonstrated that N (or F) diffusion into the gate dielectric layer can shift the band of donor-like traps, thereby impeding negative BTI (NBTI) [29]. In [30], O'Connor et al. reported that N passivates traps in HfSiO layers but this behavior can be reversed during stress, thereby giving rise to NBTI and a stress-induced leakage current (which accompanies TDDB). Further, Maheta et al. [31] speculated that the impact of N on NBTI is very intricate and is comprised of changing properties of interface traps and oxide states, thereby resulting in different characteristic energies for trap activation and NBTI time exponents. Joshi et al. [32] published a reduction of BTI due to N incorporation. On the other hand, Garros et al. claimed that in their MOSFETs with high-*k*/metal gate stacks N results in severe aggravation of BTI reliability [33,34]. Their results are consistent with data published by Reisinger et al., which demonstrate stronger NBTI in nitrided oxides compared to non-nitrided ones [35]. Finally, Takasaki et al. [36] used the charge-pumping technique to resolve the interface trap density in devices with different parameters of the nitridation process subjected to BTI stress. Their results suggest that BTI aggravates transistors with a higher N content.

Renewed interest in BTI and HBD reliability of MOSFETs with nitrided gate oxides is related to the introduction of the forksheet transistor architecture, where n- and pFET sheets are separated by an Si_3N_4 (or SiON) wall. Recent experimental studies of reliability issues in forksheet FETs did not show extra charge trapping in the Si_3N_4 (or SiON) wall [37]. From the simulation perspective, this behavior was explained to be exclusively due to electrostatic reasons, i.e., the corresponding voltage partition in the forksheet wall [38]. However, for further boosting device reliability, it is important to understand whether N incorporation into SiO_2 and SiON films improves or aggravates transistor robustness. Moreover, the knowledge on the reliability of SiON gate stacks acquired in this work should also be of relevance for novel FET architectures employing SiON related materials outside their gate stack, e.g., in the forksheet FET wall, transistor spacers, etc.

Therefore, the scope of this paper is an experimental investigation on the impact of nitridation of gate SiON layers on BTI and HBD characteristics. We also aim at contributing towards reconciling controversies regarding the impact of nitridation on gate oxide reliability.

2. Devices

We employed planar n- and p-channel MOSFETs fabricated in a 300 mm line using a standard gate first flow. These transistors have a gate stack made of an SiON layer and a 100 nm polySi layer deposited in situ. To fabricate the SiON layer, first an SiO_2 film was grown by steam generation in a rapid thermal processing system and then this film was subjected to nitridation in the N_2 ambient, followed by a post-nitridation anneal. We used two types of nitridation processes:

- The process of reference (POR), which includes plasma nitridation at a higher value of the radio frequency (RF) power of 1000 W under a pressure of 20 Torr for 12 s.

- The alternative process with softer nitridation (SN) conducted at a lower RF power of 900 W under a pressure of 20 Torr for 12 s.

Let us emphasize that these two transistor splits are close to each other, but we have a narrow device target window specified by the targeted equivalent oxide thickness (EOT), the gate leakage current density, etc. Therefore, in order to ensure that these splits fit into the specified window, we were limited in variations of the fabrication process parameters.

Devices with a targeted physical thickness of the SiON layer of 1.9 nm were fabricated using both the POR (this sample is labeled as "S #1") and the process including the SN step (this sample is labeled as "S #2"), see Table 1. In addition to this, MOSFETs with a 2 Å thicker SiON layer (targeted physical thickness is 2.1 nm) were fabricated by the POR, (S #3, Table 1). Finally, with the SN-based process, transistors with a 2 Å thinner SiON film (targeted thickness is 1.7 nm, S #4 and 5) were also grown. The EOT values for all samples, obtained using capacitance-voltage measurements combined with the CVC model for EOT extraction [39], are summarized in Table 1. Within the EOT extraction procedure, the potential partition in the depleted poly-Si layer and correction due to quantum confinement at the Si/SiON interface were taken into account.

Table 1. Equivalent oxide thickness and threshold voltage values of samples used for BTI and HBD studies shown for n- and p-channel MOSFETs. EOT data are acquired using capacitance-voltage measurements, while for V_t extraction, the maximum transconductance method (at the drain voltage V_d of +0.05 and −0.05 V for n- and pMOSFETs, respectively) was employed. The last column shows the N content rank. A higher rank corresponds to a higher concentration, i.e., '1' corresponds to the lowest N content and '4' to the highest N concentration.

Sample	Details	EOT, nMOS	EOT, pMOS	V_t, nMOS	V_t, pMOS	N Content Rank
S #1	POR	1.48 nm	1.37 nm	0.23 V	−0.22 V	3
S #2	SN	1.54 nm	1.48 nm	0.28 V	−0.17 V	1
S #3	POR + 2 Å	1.78 nm	1.66 nm	0.29 V	−0.20 V	2
S #4	SN − 2 Å	1.49 nm	1.34 nm	0.13 V	−0.27 V	4
S #5	SN − 2 Å	1.47 nm	1.28 nm	0.13 V	−0.27 V	4

Threshold voltage values were extracted from transfer characteristics ($I_d - V_g$, where I_d is the drain current and V_g is the gate voltage) using the maximum transconductance method; see Table 1. From Table 1, it can be observed that although samples S #4 and S #5 have the same targeted thickness, which is 2 Å less than that of the POR device (sample S #1), in practice, their EOT is comparable to the EOT of the reference sample (sample S #1). In addition, their V_t values substantially deviate from those of other samples. As a consequence, one can expect that S #4 and S #5 have an inferior reliability among the entire set of devices.

The extracted threshold voltage values are consistent with the parameters of the nitridation step. Indeed, N incorporated in the gate dielectric is known to result in positive charges distributed throughout the layer, which, in turn, induce a threshold voltage shift towards lower values. Samples #1 and 2 have the same targeted physical thickness, but, in the latter case, nitridation was carried out with lower power; therefore, S #2 has a lower N content compared to S #1. The corresponding V_t voltages are consistent with this trend, i.e., V_t values of S #2 are higher for both n- and pMOSFETs as compared to those of S #1. The wafers S #4 and 5 were fabricated by the same process as S #2, but the physical thickness of their SiON layers is the lowest among all devices used in this study; therefore, they have the highest concentration of nitrogen and hence the lowest values of V_t. Finally, for S #1 and 3, the same nitridation process was employed; however, the wafer S #3 has a 2 Å thicker SiON layer and therefore a lower N content and higher threshold voltages. A summary of N content can be found in the last column of Table 1, where a higher rank corresponds to a higher concentration, i.e., '1' corresponds to the lowest N content and '4' to the highest N concentration.

We would like to note that although a comparison of BTI and HBD characteristics of MOSFETs with SiON films against those acquired in devices with pure SiO_2 as a gate dielectric would be informative, such a comparison was not performed in this study. The reason for that is that the reliability measurements were carried out to qualify the gate oxide integrity for the 65 nm technology node with polySi/SiON gate stack. Therefore, in this EOT range (see Table 1), it is required to employ SiON as high-k dielectric to ensure lower gate leakage and better electrostatic control of the channel. Consequently, we do not have SiO_2-based MOSFETs at our disposal.

3. Experiment and Data Processing

In ultra-scaled FETs, characteristics of pristine devices can vary from sample-to-sample. This is called "time-zero variability" [40], which originates from several sources such as random dopant fluctuations, metal gate granularity, line edge roughness, fluctuations in material properties, oxide thickness variations, etc. [41–46]. Degradation of device characteristics is due to generation/activation of defects. Ultra-scaled FETs contain just a handful of defects (and their precursors), which are randomly distributed throughout a transistor; therefore, contributions of individual defects to degradation can be discernible. Thus, BTI and HCD types of stress leads to time-dependent variability in small-area MOSFETs [47–49]. In contrast, in large-area devices, BTI/HCD is due to a collective response of a very large number of defects, and a sample-to-sample scattering of degradation characteristics is not prominent. Hence, in order to avoid BTI-induced variability, we intentionally chose large-area devices. Regarding TDDB/HBD, this type of degradation is driven by defect build-up across the dielectric film resulting in the formation of a percolation path. Hence, for the processing/interpretation of experimental HBD data, stochastic approaches are typically employed for both large- and small-area devices [12,50]. To summarize, for BTI and HBD measurements, we chose MOSFETs with a gate length (L_g) and a width (W) of 1 µm.

The studied samples were subjected to ramped voltage stress (RVS) in BTI and HBD regimes at room temperature. For both degradation modes, we used the RVS technique developed by Kerber et al. [51,52]. Note that for BTI, the extended measure–stress–measure procedure (eMSM) [53] is commonly employed, while for HBD studies, the standard routine is constant voltage stress (CVS) [54–56]. Despite the fact that the eMSM and CVS techniques provide a more comprehensive insight into BTI and HBD, respectively, the RVS scheme was proven to have same accuracy for both BTI [51,52] and TDDB/HBD [57] degradation modes. On the other hand, the RVS technique allows us to dramatically reduce the experimental time, thereby making itself the routine of choice for conducted BTI and HBD investigations.

In these experiments, n-channel transistors were stressed under positive gate bias V_g (in both BTI and HBD regimes), while their p-channel counterparts were subjected to RVS stress at negative V_g.

3.1. Bias Temperature Instability

The RVS measurement procedure for BTI, which is comprised of sense and stress phases, is schematically depicted in Figure 1. Prior to BTI stress, $I_d - V_g$ curves in a limited V_g range (we used $|V_g|$ sweeping the range of [0; 1.0] V) of pristine transistors were measured. $I_d - V_g$ characteristics were then employed to extract the V_t value and the corresponding drain current $I_t = I_d\ (V_g = V_t)$. Next, we applied a stress pulse of a duration of t_{stress} with an increasing amplitude: for the stress phase i, the signal amplitude is $V_{g,start} + i \times V_{g,step}$. These ramps sweep the voltage range of $[V_{g,start}; V_{g,stop}]$, increasing the amplitude each time by $V_{g,step}$, see Figure 1. Each stress phase labeled with i is followed by a phase (with the same index i) when we interrupt the stress and extract V_t.

V_t is determined as the gate voltage which satisfies the criterion: $I_t = I_d(V_g)$; see Figure 2. The obtained value is $V_t(t)$, with t being the cumulative stress time: $t \approx i \times t_{stress}$. Therefore, the stress-induced shift in the threshold voltage is determined as $\Delta V_t = | V_t(t) - V_t(0) |$.

Another important parameter of the RVS routine is the ramp rate $RR = V_{g,step}/t_{stress}$. It is noteworthy that a lower RR, ceteris paribus, results in a larger ΔV_t. This is because the stress time at each voltage step is longer for the slower ramp rate (i.e., if the $V_{g,step}$ value is constant and t_{stress} is longer, then their ratio $V_{g,step}/t_{tstress}$, defined as RR, is lower). For each RR value and type of MOSFETs (i.e., n- and p-channels and the fabrication process flow) we used eight samples.

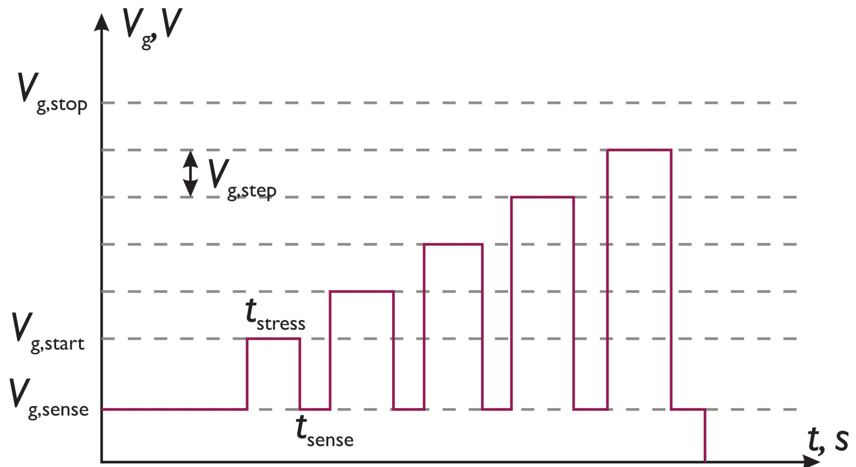

Figure 1. Schematic representation of RVS BTI measurements.

For NBTI measurements, we used the following parameters: $V_{g,start} = V_t - 0.4\,\text{V}$, $V_{g,stop} = V_t - 4.0\,\text{V}$; the voltage step $V_{g,step}$ and the pulse duration t_{stress} were chosen to ensure five different ramp rates of 0.1, 0.3, 1.0, 3.0, and 7.5 V/s. The drain voltage V_d was set to $-0.05\,\text{V}$. PBTI measurements were conducted in a similar fashion with $V_{g,start} = V_t + 0.4\,\text{V}$, $V_{g,stop} = V_t + 4.0\,\text{V}$, and RR = 0.1, 0.3, 1.0, 10.0, and 3.3 V/s; V_d = 0.05 V.

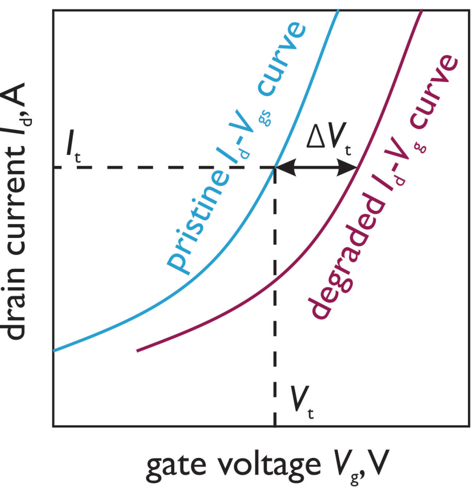

Figure 2. Schematic representation of the ΔV_t extraction technique. First, the $I_d - V_g$ curve of the pristine device is measured, thereby allowing the extraction of V_t and I_t. Next, at each stress time step t, $V_t(t)$ is determined as the gate voltage at which $I_d(V_g) = I_t$ and therefore $\Delta V_t(t) = V_t(t) - V_t(0)$.

To process BTI data acquired using the RVS routine, we assume the following ΔV_t dependency on the stress time and gate bias:

$$\Delta V_t \approx A_0 \left(\frac{|V_g - V_t(0)|}{t_{ox}} \right)^{\gamma} t^n = A_0 \left(\frac{|V_{ov}|}{t_{ox}} \right)^{\gamma} t^n = A_0 E_{ov}^{\gamma} t^n, \tag{1}$$

where A_0 is a prefactor (accounting for the thermal activation of the BTI process), t_{ox} is the EOT of the gate dielectric layer, $V_{ov} = V_g - V_t$ is the overdrive voltage, $E_{ov} = V_{ov}/t_{ox}$, while n and γ are exponents determining time dependency and field acceleration of BTI, respectively. According to Kerber et al. [51,52], this formula can be rewritten in a manner to link ΔV_t to the ramp rate RR:

$$\Delta V_t = \frac{A_0}{\left(\frac{\gamma}{n}+1\right)^n} E_{ov}\, RR^{-n}. \tag{2}$$

Therefore, if the threshold voltage shift was measured as a function of V_{ov}/E_{ov} and the RR, its time dependency can be extracted.

3.2. Hard Breakdown

In case of HBD, we used the scheme very similar to the RVS BTI measurement routine. However, instead of the sense phase, we monitored the gate leakage current I_g. In order to detect an HBD event, which manifests itself by an abrupt increase in the gate current observed at a stress voltage V_{BD}, we aimed at sweeping the $[V_{g,start}; V_{g,stop}]$ range with the minimum $V_{g,step}$ available at our measurement setup. Therefore, for HBD in nMOSFETs, we employed $V_{g,start} = 0.0$ V, $V_{g,stop} = 5.0$ V, and $V_{g,step} = 0.01$ V; for the ramp rate, we used a single value of RR = 0.09 V/s. pMOSFETs were stressed at $V_{g,start} = 0.0$ V, $V_{g,stop} = -5.0$ V. In all cases V_d = 0 V. For acquiring a comprehensive statistical set required for the extraction of the breakdown voltage distribution, we used 48 samples for each channel polarity and type of transistors (summarized in Table 1).

Extracted V_{BD} values are then binned into a Weibull distribution. First, using the Bénard approximation [58], we calculate probabilities $F_i = F_i(V_{BD,i})$ and then convert them to weibits W_i. Next, we fit the $W(V_{BD})$ dependency with a Weibull distribution and extract its parameters β (the shape factor) and η (the scale factor). To achieve this goal, we use the maximum likelihood estimation method.

4. Results and Discussion

4.1. Bias Temperature Instability

In RVS BTI measurements, at each sense phase, we recorded the drain current I_d and plotted I_d values as a function of stress voltage V_g. An example of these I_d traces obtained during NBTI stress for the pMOSFET fabricated using soft nitridation and with the targeted SiON thickness of 1.9 nm (wafer S #2) is given in Figure 3. The degradation of the device performance manifests itself by I_d reduction, and, this reduction, as discussed before, becomes more pronounced at lower ramp rates. The recorded I_d dependencies allowed us to extract threshold voltage shifts ΔV_t for each sense phase.

For all five pMOSFETs subjected to *NBTI*, dependencies of the threshold voltage ΔV_t shift on $E_{ov} = V_{ov}/t_{ox}$ are shown in Figures 4–8. ΔV_t changes are mean values obtained by averaging over the entire ensemble of eight $\Delta V_t(E_{ov})$ curves measured at a given RR rate. In Figures 4–8, the error bars for threshold voltage changes are also shown; we conclude that although standard deviations of $\Delta V_t(E_{ov})$ values are discernible, they are small. One can observe that ΔV_t values become larger at lower ramp rates and this trend agrees with Equation (2). Another pronounced peculiarity is that at high electric fields of $E_{ov} \sim 20$ MV/cm, the slope of $\Delta V_t(E_{ov})$ dependencies increases; this behavior is typical for all considered samples. Such a peculiarity is most probably related to non-equilibrium BTI driven by electrons traveling in the SiON conduction band, which can gain substantially high energies due to acceleration by the electric field and induce hydrogen release at the SiON/Si interface. Generation of interface traps according to this scenario was reported by the group from IBM [59,60] and recently by Bastos et al. [61]. However, this process occurs at very high electric fields and is related to another physical mechanism than that responsible for "conventional" BTI. Hence, we do not consider this degradation scenario

while extracting device time-to-failure (TTF). It is worth mentioning that BTI measurements continued up to high V_g values, and before reaching these voltages most of the devices broke down. During the processing of BTI data, we applied a filtering of HBD-induced current jumps; therefore, HBD events are not pronounced in Figures 4–8.

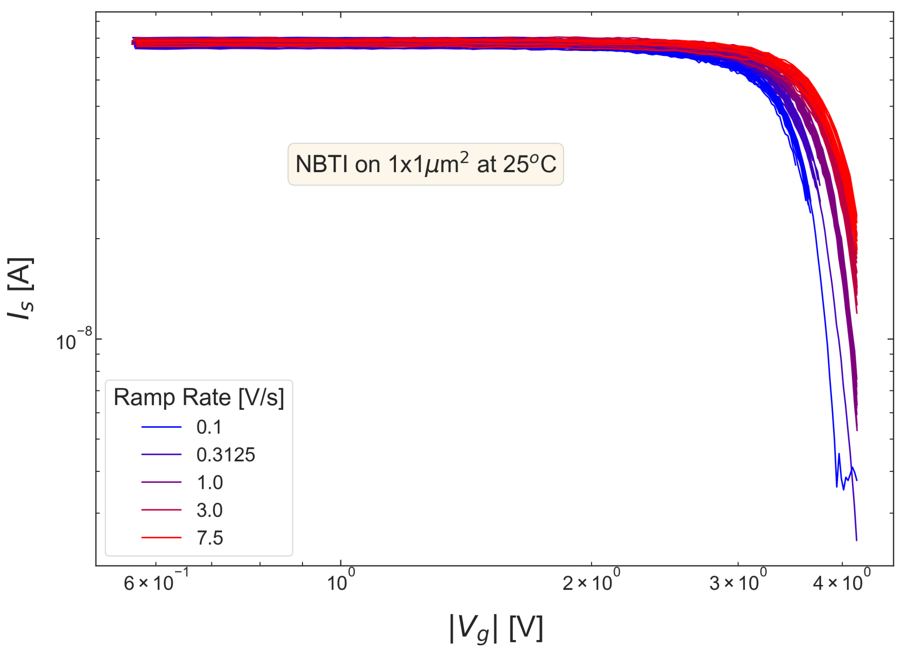

Figure 3. The typical evolution of the source-drain current I_s during RVS NBTI stress. These current values were measured during sense phases. One can observe that I_s decreases with the stress voltage; this decrease is a manifestation of device degradation during NBTI. At a lower ramp rate, the I_s change is more pronounced. The data are shown for the SN pMOSFET with the targeted physical thickness of 1.9 nm (S #2).

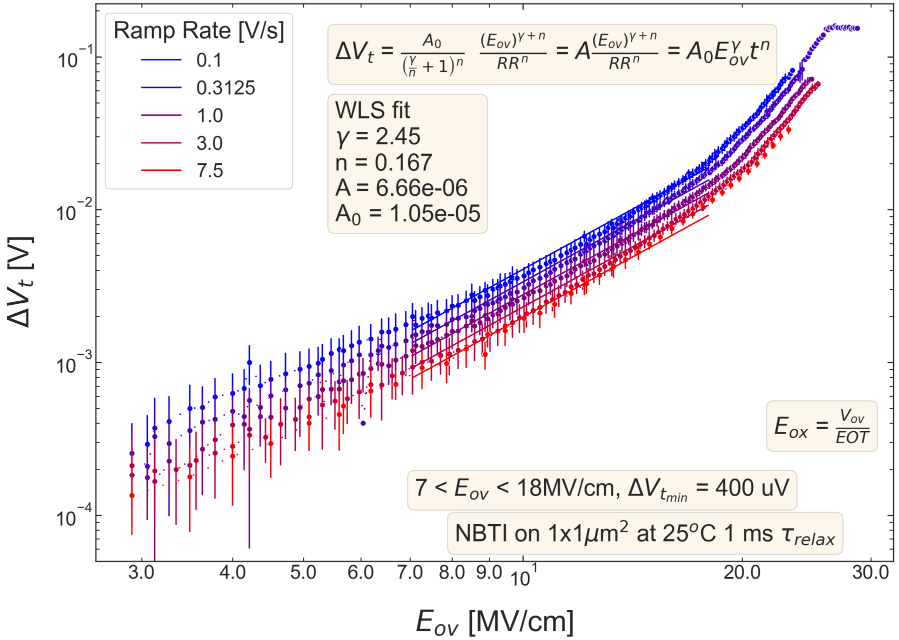

Figure 4. S #1 (POR), pMOSFETs: the threshold voltage shift ΔV_t caused by NBTI in pMOSFETs as a function of the overdrive oxide field E_{ov}. The experimental $\Delta V_t(E_{ov})$ dependency is reproduced by Equation (1).

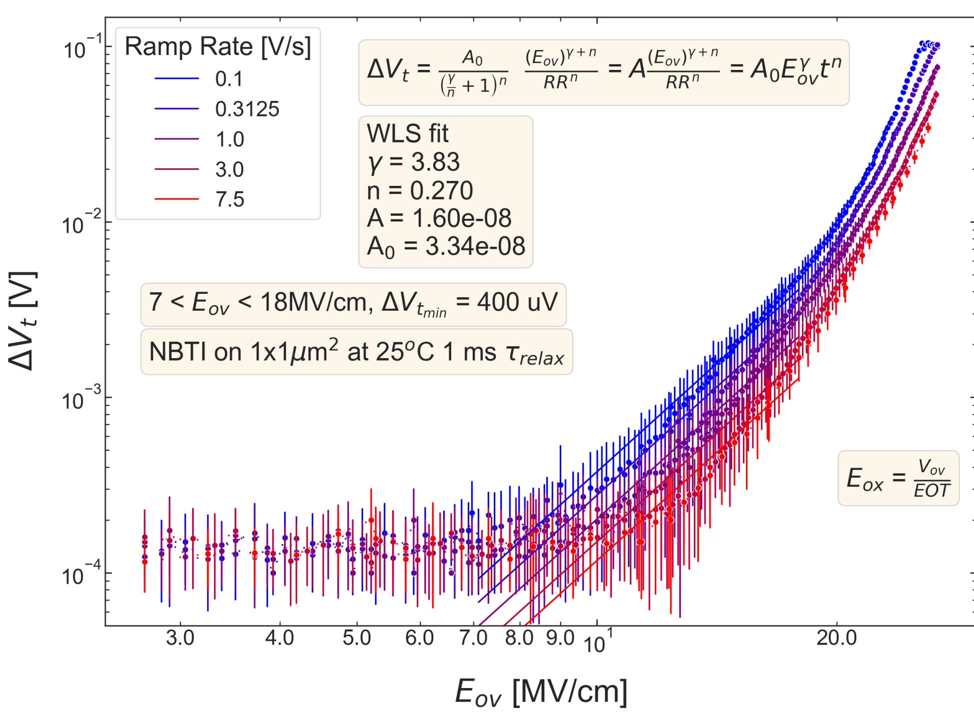

Figure 5. The same as Figure 4 but for S #2 (SN).

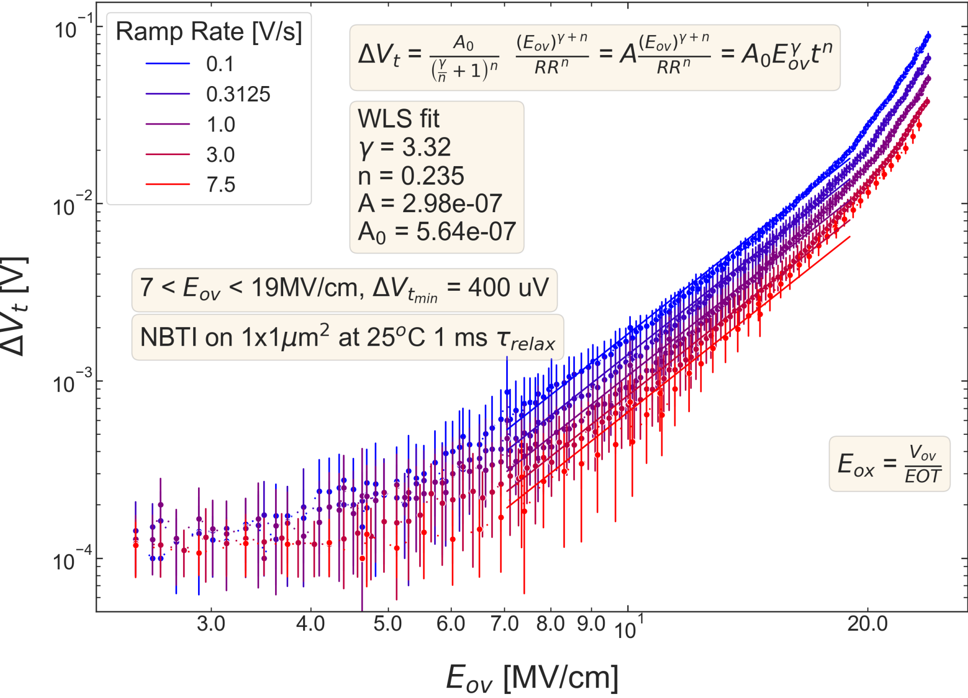

Figure 6. The same as Figure 4 but for S #3 (POR + 2 Å).

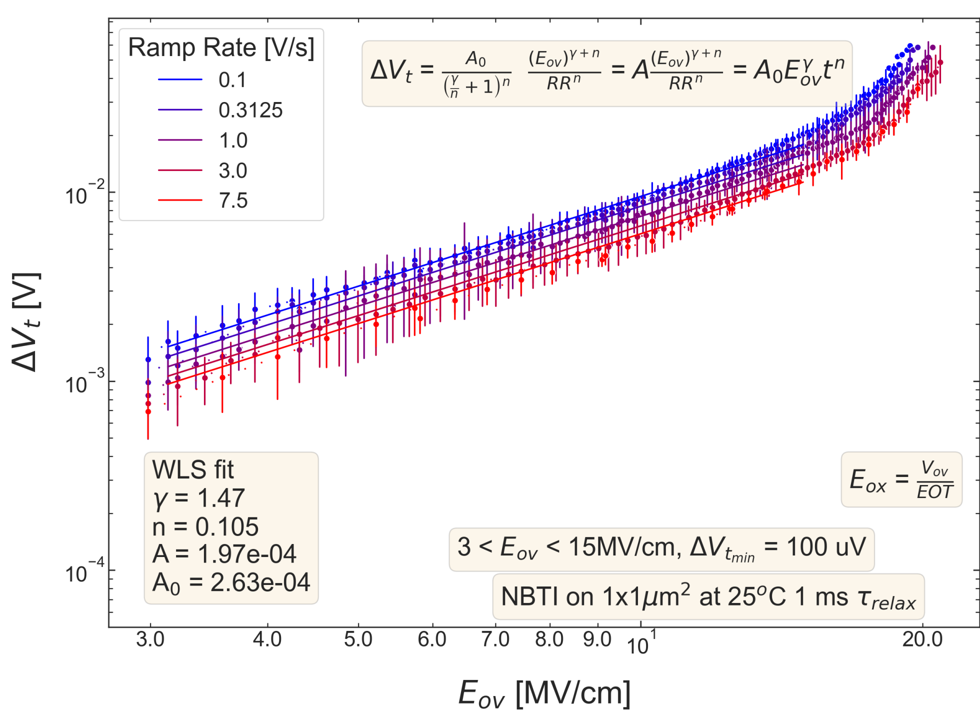

Figure 7. The same as Figure 4 but for S #4 (SN − 2 Å).

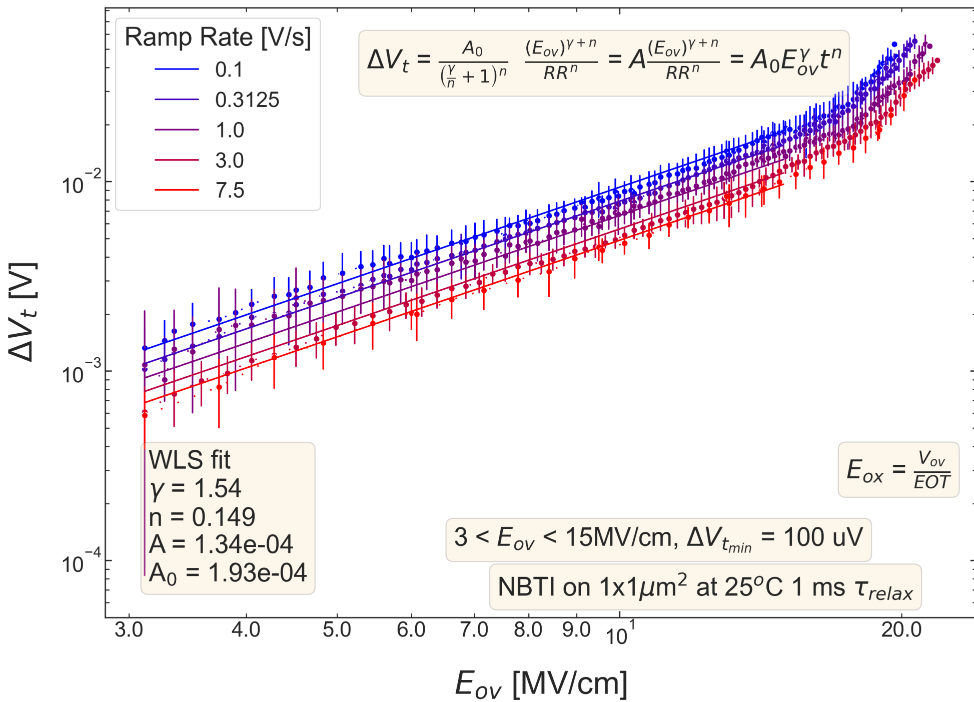

Figure 8. The same as Figure 4 but for S #5 (SN − 2 Å).

Experimental $\Delta V_t(E_{ov})$ curves were captured by formula (2) and the exponents γ and n were extracted; from Figures 4–8, it can be observed that the agreement is good. For the fitting procedure, we employed the weighted linear regression method. Note that under a considerable threshold voltage shift, we assume $\Delta V_t \gtrsim 1\,\text{mV}$; therefore, V_t values below this level were down-weighted. This also resulted in a more narrow—compared to the range determined by the used $V_{g,\text{start}}$ and $V_{g,\text{stop}}$ values (Figure 1)–E_{ov} range. For instance,

one can observe that for S #2 (Figure 5) we carried out fitting for $E_{\rm ov} \geq 7\,\rm MV/cm$ because at lower fields the threshold voltage shift is below 1 mV, i.e., negligibly small. In contrast, NBTI demonstrated by samples S #4 and 5 is much more significant; therefore, we could fit experimental data without limiting the $E_{\rm ov}$ range at the low value side. We also avoided the aforementioned $E_{\rm ov}$ region with a higher slope of the $\Delta V_{\rm t}(E_{\rm ov})$ curve (e.g., for S #1, this change is visible at $E_{\rm ov} \sim 17\,\rm MV/cm$, see Figure 4). Considering this $E_{\rm ov}$ range would result in an overestimated TTF value, which is determined as a stress time at which $\Delta V_{\rm t}$ reaches a margin of 30 mV. This is because we extract the device lifetime by extrapolating the dependency of $\Delta V_{\rm t}$ on $V_{\rm ov}$ (or $E_{\rm ov}$) from the experimentally available range to cover the operating voltage ($V_{\rm dd}$) value. However, a steeper $\Delta V_{\rm t}(V_{\rm ov})$ curve would result in a smaller $\Delta V_{\rm t}(V_{\rm dd})$ shift and hence larger TTF.

From Figures 4–8, one can observe, that, as expected (see Section 2), devices S #4 and 5 have poor NBTI characteristics, i.e., relatively high $\Delta V_{\rm t}$ values already at a low $E_{\rm ov}$; the most gradual slope of $\Delta V_{\rm t}(E_{\rm ov})$ curves determined by the parameter γ. On the contrary, the MOSFET S #2, which received soft nitridation and has a larger physical thickness of SiON than S #4 and 5, features the best NBTI reliability throughout the entire sample selection: negligibly small $\Delta V_{\rm t}$ shift up to $E_{\rm ov} \sim 8\,\rm MV/cm$ and the largest value of the exponent γ. If we compare S #1 and S #3, which have the same process flow but differ in the targeted physical thickness, one can observe that the latter one (with a lower N content) has substantially better NBTI reliability. Based on data presented in Figures 4–8, we conclude that MOSFETs with a lower N concentration (see Table 1) in their SiON layers demonstrate superior NBTI behavior.

Figures 9–13 summarize stress time values t corresponding to $\Delta V_{\rm th} = 30\,\rm mV$ plotted as a function of $V_{\rm ov}$ for all devices. These curves allow us to determine the upper limit of the safe operating area of these devices, as the $V_{\rm ov}$ value of each device lifetime is equal to 10 years. As consistent with the data set from Figures 4–8, S #4 and 5 have the lowest $V_{\rm ov}(t = 10\,\rm yrs)$ voltages, while S #2 is again the winner. More general, MOSFETs with a lower nitrogen content have longer TTF values.

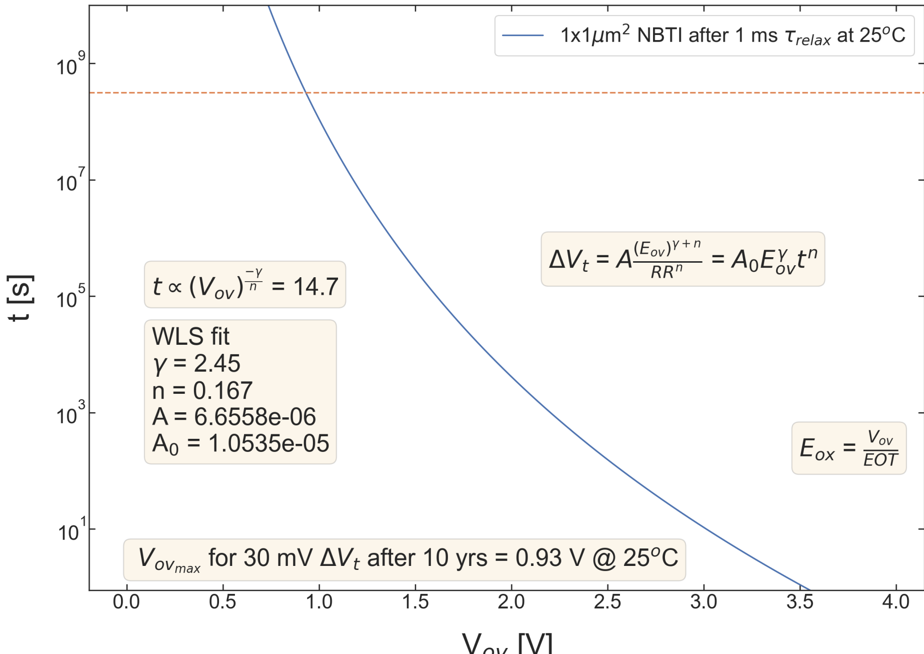

Figure 9. S #1 (POR), pMOSFETs: device time-to-failure (corresponding to the threshold voltage shift of $\Delta V_{\rm t} = 30\,\rm mV$) as a function of the overdrive voltage $V_{\rm ov}$. The upper limit of the safe operating area is determined as the $V_{\rm ov}$ corresponding to TTF of 10 years.

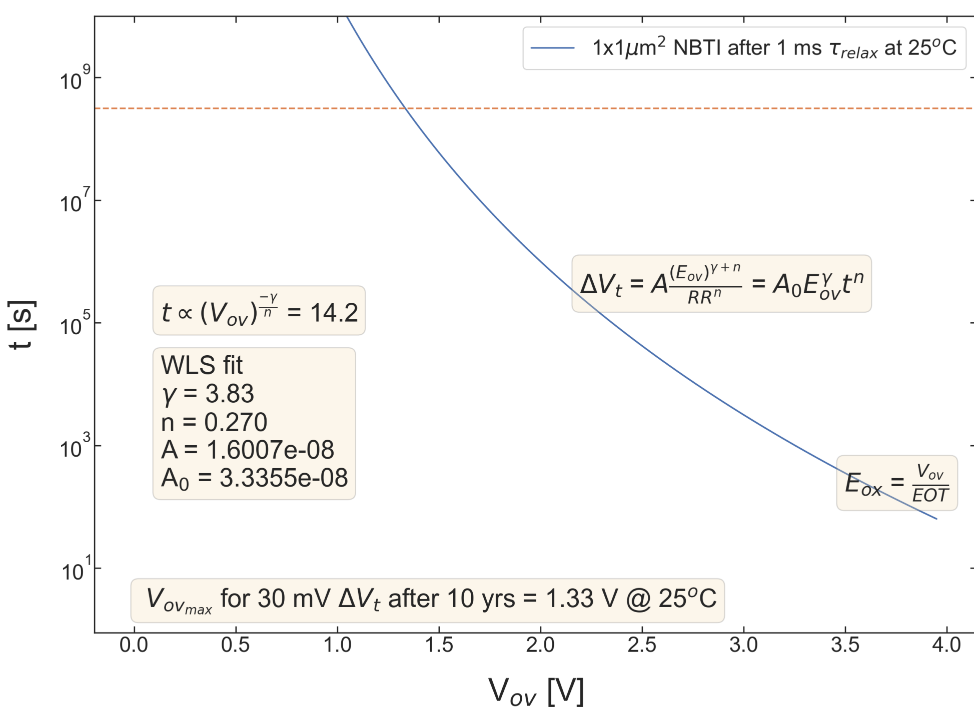

Figure 10. The same as Figure 4 but for S #2 (SN).

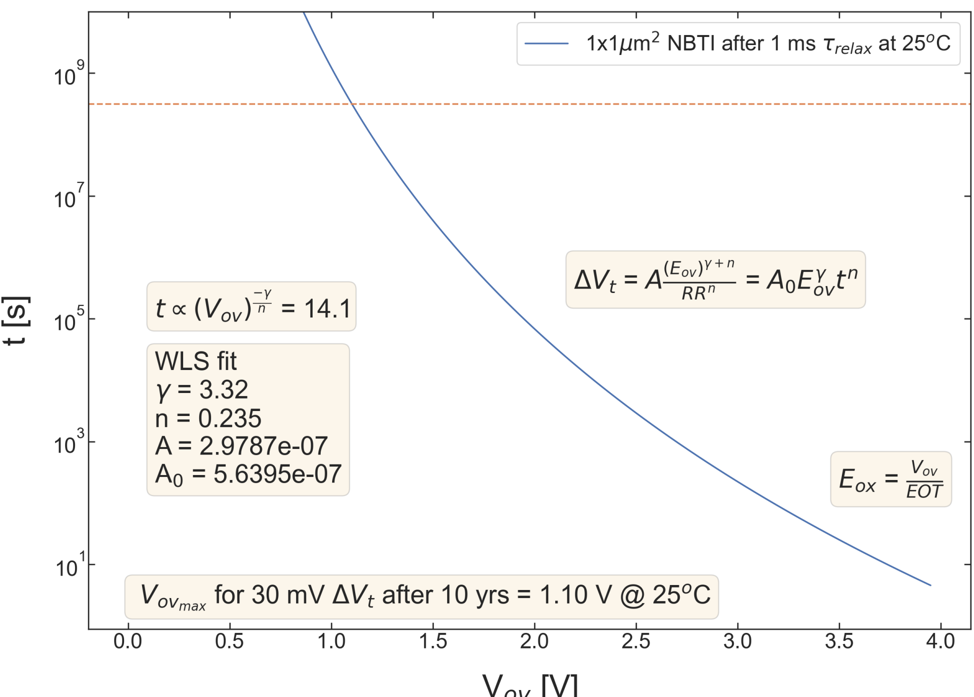

Figure 11. The same as Figure 4 but for S #3 (POR + 2 Å).

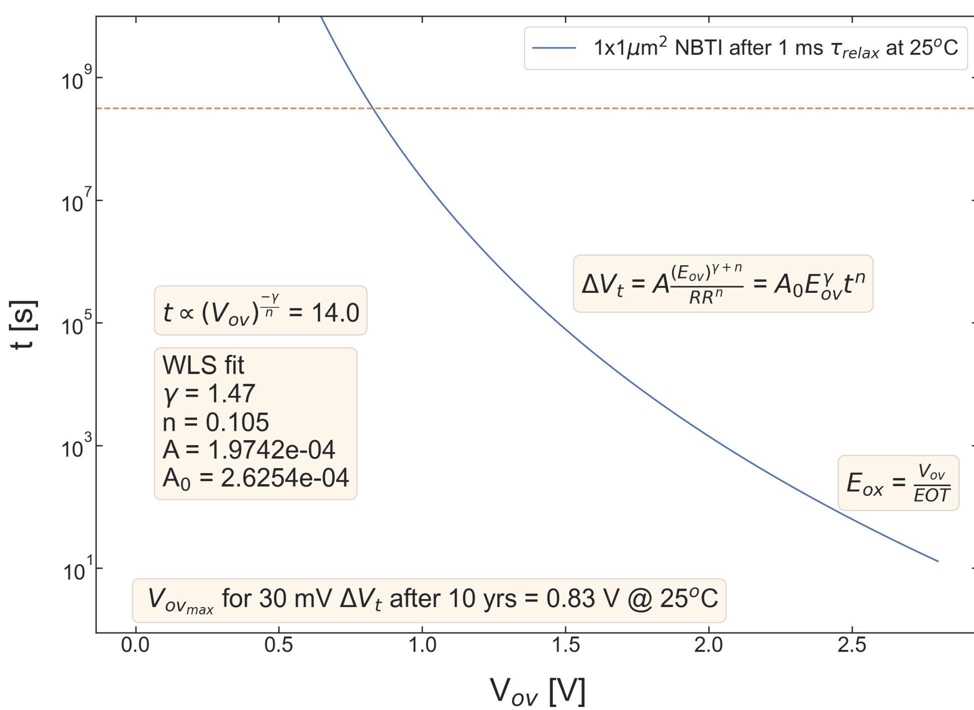

Figure 12. The same as Figure 4 but for S #4 (SN − 2 Å).

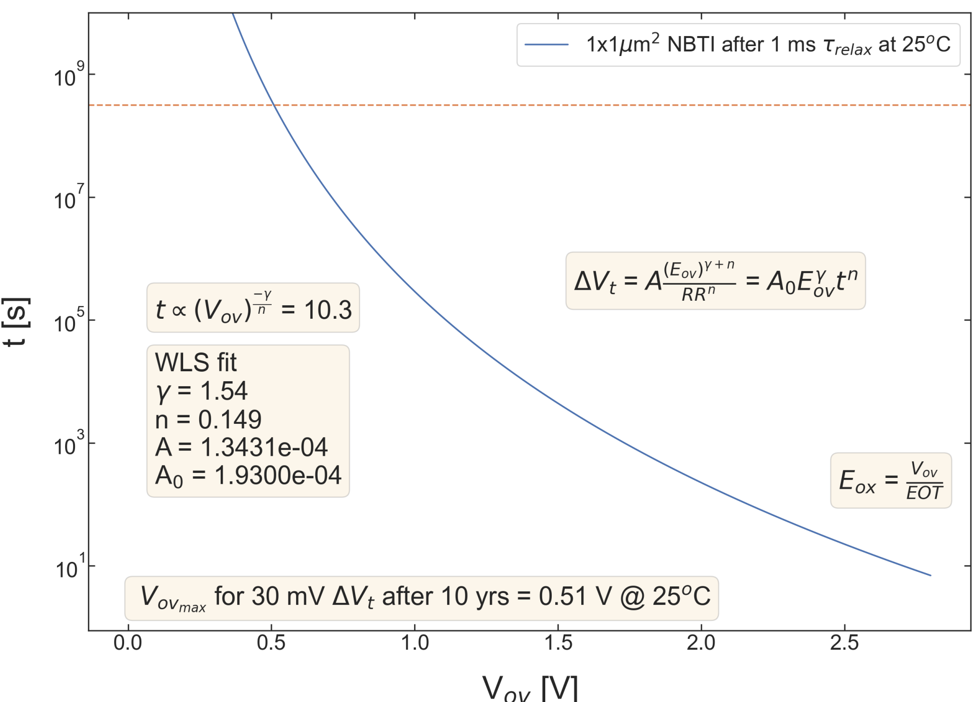

Figure 13. The same as Figure 5 but for S #5 (SN − 2 Å).

PBTI stress was applied to nMOSFETs. Figure 14 summarizes $\Delta V_\mathrm{t}(E_\mathrm{ov})$ curves obtained using samples from the wafer with the SiON film, which was grown by the POR and has the targeted thickness of 1.9 nm (S #1). It is pronounced that at low electric fields, ΔV_t values hardly overcome the noise level, and values measured at different ramp rates are not discernible. Even at such a high field as $E_\mathrm{ov} = 20\,\mathrm{MV/cm}$, the threshold voltage shift reaches a level of 4 mV, thereby suggesting that PBTI is very weak. Due to this reason,

we perform neither a fitting of $\Delta V_t(E_{ov})$ with Equation (2) nor an extraction of the V_{ov} corresponding to TTF of 10 years at the margin of $\Delta V_t = 30$ mV. Let us emphasize that this behavior is typical for all samples examined in this work (data are not shown). Therefore, we can conclude that in all these nMOSFETs, the PBTI is negligibly weak; therefore, we cannot judge which samples demonstrate superior PBTI reliability.

Note that weak PBTI in nMOSFETs is very typical for transistors with silicon oxides/nitrides [10]. This can be explained assuming that the physical mechanism underlying BTI is the capture/emission of charge carriers by/from traps in the dielectric layer [11], and, in the case of PBTI in n-channel FETs with SiO_2/SiON/SiN gate dielectric layers, the energetical position of the trap band is so that these traps are not accessible for the carriers (which are inversion electrons in the case of PBTI in nMOSFETs) [62].

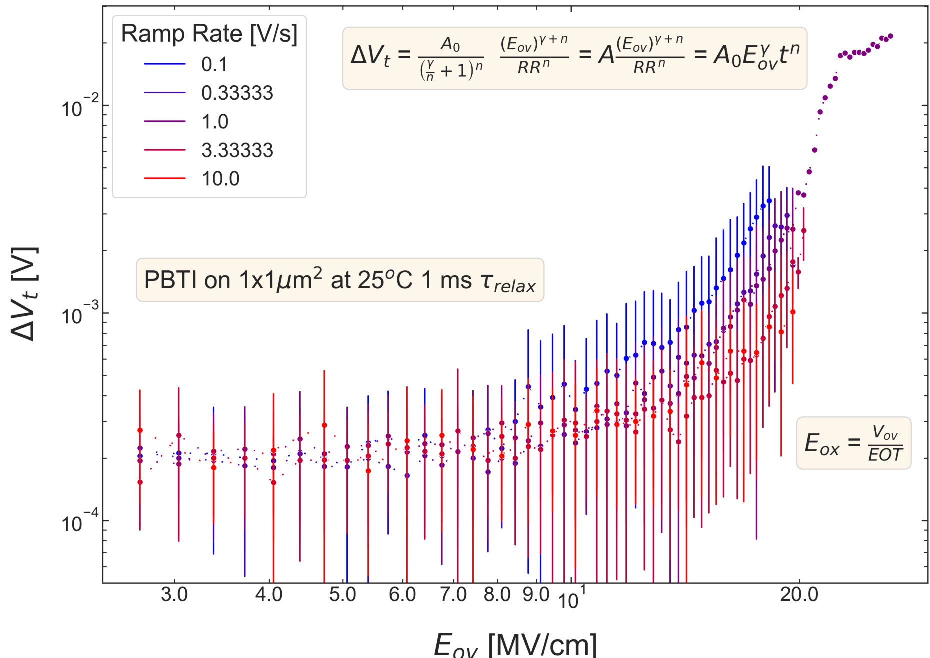

Figure 14. $\Delta V_t(E_{ov})$ dependencies measured during PBTI stress applied to the MOSFET which was fabricated by the POR process and has the targeted SiON thickness of 1.9 nm (S #1). One can observe that at the highest E_{ov} value of $\sim$ 20 MV/cm, the threshold voltage shift hardly reaches 4 mV; therefore, we can conclude that PBTI is negligibly weak. The same holds true for all other devices studied in this work (data sets for other devices are not shown in the paper).

4.2. Hard Breakdown

We compared HBD experimental data sets obtained only for MOSFETs with the targeted thickness of 1.9 nm fabricated by the POR (S #1) and with the SN step (S #2). Figures 15 and 16 show the gate current I_g as a function of stress gate voltage V_g for n-channel transistors from wafers S #1 and S #2, respectively. Gate voltage values corresponding to HBD events (V_{BD}) were extracted and binned into distributions, which are represented as Weibit plots in Figure 17. One can observe that the Weibull distribution of (V_{BD}) extracted for the transistor fabricated by the SN process is shifted by $\sim$ 0.2 V towards higher voltages compared to that obtained for the POR MOSFET. However, these samples have slightly different EOT values; therefore, the Weibull distribution of the breakdown field E_{BD} (the ratio between V_{BD} and EOT) shown in (Figure 18) appears to be more informative. From Figure 18, we conclude that the POR nMOSFET has lower breakdown fields compared to their counterparts fabricated with the softer nitridation step.

As for RVS-HBD in pMOSFETs, $I_g(V_g)$ dependencies for both POR and SN samples are shown in Figures 19 and 20, respectively. The extracted V_{BD} (Figure 21) and E_{BD} (Figure 22) distributions confirm again that the SN sample has superior HBD robustness. However,

the shift of the E_{BD} distribution towards higher E_{BD} values for the SN sample with respect to that extracted for the POR sample is not significant.

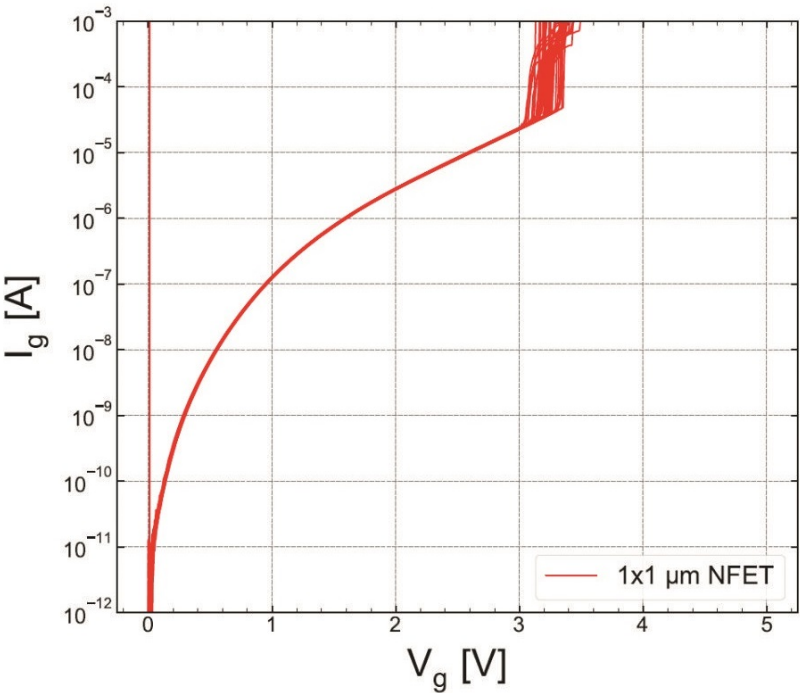

Figure 15. Gate current I_g as a function of stress voltage V_g recorded during RVS HBD measurements conducted on the POR nMOSFET with the targeted SiON thickness of 1.9 nm (sample S #1).

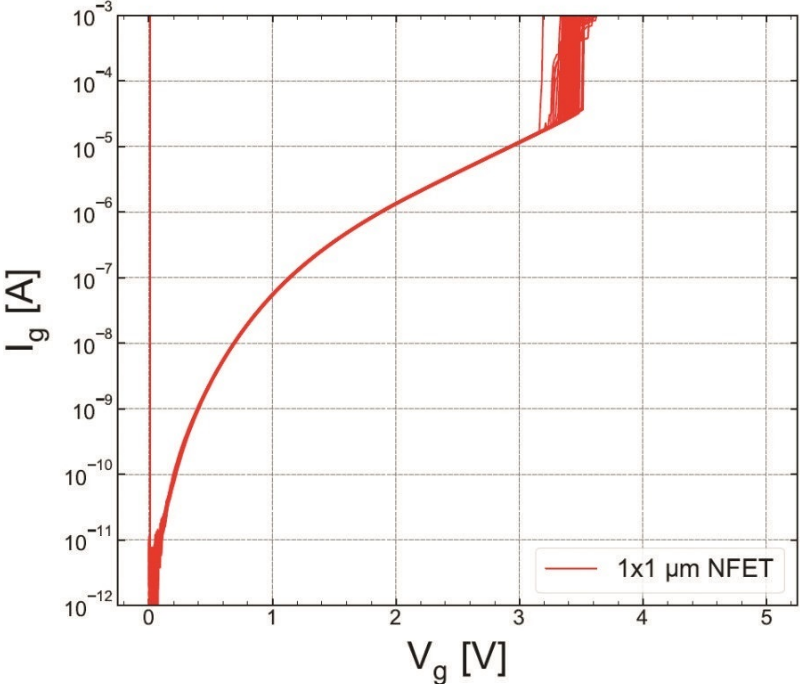

Figure 16. The same as Figure 15, but for the nMOSFET which received softer nitridation with the targeted SiON thickness of 1.9 nm (sample S #2).

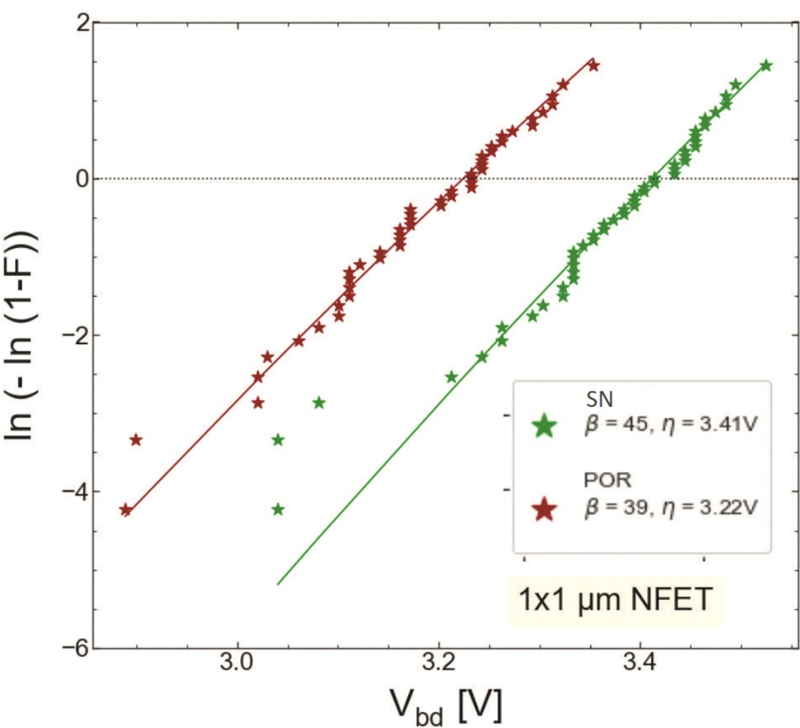

Figure 17. Weibit plots of breakdown voltages for the nMOSFETs fabricated by the POR (S #1, red symbols) and those exposed to SN (S #2, green symbols).

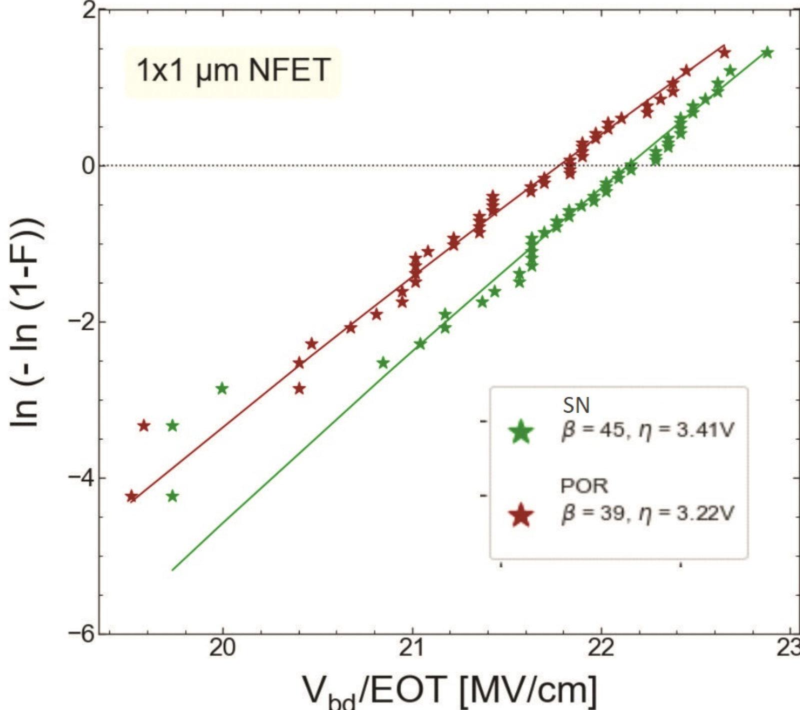

Figure 18. Weibit plots for breakdown fields extracted for nMOSFETs grown by POR and SN processes.

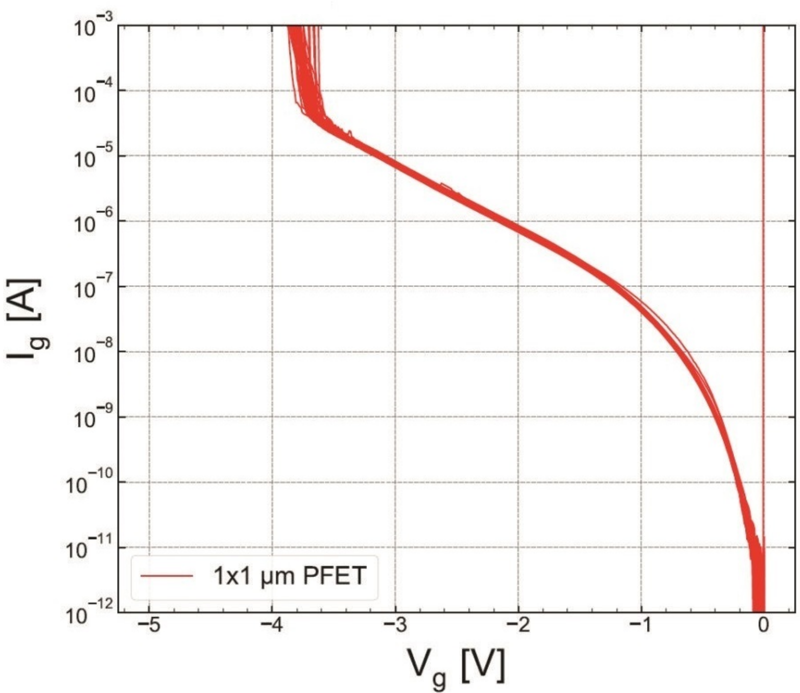

Figure 19. S #1 (POR), pMOSFETs: gate current I_g as a function of stress voltage V_g recorded during RVS HBD measurements conducted on the POR nMOSFET (sample S #1).

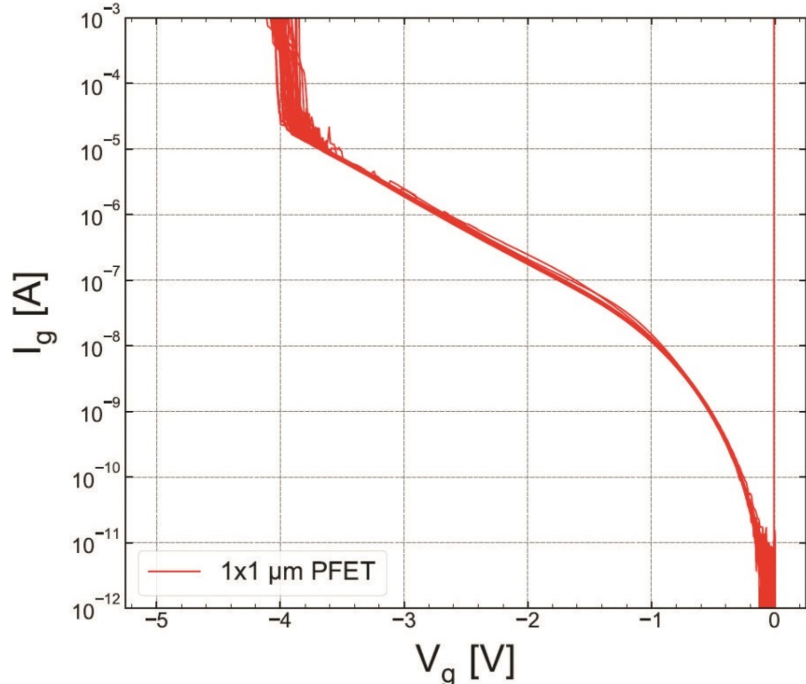

Figure 20. The same as Figure 19 but for S #2 (SN).

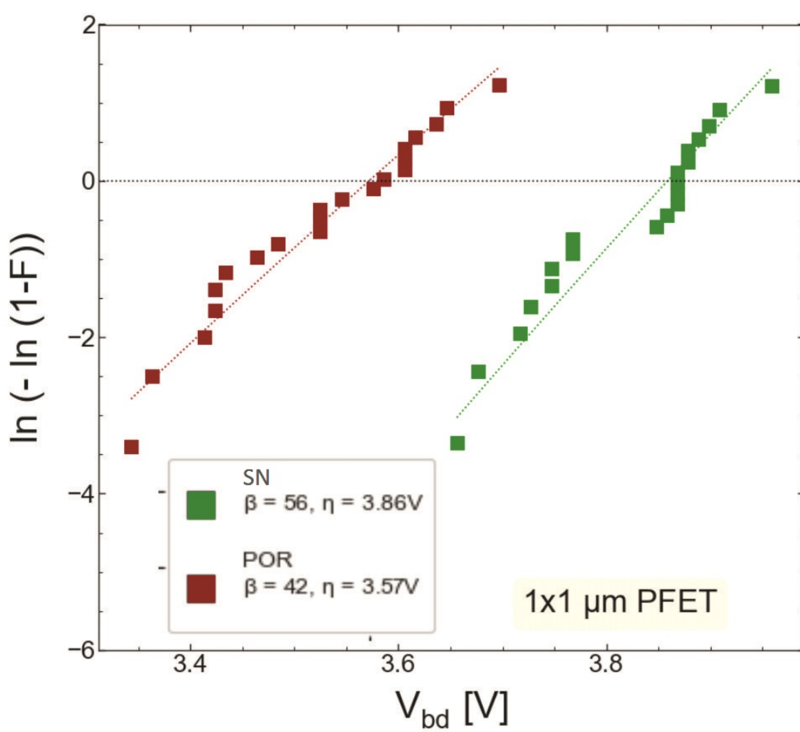

Figure 21. Weibit plots of breakdown voltages for the pMOSFETs fabricated by the POR (red symbols) and SN (green symbols).

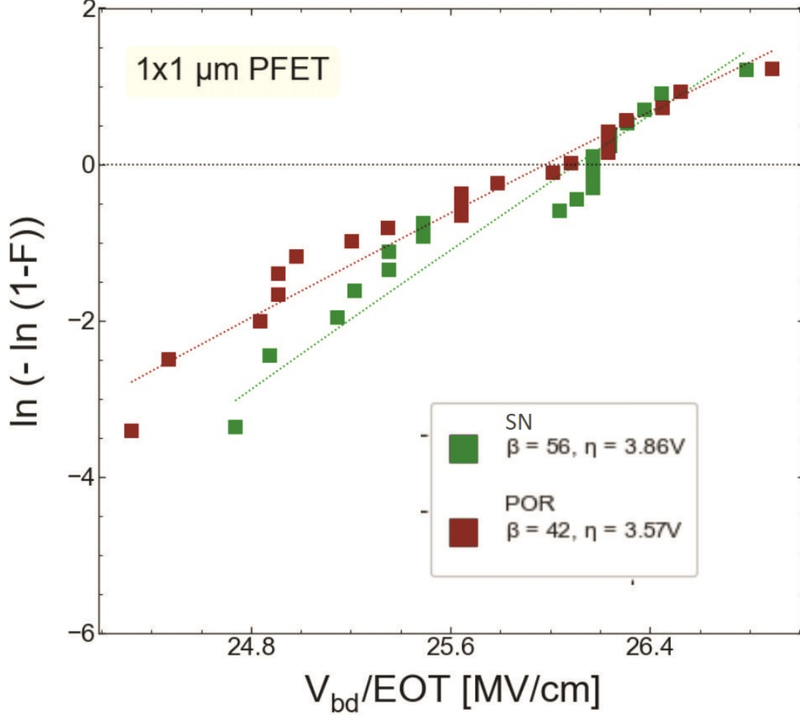

Figure 22. Weibit plots for breakdown fields extracted for pMOSFETs grown by POR and SN processes.

4.3. Interpretation of the Results

According to the current understanding of the microscopic nature of BTI in SiO_2-based transistors, traps responsible for this detrimental phenomenon are the hydrogen bridges and the hydroxyl-E′ centers [63]. These traps form two bands in the band gap of SiO_2: the band of acceptor-like states, which is situated in the upper half of the band gap, and the band of donor-like states in the lower half of the band gap [62,64]; see Figure 23. The centroid of the band of donor-like traps is situated below the Si valence band edge; therefore, the charge exchange between these traps and the valence band results in NBTI (and its recovery). On the other hand, the energetical levels of acceptor-like traps are close to the conduction band of Si, but their density-of-states is low; therefore, they provide a negligible contribution to PBTI (this behavior is consistent with experimental data reported in this work). As for traps responsible for BTI in SiON/Si_3N_4-based MOSFETs, they were identified as k_N centers with the corresponding trap density-of-states featuring a peak close to the center of the Si band gap [64–67]. As a result, they are more easily accessible for holes, thereby making the NBTI stronger in MOSFETs with SiON/Si_3N_4 layers compared to their SiO_2-based counterparts (under the same stress conditions). Therefore, an increasing N content in the SiON film leads to the "transition" from the hydrogen bridges and hydroxyl-E′ centers to k_N centers and hence more prominent NBTI. This picture is consistent with the explanation of stronger NBTI typical for SiON-based devices compared to MOSFETs with SiO_2 as the gate dielectric given by Reisinger et al. [35,68].

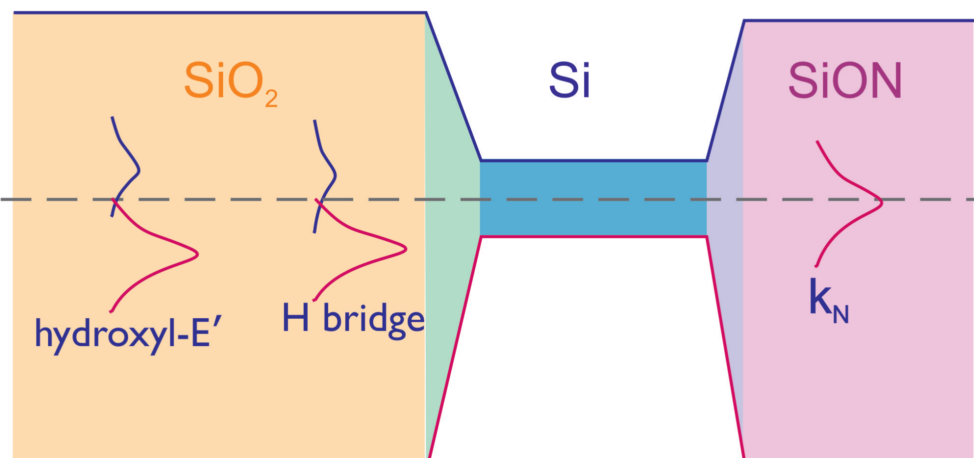

Figure 23. Schematically represented charge transition levels of traps responsible for NBTI in SiO_2-based MOSFETs—hydroxyl-E′ centers and H bridges. Both form acceptor-like states close to the edge of the Si conduction band as well as donor-like states placed below the valence band of Si. In FETs with SiON/Si_3N_4 layers, another type of defects, namely k_N centers, govern BTI. They form the defect band with a centroid close to the mid-gap of Si.

As for HBD, this event is a terminal stage of TDDB when a local concentration of generated defects is so high that these defects form a percolation path (with ohmic conductivity) [12,50]. Recent studies suggested that the microscopic mechanism underlying defect creation during TDDB/HBD is generation of O vacancies driven by the double trapping of electrons at wide angle O-Si-O sites (defect precursors) [69,70]. Although we are not aware of any papers studying the structure of TDDB-related defects and their precursors at a varying concentration of N in SiON, we can speculate that, at a higher N concentration, the energetical position of defect precursors becomes more favorable for phonon-assisted tunneling, thereby giving rise to defect creation and thus HBD at lower fields/voltages.

5. Conclusions

We compared bias temperature instability and hard breakdown characteristics of planar transistors with SiON layers with different nitrogen content. To accomplish this task, we attracted MOSFETs fabricated using processes with 1000 W (POR) and 900 W (SN) powers of radio frequency plasma nitridation; consequently, corresponding SiON films were exposed to different doses of N. In addition to this, we also used samples which—although fabricated by the same process flow—have different targeted thicknesses of SiON layers, thereby leading to different values of the N content. Nitrogen incorporated in gate oxides is known to result in positive charges distributed throughout the dielectric layer; these charges result in a threshold voltage shift towards lower V_t values. The threshold voltages values of pristine devices are consistent with the N content estimated based on the process flow details.

All MOSFETs were subjected to ramped voltage stress to study the BTI and HBD behavior of these transistors. In case of BTI, p-channel MOSFETs were stressed in the NBTI regime and nMOSFETs were subjected to PBTI. Regarding HBD, stress measurements applied to n- and p-channel MOSFETs were carried out at positive and negative gate voltages, respectively.

NBTI data demonstrated a pronounced trend—NBTI reliability is correlated with the N concentration of SiON layers, i.e., devices with a lower N content demonstrated a superior NBTI behavior (smaller ΔV_t shifts and longer TTF values). PBTI appeared to be negligibly weak in both devices with low and high N content. In the case of HBD, we compared MOSFETs with the same targeted thickness of SiON layers but fabricated using POR and SN processes. The latter samples have a lower N concentration; their Weibull distribution of the breakdown electric field is shifted towards higher values with respect to that obtained for MOSFETs with a high N content. Therefore, similar to BTI, transistors with a smaller N concentration feature a superior HBD behavior.

The aggravation of BTI in MOSFETs with a higher N concentration can be explained within the paradigm that in SiO_2-based (or SiON with a low N dose) transistors, traps responsible for BTI are the hydrogen bridges and hydroxyl-E′ centers, while in transistors with $SiON/Si_3N_4$ as the gate dielectric, BTI originates from k_N centers, which have different energy positions and therefore are more accessible by carriers. Regarding HBD, this event corresponds to such a high concentration of traps, that they form a percolation path and the dielectric film loses its insulating properties. The physical mechanism underlying the defect creation is related to double electron trapping at a wide angle O-Si-O bond, and we expect that at a higher N concentration, energetical positions of these precursor sites are shifted towards values more favorable for tunneling.

It is worth emphasizing that there is no consensus in literature regarding the impact of nitridation on BTI behavior; therefore, our result is consistent with findings of those groups who reported aggravation of BTI in strongly nitrided SiON films. Regarding the influence of nitridation on HBD, there are the very limited number of papers dealing with this topic; our contribution additionally confirms that HBD occurs at lower electric fields in devices with a higher N content.

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Abbreviations

The following abbreviations are used in this manuscript:

BTI	Bias temperature Instability
CVS	Constant Voltage Stress
eMSM	extended Measure–Stress–Measure (technique)
EOL	Equivalent Oxide Thickness
HBD	Hard Breakdown
HCD	Hot-Carrier Degradation
MOSFET	Metal–Oxide–Semiconductor Field Effect Transistor
NBTI	Negative Bias Temperature Instability
PBTI	Positive Bias Temperature Instability
POR	Process of Reference
RF	Radio Frequency
RVS	Ramped Voltage Stress
SN	Soft Nitridation
TDDB	Time-Dependent Dielectric Breakdown

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