Modeling Analysis of BTI-driven degradation of a Ring Oscillator Designed in a 28-nm CMOS Technology

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***Abstract*—With tightening reliability margins, product-level aging analysis is gradually gaining impetus and is set to become an integral part of the modern design flow. Increased emphasis is placed on the development of physics-based compact models for the phenomena responsible for transistor degradation and their integration into EDA environments. Commercial Process Design Kits (PDKs) of advanced technologies have also started to include compact models for transistor degradation along with a dedicated reliability simulation framework. In this work, we present a comprehensive study of the compact aging models in one such commercial PDK, with the help of extensive measurement data from individual devices as well as Ring Oscillators (RO). Then, we perform our own extraction of model parameter shifts from full I_d-V_{gs} fitting of the measured BTI-stressed devices to gain insight into the modeling procedure adopted by the foundry. We finally use the parameters extracted thusly to investigate the impact of the time-0 and the time-dependent device-to-device variability on RO degradation.**

***Index Terms*—BTI, HCI, Circuit Simulations, Compact modeling**

I. Introduction

Tighter reliability margins in advanced technologies have created an increased demand for circuit aging simulation capabilities so that potential reliability pitfalls can be identified at the design stage. The deviation in the performance of a circuit over time is a result of a drift in key performance parameters like threshold voltage (V_{th}), transconductance (g_m), subthreshold slope (SS), etc. of its constituent devices. Physical mechanisms like Bias Temperature Instability (BTI), Hot Carrier Injection (HCI), Self Heating Effects (SHE), etc. are responsible for this parametric drift at the device level. Consequently, foundries have started to provide aging models for prominent degradation mechanisms with the Process Design Kits (PDKs) of their modern technologies. Typically, observable quantities like the threshold voltage shift (ΔV_{th}), the drain current degradation in the linear regime (ΔI_{dlin}) and the drain current degradation in the saturation regime (ΔI_{dsat}) are modeled as a shift in core compact model parameters, like e.g. for the Berkeley Short channel IGFET Model (BSIM), the threshold voltage parameter, $vth0$, and the low-field mobility parameter, $u0$ [1], [2].

Real-life workloads experienced by a circuit can be complex and can cause multiple parameters of the constituent devices to shift simultaneously. Even for Negative Bias Temperature Instability (NBTI), it is well known that there is a degradation in mobility along with a threshold voltage shift [3], [4]. This potentially limits the scope of the compact models that mainly focus on modeling the ΔV_{th} due to BTI [5]–[7]. Hence, emphasis is laid on the accurate reproduction of the full I-V characteristics of an aged device by the reliability compact models [8].

Attempts towards simultaneous modeling of the threshold voltage shift and the mobility degradation have been made before [9], [10], but the models have not been validated at the circuit level using measurement data from real circuits. Since a device in a real circuit may experience degradation due to several overlapping mechanisms, isolating a single mechanism and verifying its model at the circuit level can be challenging.

The main aim of this work is to derive insights into the similarities and differences in the device-level and the circuit-level degradation, primarily under BTI stress conditions. In other words, we investigate how well the device-level parameter shifts reproduce the circuit-level parameter shifts. To this end, we designed specific test chips. For the device-level analysis, we designed dedicated device arrays while for the circuit-level analysis, inverter-based Ring Oscillator (RO) arrays were designed. The inverter-based RO topology is mainly chosen because, as will be explained in Section II-B, with just a simple modification, it is possible to ensure that the RO degrades predominantly due to BTI. Thus, the underlying idea is not to have an exhaustive coverage of stress profiles representing diverse circuits, rather it is to sufficiently decouple the BTI-induced degradation component at the circuit level. Additionally, with the help of the so-called *differential degradation maps*, we provide a clear picture of the areas in which the models could potentially be improved. Hence, this work is also intended as feedback to the reliability compact model developers. The logical flow of this work is depicted schematically in Fig. 1.

This paper is organized as follows : Section II provides information on the experimental setup for the device- and the circuit-level reliability characterization. Section III describes the aging simulation setup in the PDK and presents the device-

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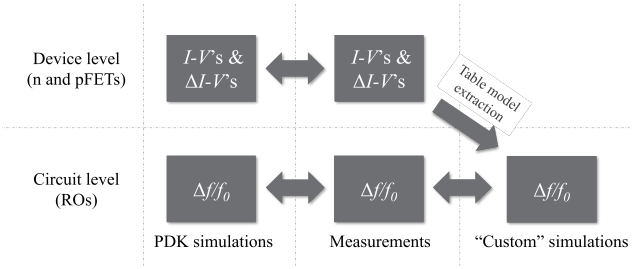

Fig. 1. The schematic describes the analysis strategy we adopt in this work. Double arrows symbolize data comparison between the two respective blocks.

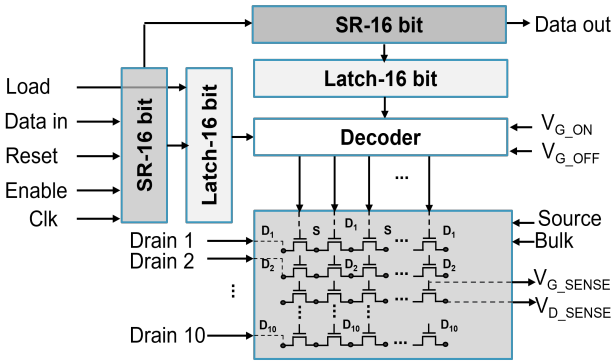

Fig. 2. Schematic of the device array used for statistical reliability characterization of devices [11]. For simplicity, the external unused peripheral blocks are not included in the diagram.

and the circuit-level simulation data. Section IV elucidates the approach adopted for the extraction of degradation parameters for each device by fitting the complete I-V characteristics. A detailed discussion of our results follows in Section V. Finally, our conclusions are summarized in Section VI.

II. Measurements

Application of over-voltage stress is one of the most common methods employed to accelerate the aging of a Device Under Test (DUT) in a laboratory environment. In this section, we describe our experimental setup for exerting electrical stress on our test chips using the voltage acceleration method.

A. Device-level characterization

Arrays of devices, similar to [11], were designed in a commercial 28-nm bulk CMOS technology, containing 2500 pFETs and nFETs. As shown in Fig. 2, individual transistors can be accessed using pass-gates (controlled by the peripheral circuitry) connected to the gates of the transistors, and by selecting the corresponding drain lines, directly routed to the bondpads. Due to this, we typically measure a higher leakage current originating from the non-selected devices sharing the same source and drain lines. However, since the degraded characteristics of each device are compared relatively to its nominal performance, this higher off-state leakage does not significantly affect our analysis. Further information about the design of the array and the peripheral circuitry can be found in [11].

The pFETs and the nFETs integrated in the array are core devices of identical gate lengths of 28 nm (drawn 30 nm) and widths of 90 nm (drawn 100 nm). The devices were measured under a wide range of stress conditions. Each stress condition is represented by the coordinate pair $\{V_{gs}$,$V_{ds}\}$, which is the DC V_{gs} and V_{ds} combination at which the stress is applied. At each $\{V_{gs}$,$V_{ds}\}$, 50 devices were measured using the Measure-Stress-Measure (MSM) method [12] (see Fig. 3) for stress times of 1, 3, 10, 30 and 100 s and a temperature of 25 °C. Full I_d-V_{gs} characteristics in the linear regime were measured at V_{ds} = 50 mV pre- and post-stress. The threshold voltage (V_{th}) was extracted using the constant current method, and the drain current in the linear regime (I_{dlin}) was extracted at V_{gs} = V_{dd} = 0.9 V.

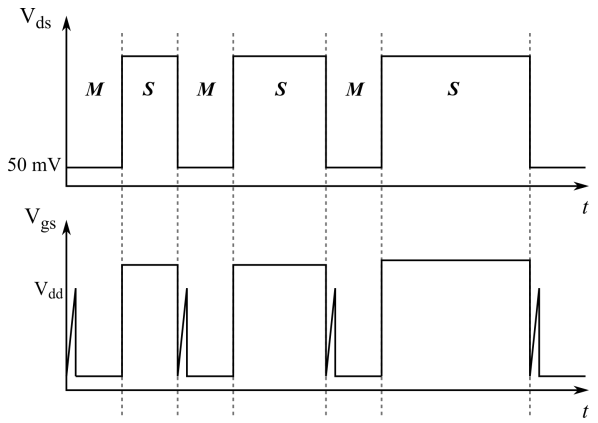

Fig. 3. Schematic of the MSM method used for reliability measurements.

B. Circuit-level characterization

An array of 51-stage Ring Oscillators (ROs) was designed and fabricated in the same commercial 28-nm technology [13], using the same core devices as the ones in the device array, but with slightly different (drawn) gate length of 35 nm. This is because the ROs were designed using standard cells which use 35 nm drawn gate lengths. Some simulations done at our end show that the difference in the gate lengths at the device and the circuit level is small enough not to significantly impact our analysis. The over-voltage stress was applied to the ROs by increasing the V_{dd} beyond the nominal value. The frequency of the designed RO (f_0) was about 2 GHz and the relative shift in the frequency ($\Delta f/f_0$) with aging was measured. A 15-stage frequency divider module was added to the output of the RO to reduce the output frequency to the kHz range. This eliminates the necessity of a Radio Frequency (RF) setup to measure the chip. To prevent the stressing of the frequency divider module, a thick-oxide inverter buffer was added in between the RO and the frequency divider, and separate V_{dd} rails were used to supply power to the RO and the frequency divider.

In the design of the RO, one of the inverter stages was replaced by a NAND gate, which has an enable input, as shown in Fig. 4. The oscillations of the RO can be turned

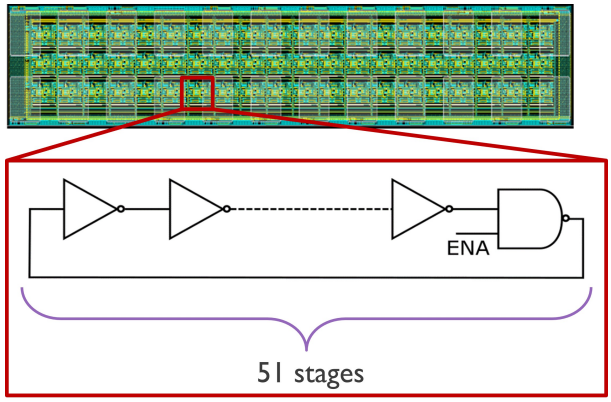

Fig. 4. The layout of the RO chip and the schematic of the RO modules are shown here. Each unit cell also contains a thick-oxide inverter buffer, frequency divider and some selector circuitry which are not shown here for simplicity. Details about the construction of the RO array are explained in detail in [13].

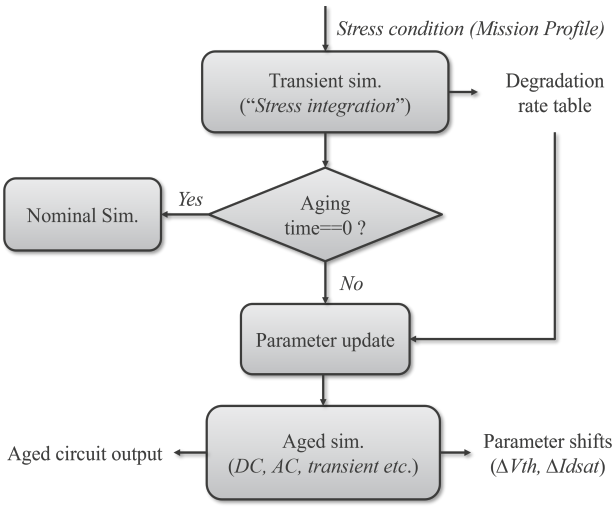

Fig. 5. Reliability simulation flow in the PDK provided by the foundry.

on or off using this enable signal (ENA). Thus, the RO can be stressed in two modes : (i) when the oscillations are enabled (dynamic stress mode), and (ii) when the oscillations are disabled (static stress mode). The frequency shift of the RO was measured under both the stress modes under a range of stress voltages from 1.4 V to 2.4 V and for stress times ranging from 60 ms to 3000 s, using the extended Measure-Stress-Measure (eMSM) methodology [14] at 25°C. After each stress condition, the RO frequency was continuously monitored for 100 s, with a measurement delay of no more than 100 μs. Detailed frequency recovery traces are presented in a previous work [13].

III. PDK MODEL SIMULATIONS

The PDK for the 28-nm technology used provides commercial aging models integrated into a native reliability simulation framework. The circuit aging simulation flow of the PDK is depicted schematically in Fig. 5. It is similar to the standard simulation flow that is implemented in other commercial reliability tools like RelXpert [15] and MOSRA [16], and consists of two steps : (i) a stress simulation, and (ii) an aged simulation.

A workload (mission profile) representative of the real-life operating conditions of the circuit is provided as the input transient to the circuit during the stress simulation. The so-called "stress integration" process takes place, where internally the aging models calculate the accumulated stress on each device in the circuit during the transient simulation time. Next, an aged simulation is run, which is aimed at simulating the performance of the degraded circuit. To this end, the accumulated stress from the stress simulation is then extrapolated to the desired operation time and transformed into a shifts in the core model parameters, that adequately emulate the characteristics of the degraded device for the aged simulations.

To the best of our knowledge, information regarding the physical foundation of the commercial aging models has not been published in the PDK documentation. Additionally, the PDK models are programmed with pre-calibrated internal parameters, which the designer does not have access to. There are some empirical parameters that can be changed to scale the calculated degradation of a performance parameter by a certain value. These scaling parameters can be used to account for the BTI recovery phenomenon, which is not inherently included in the model. But these empirical parameters have limited physical meaning, so in the context of this work we avoid their usage.

A. Device-level simulations

The transfer characteristics of the degraded devices were simulated using the 28-nm PDK reliability flow (Fig. 5). DC stress transients were applied at different V_{gs} and V_{ds} combinations, each ranging from 0 V to 2 V for stress times of 1, 3, 10, 30 and 100 s. Using the same extraction method as for the measurements, ΔV_{th} and ΔI_{dlin} were extracted from the simulations. The median values of the degraded parameters extracted from the measurements at a particular stress condition were subtracted from the values obtained from the simulations at the same stress condition, and plotted in the $\{V_{ds}$,$V_{gs}\}$ space for a given stress time. These plots, called *differential degradation maps*, shown in Figs. 6 and 8 for the nFETs and Figs. 7 and 9 for the pFETs. The maps are an efficient visualization tool for device-level reliability assessment as they allow the simultaneous investigation of different degradation mechanisms occurring in different operation regimes [17]. The underlying idea is that the model simulations should agree well with the measurements across the entire differential degradation map, including its time evolution. If this is true, then any arbitrary stress profile that may exist in a circuit can be covered by the models.

The mechanisms that predominantly cause device degradation at different $\{V_{gs}$,$V_{ds}\}$ conditions, are also indicated in Figs. 6 and 7 for the nFETs and pFETs respectively. In the bottom right corner, BTI is dominant, whereas in the top right corner, HCI is dominant [18]. With pFETs there is additionally an impact of Off-State Stress (OSS) in the top left corner,

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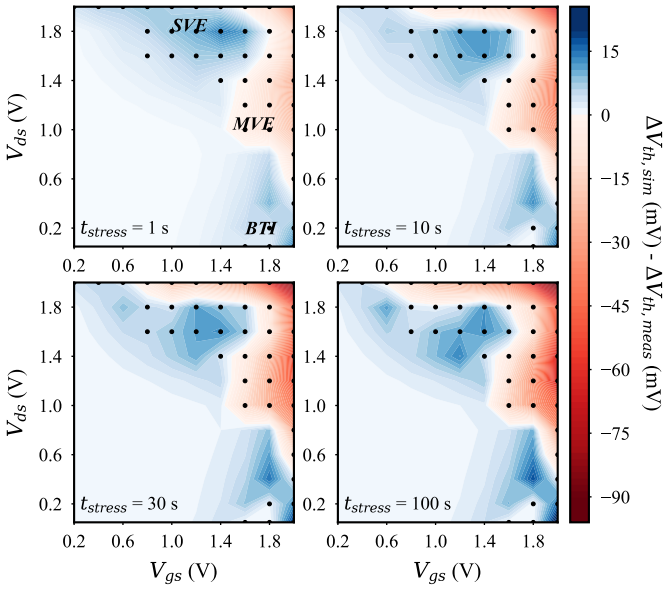


Fig. 6. The difference between ΔV_{th} extracted from nFET simulations and measurements at different stress conditions plotted in the $\{V_{gs}$,$V_{ds}\}$ space for different stress times. 50 devices were measured at each stress condition for different stress times and the median value of ΔV_{th} extracted from those 50 devices was used. Markers represent data points and the rest are interpolated values.

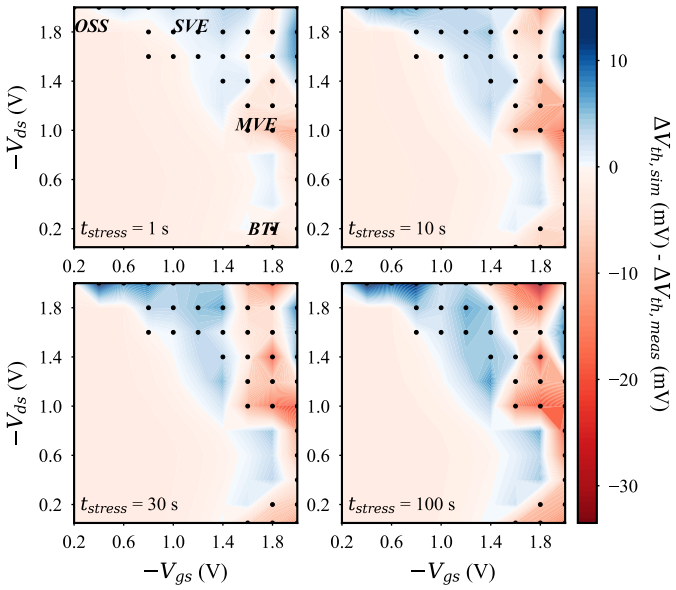


Fig. 7. Differential degradation maps for the pFET ΔV_{th} for different stress times.

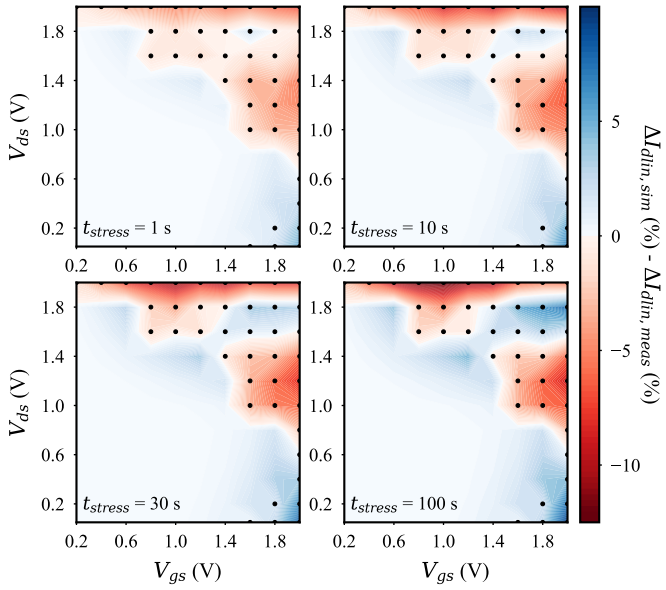


Fig. 8. Differential degradation maps for the nFET ΔI_{dlin} for different stress times.

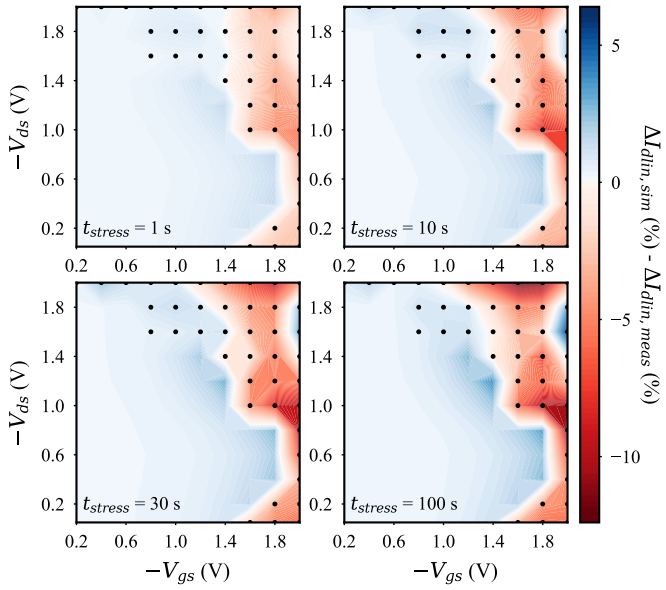


Fig. 9. Differential degradation maps for the pFET ΔI_{dlin} for different stress times.

as shown in Fig. 7, which is caused by the trapping of hot electrons in the gate oxide defects [19]. Single Vibrational Excitation (SVE) and Multiple Vibrational Excitation (MVE) are the two modes of the HCI mechanism. In the SVE mode, individual carriers have sufficient energy to excite an electron to the antibonding orbital in the Si-H bond, whereas in the MVE mode, electron bond excitation takes place due to the impact of multiple carriers [20]. A strict demarcation between the operating conditions of the SVE and MVE modes is difficult. However, as shown in Fig. 6, the MVE mode can be said to be dominant at high V_{gs} and moderate to high V_{ds}, whereas the SVE mode can be considered to be dominant at high V_{ds} and moderate to high V_{gs}.

Observing the maps in Figs. 6 to 9, we find that as the stress time increases, the agreement between the measurements and the PDK model simulations gets worse for both the nFETs and the pFETs. If this trend holds for longer times, it may

lead to an inaccurate long-term projection of circuit aging. Comparison of the BTI-dominated region for the nFET ΔV_{th} and ΔI_{dlin}, in Figs. 6 and 8, respectively suggests that for the ΔV_{th} parameter, there is a good agreement between the measurements and the simulations, while the ΔI_{dlin} parameter is significantly overestimated by the PDK models. A similar comparison for the pFET ΔV_{th} and ΔI_{dlin} in Figs. 7 and 9, respectively, suggests that both parameters are underestimated by the PDK models.

Assessment of the PDK models in other regions of the degradation space has been presented in great detail in [21], [22]. It should be noted that we have conducted the assessment under high stress conditions (1.5× - 2× V_{dd}); the stress conditions at which the foundry qualifies the models may be different.

B. Circuit-level simulations

Circuit-level RO simulations were conducted using the same PDK reliability flow (Fig. 5) by creating netlists that emulate both the static and the dynamic stress conditions. The frequency divider module and the intermediate buffer were not included in the schematic, because, as mentioned earlier, they share a different supply voltage line and therefore do not get stressed in the measurements.

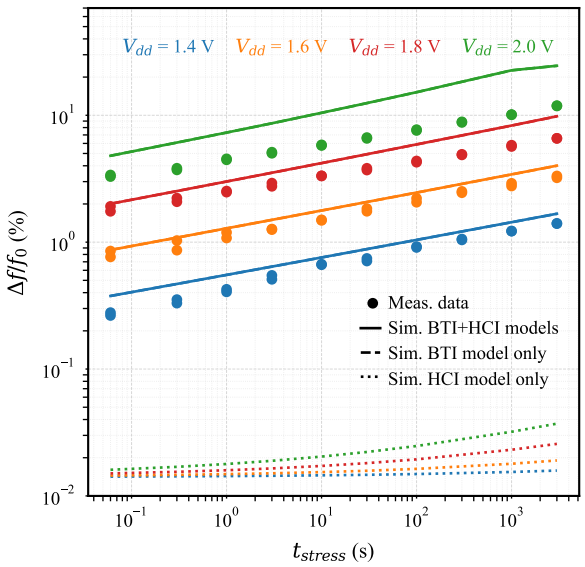
Under static stress, the voltage levels at the input of each alternating inverter stage are fixed at either 0 or V_{dd}. Hence, either the pFET or the nFET of each inverter stage experiences a high V_{gs} while its V_{ds} is effectively 0, which implies that the device is under BTI stress. Thus, the degradation of the RO under static stress is mainly driven by the BTI mechanism. On the other hand, under dynamic stress, HCI can also be expected to contribute to the RO degradation because there is current flowing through the inverter stages during the switching phases. We describe this point in detail in [21].

Fig. 10 compares the PDK model simulations of the RO with the measurements under different stress voltages. The simulation data from the BTI model only and BTI+HCI models almost coincide in Fig. 10(a), thus confirming that the RO degradation under static stress is indeed dominated by BTI.

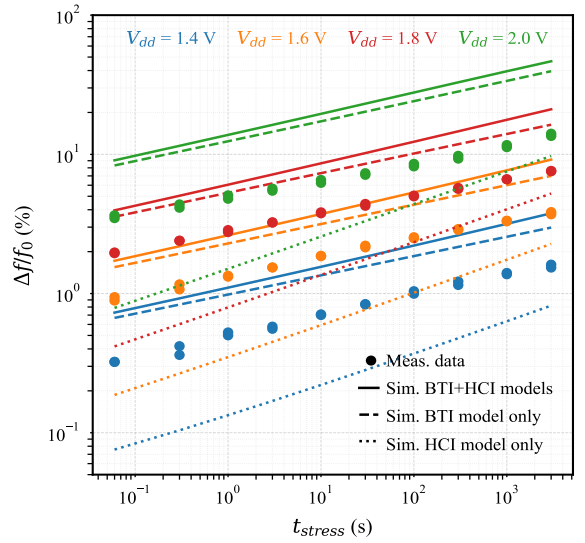
As expected, the simulations show a relatively larger contribution of HCI to the overall degradation under dynamic stress in Fig. 10(b), but BTI is still observed to be having a dominant share. The HCI contribution, however, tends to increase and compete with that of BTI as the RO is stressed for a longer period of time.

From a modeling perspective, we observe from Fig. 10(a) that under static stress, the PDK models agree well with the measurements for $V_{dd} \leq 1.8$ V. At $V_{dd} > 1.8$ V, an overestimation is observed. This trend is consistent with the trend observed for individual devices in the BTI region in Figs. 6 and 8. Previously, we had reported a constant overestimation of the RO static stress degradation by the models, also at $V_{dd} \leq 1.8$ V [21], which we have later identified as a simulation artefact [22].

For the dynamic stress mode (Fig. 10(b)), we observe that the simulations overestimate the RO degradation. One of the



(a)



(b)

Fig. 10. (a) Relative frequency shift of the RO under static stress. The simulations agree well with the measurements for $V_{dd} \leq 1.8$ V. The data from BTI only model simulations are not visible because they are overlapping with BTI+HCD model simulations. (b) Relative frequency shift of the RO under dynamic stress. Simulations can be observed to overestimate the RO degradation.

likely causes of this is the BTI recovery effect. It is well known that a BTI stressed device shows partial recovery once the stress is removed [12]. Under dynamic stress, except for the time spent in toggling, each transistor is BTI stressed for only half the time. For the other half, there is a possibility to recover. Since the PDK BTI model does not include the recovery effect, a pessimistic reliability projection is delivered.

Furthermore, the dependence of the RO frequency shift on the stress time for our measurement window can be modeled using a simple power law :

$$\Delta f/f_0 \propto {t_{stress}}^{\beta_{acc}} \quad (1)$$

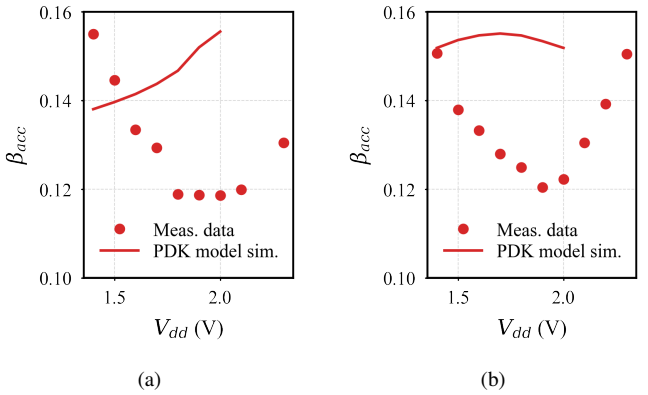


Fig. 11. Stress time acceleration factors extracted from the RO measurements and simulations under (a) static stress, and (b) dynamic stress.

where, β_{acc} is the stress time acceleration factor.

The β_{acc} extracted using the power law under different stress V_{dd} values are shown in Fig. 11. Under the static stress mode in Fig. 11(a), β_{acc} obtained from the measurements are observed to decrease at first with the stress V_{dd}. This is consistent with a gradual saturation of the BTI time acceleration factor at higher gate overdrive voltages, as has been reported previously [23]. However, a slight increase in β_{acc} is observed for V_{dd} greater than 2 V. This could be due to an increased impact of the generation of traps in the bulk of the oxide [24].

A similar qualitative observation can be made for the dynamic stress mode in Fig. 11(b). In this case, however, the increase in β_{acc} is more prominent and occurs already at $V_{dd} \geq 1.8$ V. Under dynamic stress, the oscillation frequency increases as the V_{dd} is increased, leading to a larger number of switching transitions for the same stress time. More importantly, increasing the stress V_{dd} pushes the transient operating points of the transistors towards the high $\{V_{gs}$,$V_{ds}\}$ domain (top right corner in our maps), where degradation due to HCI gets more aggressive. Due to higher contribution of HCI at these high V_{dd} stress conditions, we observe an increase in β_{acc}.

The simulations predict a trend of marginal increase in β_{acc} with increasing stress voltage, which is contrary to what is measured. The time acceleration factors are crucial to determining the long-term circuit performance and inaccurate estimation thereof may lead to significant errors in the predicted lifetime of the circuit.

IV. Parameter Extraction by Full I_d-V_{gs} Fitting

The shift in the device parameters due to aging is fundamentally understood as originating from the interaction of the mobile channel charge with the defects (traps) in the gate stack of a device [25]–[27]. The defects can capture or emit mobile charges from the channel. Additionally, a charged defect can electrostatically interact with mobile channel charges. The former is generally associated with the threshold voltage shift of the device, while the latter is associated with the mobility degradation in the device [28]. This mobility degradation is primarily driven by Coulomb scattering, so the location of

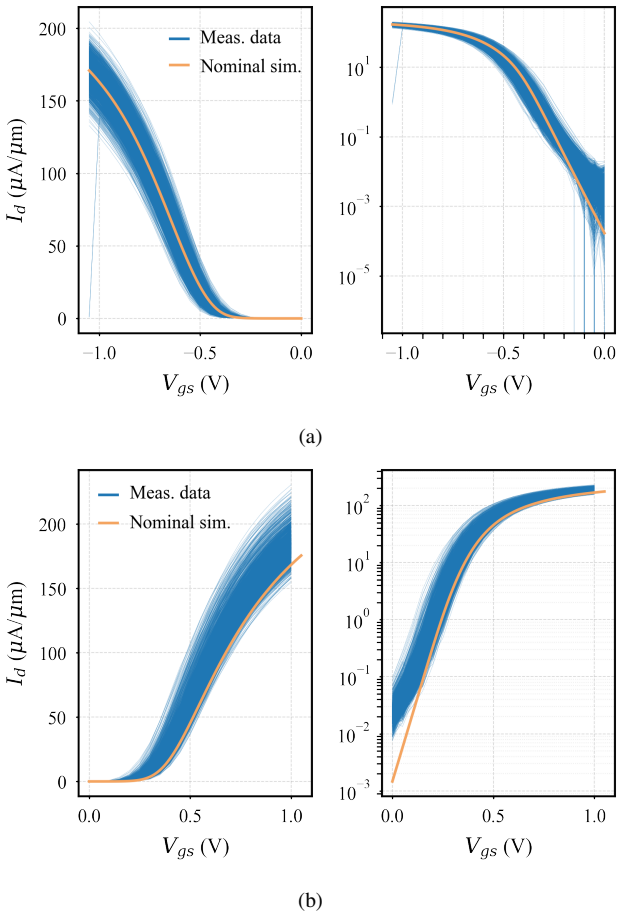


Fig. 12. I_d-V_{gs} characteristics measured from about 2500 fresh (a) pFETs, and (b) nFETs compared to the respective nominal simulations of the core model (BSIM).

the traps in the depth of the oxide bulk with respect to the channel plays a very important role in determining its impact on the overall degradation profile of a device. Additionally, given the nature of the mobile charge and the oxide electric field, new traps may also be generated by highly energetic carriers interacting with defect precursors.

For a given device, the trapping/de-trapping and the charge scattering events are caused by the same traps, which makes the two mechanisms highly correlated. It is difficult to decouple them and gain physical insights by using macroscopic observables like ΔV_{th} and ΔI_{dlin}, because one influences the other. A better approach would be to perform the fitting of the complete I_d-V_{gs} characteristics using the core device model and to extract the threshold voltage- and mobility-specific model parameters for the degraded devices. This approach ensures a better physical understanding of the operating mechanisms because it exploits the essential device electrostatics and charge transport physics already encompassed in the core device models.

The core device models in the PDK are BSIM-based. The BSIM model has two parameters $delvto$ and $mulu0$, which can respectively be used to shift the threshold voltage and scale the mobility of the device by a specified value [29]. Since these parameters are relative, they can be efficiently used to model

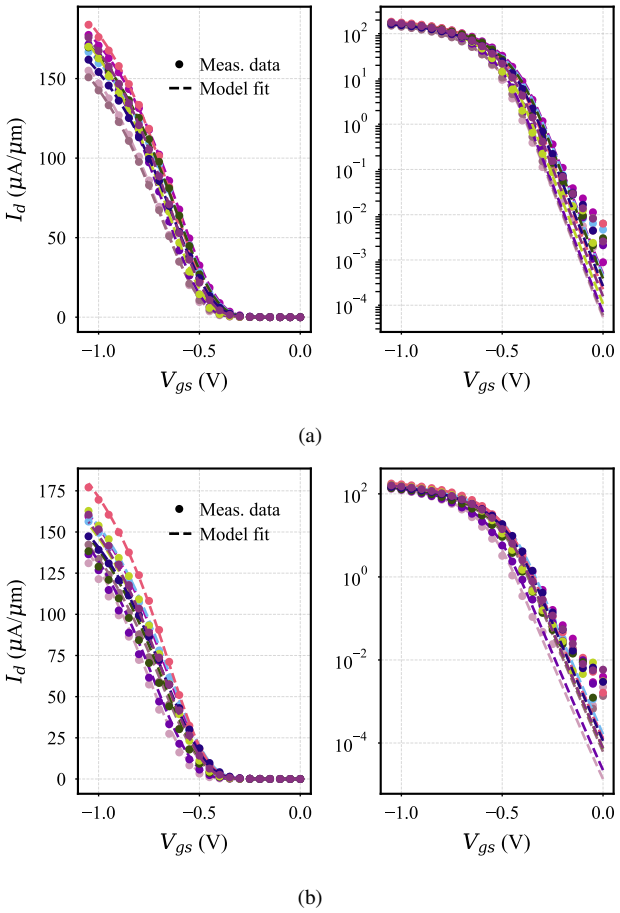


Fig. 13. I_d-V_{gs} characteristics of 10 arbitrarily selected (a) fresh pFET devices, and (b) the same pFET devices after a stress at $\{V_{gs}$,$V_{ds}\}$ = {-2.0 V, 0.05 V} for 100 s. $delvto$ and $mulu0$ parameters are used to fit the core BSIM model to the measured I_d-V_{gs} characteristics. Except for the deep subthreshold region, good fits are obtained.

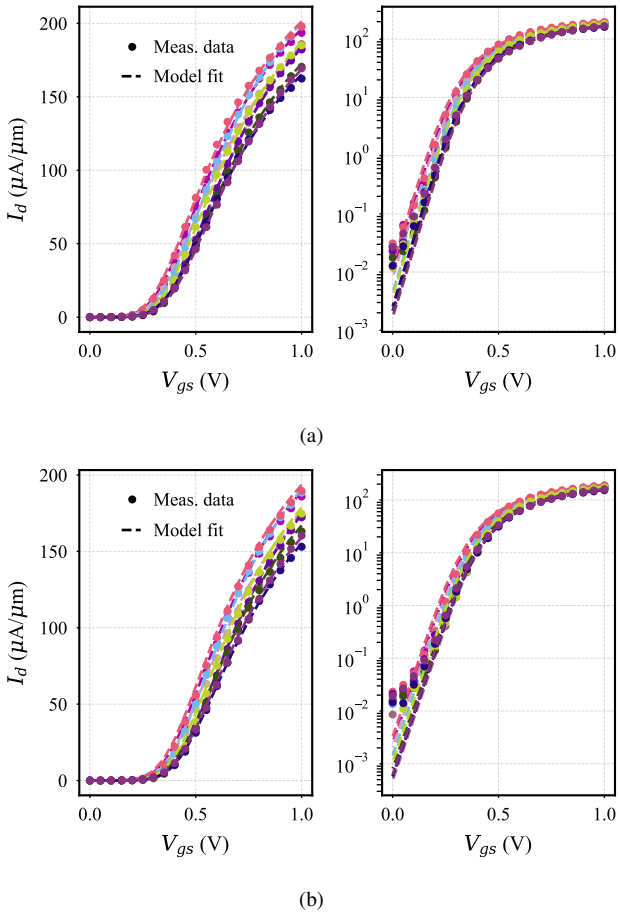


Fig. 14. I_d-V_{gs} fits of 10 arbitrarily selected (a) fresh nFET devices, and (b) the same nFET devices after a stress at $\{V_{gs}$, $V_{ds}\}$ = {2.0 V, 0.05 V} for 100 s. Except for the deep subthreshold region, good fits are obtained.

the degraded I_d-V_{gs} characteristics without the knowledge of the original values of $vth0$ and $u0$.

Firstly, we investigate the spread of the time-0 I_d-V_{gs} characteristics from the measurements with respect to the nominal simulation of the same using the core device models. A nominal core model simulation would have $delvto$ = 0 and $mulu0$ = 1, which are the default values. Fig. 12 shows that a significant time-0 variability exists among the measured devices. Hence, the fresh time-0 device characteristics also need to be fitted using the $delvto$ and $mulu0$ parameters to correctly track the shift in the performance of each device post-stress.

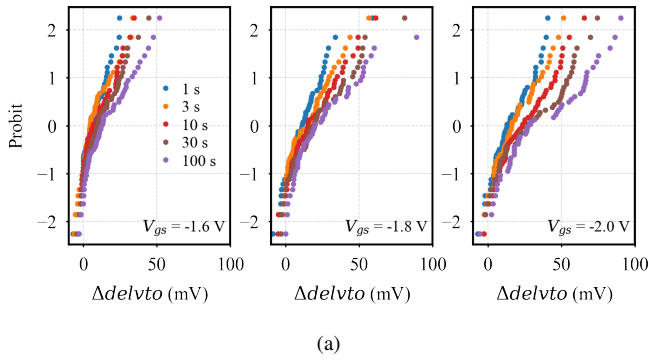
Since our primary aim here is to model the RO frequency shift under static stress, which is BTI-driven, we have restricted the fitting of our I_d-V_{gs} characteristics to the BTI-dominated region. Measurements were available at $\{|V_{gs}|,|V_{ds}|\}$ = {1.6 V, 50 mV}, {1.8 V, 50 mV} and {2 V, 50 mV} for stress times of 1, 3, 10, 30 and 100 s, as described already in Section II. All of the transfer characteristics measured from 50 devices under each of the stress conditions, including the ones from the fresh devices, were fitted.

Figs. 13 and 14 show the model fits of fresh and aged transfer characteristics from 10 arbitrarily selected pFETs and nFETs, respectively. In the deep subthreshold region, we obtain poor fits because of the leakage from non-selected devices, as already mentioned in Section II-A. For current higher than 0.1 μA/μm, we obtain excellent fits. This is actually the more relevant range because the constant current at which we extract the threshold voltage (1 μA/μm) lies in this range.

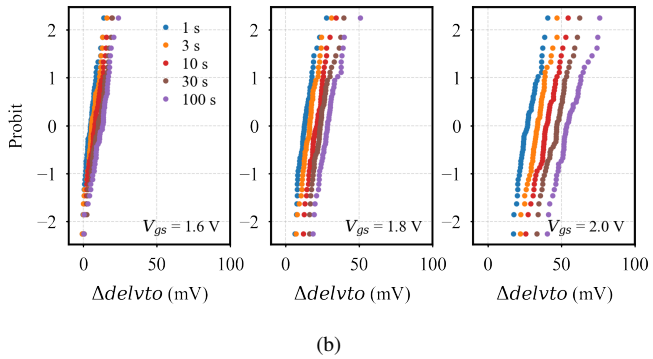
V. Discussion

In this section, we present a detailed analysis of the $delvto$ and $mulu0$ parameters extracted from our I_d-V_{gs} fits. The shifts in the $delvto$ parameters for the pFETs and the nFETs under different stress conditions are shown in the plots in Fig. 15. It can be observed that, as the stress time is increased, the variability among both the pFET and the nFET devices increases. Moreover, there is a wider dispersion of $\Delta delvto$ in the pFETs compared to the nFETs under similar stress conditions.

Fig. 16 similarly shows the shifts in $mulu0$ for the pFETs and the nFETs under different stress conditions. A steady increase in $\Delta mulu0$ is observed for the pFETs in Fig. 16(a) when the stress voltage and the stress times are increased. On the other hand, the dispersion of $\Delta mulu0$ for the nFETs

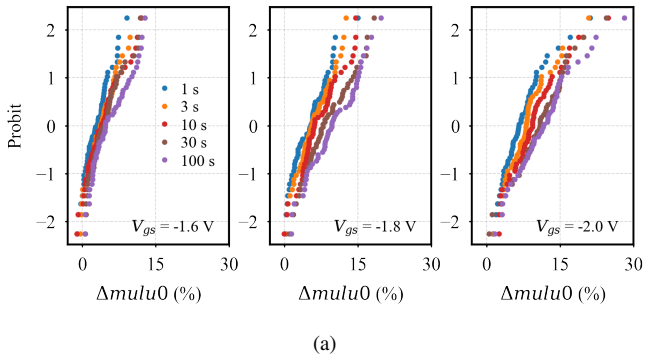


(a)

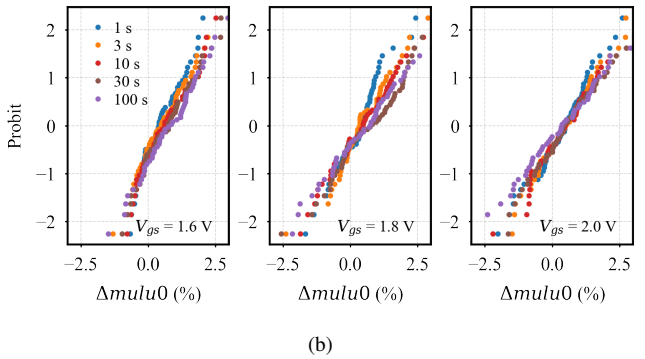


(b)

Fig. 15. Extracted $\Delta delvto$ from full I_d-V_{gs} fitting under each stress condition in the BTI-dominated region for (a) pFETs and (b) nFETs.



(a)



(b)

Fig. 16. Extracted $\Delta mulu0$ from full I_d-V_{gs} fitting at each stress condition in the BTI-dominated region for (a) pFETs and (b) nFETs.

in Fig. 16(b) remains effectively unchanged. Moreover, the absolute shifts in $mulu0$ for the nFETs are below 3%, which can be considered to be negligible relative to those for the pFETs.

This is consistent with previous studies [4], where mobility degradation was mainly observed after NBTI stress. The generation of defects at the Si/SiO_2 interface accompanies the charge trapping/de-trapping during NBTI. The interface traps and the bulk oxide traps lying close to the channel cause significant Coulomb scattering of the mobile charge carriers, which leads to a degradation in mobility. On the other hand, traps responsible for PBTI are present in the high-K layer or at the high-K/SiO_2 interface [28], which are relatively farther away from the channel to exert significant Coulomb forces on the mobile charge.

Now that we have a complete dataset of model parameter shifts at each stress condition and stress time, we can move forward with utilizing them in our RO static stress simulations. Firstly, we assume that under static stress, 25 nFETs and 26 pFETs in the 51-stage RO experience BTI stress and thus undergo a shift in performance. The remainder of the devices remain unaffected and therefore retain their nominal performance. This assumption was verified using the PDK reliability flow, which predicted a similar behaviour of the devices in the RO under static stress.

The simplest approach is to extract the *median* model parameter shifts under each stress condition for the nFETs and the pFETs, assign those shifts identically to the 25 nFETs and the 26 pFETs, respectively, and run RO transient simulations to calculate the degraded output frequency. The relative frequency shifts obtained using this approach are plotted along with the measurement data in Fig. 17. We obtain good fits even at high V_{dd} stress conditions.

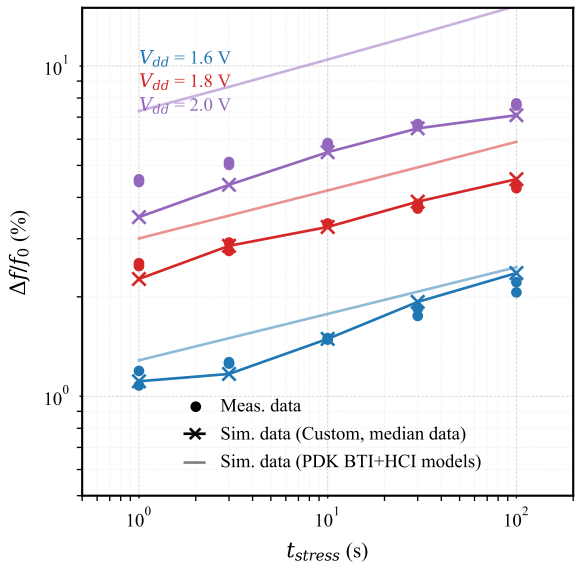


Fig. 17. Custom RO simulations using the *median* parameter shifts from Figs. 15 and 16. Good agreement with the measured data is observed.

In the above approach, we assumed that all devices in the RO are identical and do not exhibit any time-0 or time-dependent variability. To further investigate the impact of variability, we can adopt a "pseudo Monte-Carlo" approach.

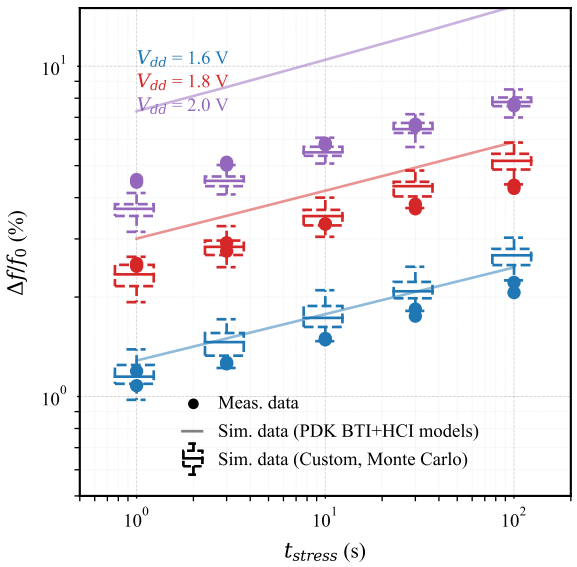


Fig. 18. Pseudo Monte-Carlo simulations performed from random sampling of parameter shifts in Figs. 15 and 16. 50 Monte-Carlo iterations were run under each V_{dd} condition.

Instead of utilizing the median parameter shifts, for a given stress condition, we can randomly sample through the parameter shifts in Figs. 15 and 16 and assign them to each degrading device in the netlist. With this approach, we can not only investigate the impact of time-dependent variability, but also time-0 variability because we have also extracted $delvto$ and $mulu0$ values from transfer characteristics of fresh devices. Indeed, in this case, there would be a statistical variation of the nominal RO frequency (f_0) and the relative frequency shift under each stress condition is determined with respect to the f_0 corresponding to the particular sample set of devices.

The results obtained from our "custom Monte-Carlo" simulations are shown in Fig. 18. We observe that, despite the devices exhibiting significant time-0 and time-dependent variability, the RO relative frequency shift does not exhibit a significant variability. This is due to two main reasons : (i) the factor $\Delta f/f_0$ intrinsically suppresses the impact of time-0 variability, and (ii) the large number of devices in the RO average out and suppress the impact of both time-0 and time-dependent variability.

VI. Conclusions

This paper has presented a consistent set of data obtained from extensive reliability measurements in a commercial 28-nm bulk planar CMOS technology, both at device and circuit level. Using differential degradation maps, a detailed assessment has been presented of the transistor aging models included in the PDK of the technology across a wide range of $\{V_{gs}$,$V_{ds}\}$ conditions at the device level. For a ring oscillator (RO) designed in the same technology, we observe that the PDK aging simulations model the degradation under static stress well. Under dynamic stress conditions, however, the PDK models overestimate the RO degradation, likely because the BTI recovery effect is not included in the models. Furthermore, with our full transistor I_d-V_{gs} fitting scheme to measurement data, we have demonstrated that the simultaneous extraction of the threshold voltage shift and the mobility degradation reproduces the RO degradation under static stress well, even under high stress conditions. It also enabled us to investigate the impact of time-0 and time-dependent device-to-device variability on the RO performance, which was found to be minimal.

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