Novel Low Thermal Budget CMOS RMG: Performance and Reliability Benchmark Against Conventional High Thermal Budget Gate Stack Solutions

J. Franco, *Member, IEEE*, H. Arimura, J.-F. de Marneffe, S. Brus, R. Ritzenthaler, K. Croes, B. Kaczer, and Naoto Horiguchi

***Abstract*— Low thermal budget gate stack fabrication is a key enabler for upcoming CMOS technology innovations, such as Sequential-3D integration and CFETs. In this paper, we discuss the impact on gate stack properties of the novel low temperature atomic hydrogen and oxygen treatments that we have recently demonstrated on MOS capacitors. Next we evaluate on a planar CMOS transistor platform various low thermal budget RMG gate stacks based on (combinations of) these treatments, by benchmarking them against high temperature RMG and Gate-First counterparts. This first demonstration on both *p*- and *n*-channel transistors with properly tuned gate work functions allows to benchmark electron and hole mobilities, and to assess stochastic variability (V_{th} mismatch), NBTI and PBTI reliability, and the performance (I_{ON}-I_{OFF}) and Channel Hot Carrier reliability (Safe Operating Area) of short channel nMOS. We find that the atomic hydrogen treatment, originally developed to improve pMOS NBTI reliability, substantially boosts also the nMOS device performance and reliability due to a remarkably improved interfacial layer quality, matching high-temperature counterparts and thus providing a complete solution for low thermal budget CMOS RMG at a competitive EOT's.**

***Index Terms*—Bias Temperature Instabilities, Stacked CMOS, Sequential 3D Integration, CFETs, Low Thermal Budget Gate Stack, Radical Treatments.**

I. Introduction

Low thermal budget gate stack fabrication is a key enabler for several upcoming CMOS technology innovations. In contemporary High-k Metal Gate (HKMG) Replacement Gate (RMG) flows a so-called 'reliability anneal' is performed after HK deposition to cure dielectric defects [1]. This high-temperature (T) process step (~850˚C) is not suitable for Sequential 3D integrations of stacked transistors (Fig. 1), as top device tiers need to be fabricated at reduced thermal budget [2] to preserve the functionality of the bottom tiers already in place. For monolithic CFET [3] fabrication, in a "RMG-last" flow the high-T reliability anneal can degrade the contact performance.

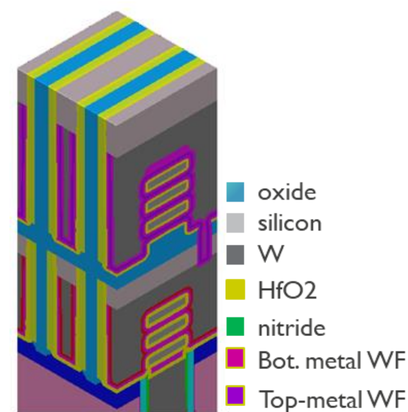

Fig. 1. Illustration (Coventor® image) of a CFET consisting of two groups of stacked nanosheets (p- and nMOS). A tight vertical pitch poses limits on the total gate thickness; either Sequential 3D or monolithic integration flows pose limits on the top tier fabrication thermal budget.

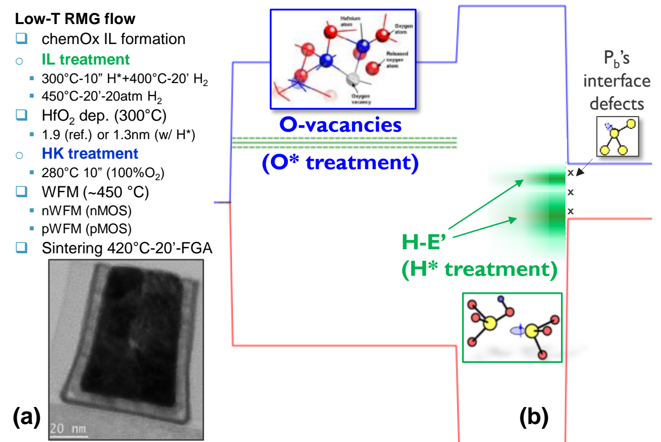

Fig. 2. (a) Schematic of the low-T RMG flow, with insertion of the novel H* and O* treatments before and after the HK deposition, respectively. The inset shows a TEM of one such fabricated gate (b) Band diagram illustrating the SiO_2 and HfO_2 defect bands (related to the hydroxyl-E' and oxygen vacancies defects, respectively) targeted by each treatment.

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Conversely, moving the RMG module to earlier in the flow ("RMG-first") imposes stringent thermal stability requirements for the HKMG stacks to endure the epi and contact module thermal budgets (max T~525°C for several hours), which would be particularly challenging for the tight effective Work Function (eWF) control [4] required by multi-V_{th} technologies. Furthermore, a standard RMG "reliability anneal" requires the deposition of a (relatively thick, typ. ~7nm) sacrificial gate (TiN/a-Si), which is then replaced with the final WFM after a high-T spike anneal [1]; this integration flow, and in particular the removal of the sacrificial gate, become challenging for stacked nanosheets with tight vertical pitches (see Fig. 1). The development of novel low thermal budget RMG stacks discussed here (Fig. 2a), with simplified integration and with competitive performance and reliability as compared to state-of-the-art high thermal budget RMG, addresses these concerns.

In order to develop effective low thermal budget gate stack treatments, it is crucial to understand the microscopic nature of the electrically-active defects present in the as-deposited dielectric stack. In [5] we have shown that hydroxyl-*E'* (H-*E'*) defects [6] are abundant in SiO_2 (interfacial) layers grown at reduced T (≤600˚C) and not subsequently annealed at high T (≥700˚C); this defect structure form at stretched Si-O-Si bonds, which exist due to unrelaxed interface strain: the incorporation of an OH-group (recall hydrogen is ubiquitously available in the gate stack fabrication flow, including during the formation of the SiO_2 interfacial layer by wet chemical oxidation – chemOx – or by in-situ steam generation – ISSG) releases the strain locally, but leaves behind a Si dangling bond (see Fig. 2b). In [7] we have shown that the density of these defects peaks at the Si/SiO_2 interface, and decays exponentially across the IL depth with a characteristic depth of 0.5nm, in agreement with the interface strain profile. Ab-initio calculations predict the H-*E'*s to behave as amphoteric defects [8], with charge transition levels located below the Si conduction band (and thus potentially detrimental for nMOS mobility) and above and below the Si valence band (thus behaving either as positive "fixed" charge or as a NBTI hole trap [5], and potentially detrimental for pMOS mobility). In HfO_2 instead, oxygen vacancies (V_o) with charge transition level above the Si conduction band (see Fig. 2b) are often quoted as the primary responsible for electron trapping (and thus degraded nMOS PBTI reliability) [9]. To passivate efficiently the H-*E'*s in the SiO_2 interfacial layer (IL) and the V_o's in HfO_2 at low temperature, a remote plasma treatment was developed to provide hydrogen (H*) [5,7,10] and oxygen (O*) [11] radicals at suitable insertion points during the RMG flow, and efficiently passivate defects at low T (≤300˚C). The H* can deactivate the H-*E'* defect either by passivating its Si dangling bond, or by removing the OH- or H- present at the defect sites (releasing a H_2O or a H_2 molecule respectively), and thus transforming the defect configuration into an (electrically-inactive) oxygen vacancy [6], or back into a (stretched) Si-O-Si bond. The O* instead appears to passivate efficiently V_o's in HfO_2 at low-T.

In Section II we summarize the impact of the H* IL treatment on the electrical properties of a pMOS gate stack with a *p*-WF metal (WFM, TiN), as assessed on planar MOS capacitors. In Section III, a similar analysis is reported regarding the impact of the O* HK treatment on a nMOS gate stack with *n*-WFM (TiAl-based). In Section IV, we evaluate various low thermal budget RMG gate stacks comprising H*, H_2 and O* treatments (see Table I) on a planar CMOS transistor platform and benchmark them against high-T RMG and Gate-First HKMG counterparts. We find that, due to the induced remarkable improvement of the IL quality, the H*-H_2 treatment boosts both the pMOS and nMOS carrier mobilities and both NBTI and PBTI reliability. Furthermore, a substantial improvement of the short channel nMOS Safe Operating Area is also observed, due to a reduced non-equilibrium charge trapping in the IL during Channel Hot Carrier stress. Thanks to the simultaneous improvement of pMOS and nMOS device metrics, and to a better EOT scalability as compared to the O* HK treatment, the H*-H_2 IL treatment comes out as a complete stand-alone solution for low thermal budget CMOS gate stacks.

II. EFFECTS OF THE H* IL TREATMENT

The H* treatment is performed right after formation of the IL (see Fig. 2a) to maximize the passivation of the pre-existing SiO_2 H-*E'*. Performing the H* treatment later in the flow results in an insufficient passivation degree (not shown), likely due to

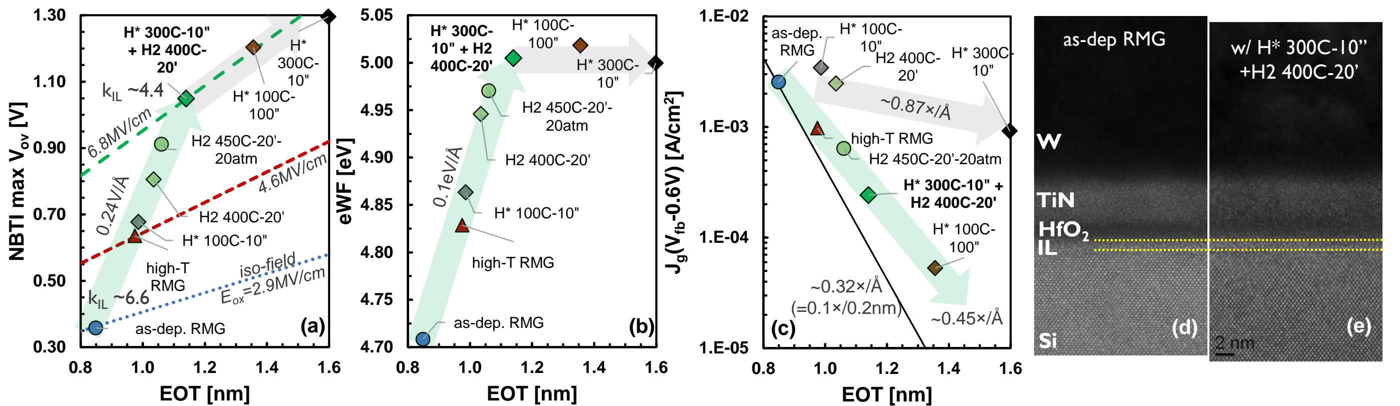

Fig. 3. (a) NBTI max. operating V_{ov} (defined as the overdrive inducing a 2.5mV shift after 1ks stress at 25°C, which projects to a ~50mV shift after 10-year at 125°C for a typ. kinetics) of low-T RMG gate stacks with different H*/H_2 IL treatments, plotted vs. EOT (note: a standard high-T RMG gate stack is also shown as ref). (b) eWF.and (c) gate leakage density at V_G=V_{fb}-0.6V plotted vs. EOT for each gate stack. (d) HR-TEM's of the as-deposited RMG gate stack, and (e) with insertion of the H*-H_2 IL treatment.

the radicals reacting at other sites in the dielectric stack volume before reaching the H-*E'* preferentially located near the channel interface. A limited concentration of hydrogen radicals can be conveniently generated in-situ without plasma processing by annealing the IL at 400-450˚C in H_2 before HKMG deposition, exploiting the native interface P_b centers (see Fig. 2b) as hydrogen molecule cracking sites [12]. In this case, the generated density of H* equals (at most) the native surface density of P_b defects, i.e., 5-7×10^{12} /cm^2, irrespective of the dielectric thickness: this simplified approach is therefore not suitable for thicker SiO_2 layers [5], or if applied after HK deposition, as the generated radicals can "get stuck" at other sites in the dielectric volume before they can reach the closest H-*E'* near the interface. This explains why standard anneals in molecular hydrogen or forming gas performed at the end of the device fabrication flow are not sufficient to passivate the H-E' and improve adequately the quality of low-T IL's [5].

Fig. 3 depicts the impact of various H* and H_2 IL treatments on the electrical properties of a pMOS gate stack, as assessed on MOS capacitors. Stronger H*/H_2 treatments (i.e., longer duration or higher T) result in larger NBTI improvement, but also in increased EOT (Fig. 3a). Notice the reliability improvement is at first much stronger than the expectation related to the reducing oxide electric field (due to the increasing EOT), confirming a genuine reduction of the dielectric trap density; eventually, for the strongest treatments, the NBTI improvement rate saturates towards an iso-electric field line. The eWF (Fig. 3b) also increases upon the H*/H_2 treatments, suggesting a reduction of the positive charge in the IL: this is readily explained by the H-E' defect band spanning above and below the Si E_v [6,8] (see Fig. 2b), and thus behaving partially as positive "fixed" charge, and partially as NBTI hole traps. The eWF change eventually saturates for longer treatments, suggesting that the number of passivatable H-*E'* defects fades out (consistent with the saturation of the NBTI improvement rate). The H*/H_2 treatments are found to also reduce the gate leakage density (Fig. 3c); the J_g reduction rate vs. EOT increase is however incompatible with an IL thickness increase (as the latter would induce a stronger J_g reduction of ~10× per 2Å); indeed High Resolution-Transmission Electron Micrographs (HR-TEM's, Figs. 3d,e) do not reveal any significant difference

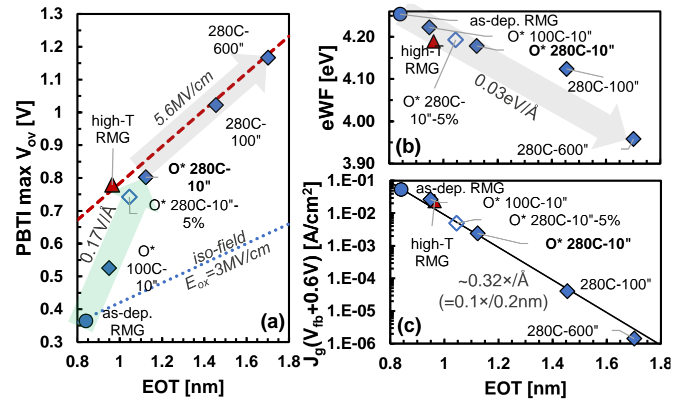

Fig. 4: (a) PBTI max. operating V_{ov} of low-T RMG gate stacks with different O* HK treatments, plotted vs. EOT (note a standard high-T RMG gate stack is also shown as ref). (b) eWF.and (c) gate leakage density at V_G=V_{fb}+0.6V plotted vs. EOT for each gate stack.

in the IL thickness w/o or w/ the H* treatment. We therefore ascribe the reduced leakage to a bandgap widening of the chemOx upon defect passivation, towards the nominal 9eV of thermal SiO_2 [10]. Similarly, the EOT increase up to ~3Å observed for moderate H*/H_2 treatments is ascribed to the lowering of the chemOx relative permittivity from ~6.6 (as-deposited, i.e., containing a large density OH group) towards ~3.9 (nominal for high quality SiO_2) upon removal of OH-groups at the defect sites, and thus should be considered as an unavoidable side effect of the H-*E'* defect deactivation. For stronger H* treatments, an EOT increase up to ~8Å is observed, without a corresponding J_g reduction (Fig. 3c): this is ascribed to suboxide formation, likely at the interface P_b sites depassivated by the excessive presence of H radicals [7]. To avoid this detrimental effect, the strongest H* treatment condition (300˚C-10") is coupled with an early H_2 sintering anneal (400˚C-20') to restore an optimal passivation of the P_b's already before HK deposition [7]. The H*-H_2 combination results in the largest NBTI and eWF improvement with a moderate EOT increase (~3Å) solely related to the IL k-value change. A H_2 IL treatment only instead minimizes the EOT penalty (~1.5Å) while still yielding a superior NBTI reliability as compared to a high-T RMG ref. These two IL treatment conditions have been selected for the transistor benchmark discussed later in Section IV.

	Gate Stack	Low-T IL treatment	HfO_2 [nm]	Low-T HK treatment	HK PDA	Reliability anneal	nMOS WFM	pMOS WFM
Low thermal budget	RMG as-dep.	-	1.9	-	-	-	TiN/TiAl/TiN (1/4/3 nm)	TiN (5nm)
	HP H_2 on IL *(thin HK)*	H_2 450°C-20'-20atm	1.3	-	-	-	-	TiN (5nm)
	H*+H_2 on IL *(thin HK)*	H* 300°C-10" + H_2 400°C-20'-1atm	1.3	-	-	-	TiN/TiAl/TiN (1/4/3 nm)	TiN (5nm)
	O* on HK	-	1.9	O* 280°C-10"	-	-	TiN/TiAl/TiN (1/4/3 nm)	-
	H*+H_2 on IL +O* on HK (thin HK)	H* 300°C-10" + H_2 400°C-20'-1atm	1.3	O* 280°C-10"	-	-	TiN/TiAl/TiN (1/4/3 nm)	TiN (5nm)
High thermal budget refs.	PDA 850C ref.	-	1.9	-	He 850°C-1.5"	-	TiN/TiC/TiN (0.5/2/3nm)	TiN (8nm)
	SSA 850C Rel. Ann. ref.	-	1.9	-	-	2/5nm TiN/a-Si +He 850°C-1.5"	TiN/TiAl/TiN (1/4/3 nm)	-
	Gate-First HKMG refs.							

Table I. Experimental RMG splits comprising H*, H_2, O*, and H*+H_2+O* low-T treatments. An "as-deposited" RMG is used as low-T ref., while RMG splits with 850°C post-HK or post-metal "reliability" anneals or a first-generation HKMG with Gate-First integration are used as high-T refs. For V_{th} tuning, a low WFM stack comprising TiN and TiAl(C) is used for nMOS, while a high WFM (TiN) is used for pMOS (see Fig. 5). All the H* splits have a scaled HfO_2 to compensate for the expected EOT penalty due to the reduced IL permittivity.

III. Effects of the O* HK Treatment

The O* HK treatment [11] yields a substantial PBTI reliability improvement at processing T's ≤280°C (Fig. 4a). A 280C-10" O* exposure yields a PBTI reliability comparable to the high-T RMG ref. with an EOT penalty of just ~1.5Å (or ~3Å w.r.t. the the as-deposited RMG ref.) and is thus selected as the HK low-T treatment condition for the transistor benchmark discussed later in Section IV. Longer treatments result in larger reliability improvement but also larger EOT increases (up to ~9Å). The J_g-EOT relation (Fig. 4c) clearly reveals an increase of the IL physical thickness, due to the radicals oxidizing the Si surface. The EOT increase can be reduced by reducing the oxygen content in the remote plasma ambient (e.g., from 100% to 5%, topped up by He, open symbol in Fig. 4), but remains to some extent unavoidable. The O* HK treatment also induces an eWF reduction (Fig. 4b), either by i) reduction of negative dielectric charge, or ii) increase of the total positive fixed charge in the thickened IL due to lower-T oxidation, or iii) enhanced electrostatic weight of the interface positive charge upon EOT increase: Notice, however, that the eWF modulation rate is much smaller compared to the H* IL treatment (cf. Fig. 3b and 4b), and thus the eWF change can be almost neglected for the mild O* treatments inducing acceptable EOT increases (≤3Å).

IV. Benchmark of Low Thermal Budget Gate Stacks with H*, H2 and O* Treatments on a CMOS Platform

In this Section, various low thermal budget RMG gate stacks comprising H*, H_2 and O* treatments (Table I) are evaluated

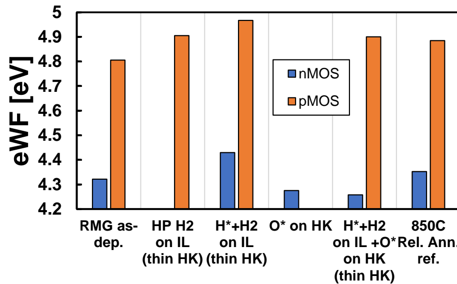

Fig. 5. eWF of each studied nMOS and pMOS split (see Table I), as estimated on the final devices.

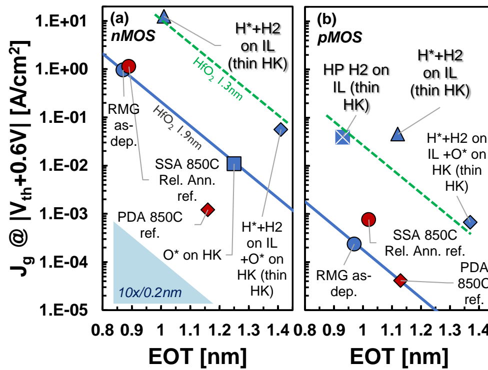

Fig. 6. Gate leakage density evaluated at V_{th}±0.6V in (a) nMOS and (b) pMOS, plotted against the gate stack EOT (from C-V curves). A competitive EOT of 1nm is achieved with H*/H_2 IL treatments combined with a scaled HK. The improved IL quality (increased bandgap) enables scaling of the HfO_2 from 1.9 (solid blue line) to 1.3nm (dashed green line), with a tolerable J_g penalty (nMOS J_g≤10A/cm²). Notice the O* HK treatment always inducing a J_g reduction and an EOT penalty compatible with an increase of the IL thickness (10×/0.2nm).

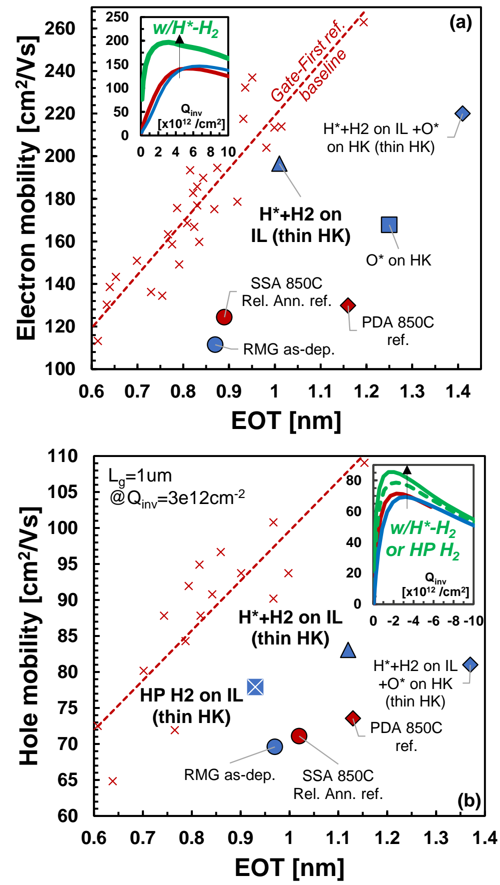

Fig. 7. Long channel split-CV (a) electron and (b) hole mobilities estimated at an inversion charge density of 3×10^{12} cm^{-2}. Insets: mobility vs. Q_{inv} curves for the as-dep. RMG (blue), w/ 850˚C Rel. anneal (red), and w/ H*-H_2 or H_2 IL treatment (green). The improved IL quality with the H*/H_2 treatment enhances the mobilities at thin EOT almost up to the level of the Gate-First baseline, outmatching the high-T RMG counterparts. Note: no boosters (e.g., S/D stressors) were implemented in the planar transistor test vehicle.

on a planar CMOS transistor platform and benchmarked against high-T RMG and Gate-First HKMG counterparts. For proper V_{th} tuning (Fig. 5), consistently with the MOS capacitors results discussed in Sections II and III, a *p*-WFM (TiN) was deployed on the pMOS transistors, while the nMOS transistors employed a *n*-WFM stack (TiN/TiAl/TiN). To compensate for the inherent EOT penalty associated with the lower permittivity of the chemOx after H*/H_2 treatments (see Fig. 3a), the HfO_2 thickness was scaled from 1.9nm to 1.3nm in all the gate stacks subject to IL treatment (see Table I), achieving competitive EOT's down to 1nm. The widened bandgap of the treated IL allows to maintain nMOS gate leakage at operating conditions within ~10A/cm² (Fig. 6a). pMOS gate leakage does not represent a concern (Fig. 6b). The improvement of IL quality by H*-H_2 treatment also results in the best mobility/EOT trade-off (Fig. 7). Both electron and hole mobilities are boosted substantially compared to the as-dep. RMG, outmatching the standard high-T RMG ref. and competing with the Gate-First HKMG baseline. Thanks to the mobility improvement, the I_{ON}-I_{OFF} performance benchmarks of short channel nMOS (Fig. 8) are shown to be comparable to (or slightly better than) the conventional high-T RMG counterparts, despite the remaining ~1Å EOT penalty of the H*-H_2 treated gate stack (see Fig. 6a). The O* HK treatment results in a less favorable performance

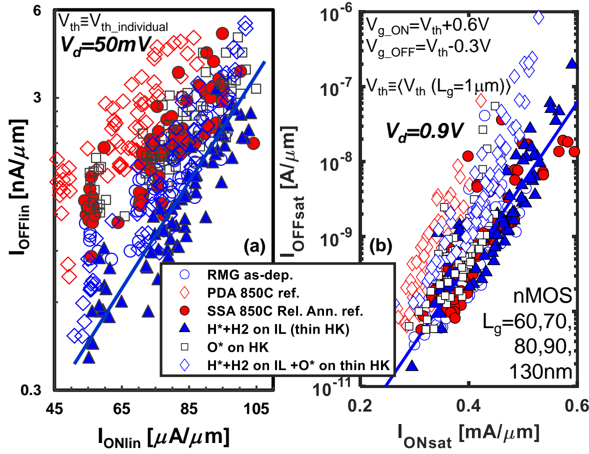

Fig. 8. I_{ON}/I_{OFF} benchmark of short channel nMOS at (a) low and (b) high V_d. Thanks to the improved IL quality and electron mobility, the performance of the H*+H$_2$ treated gate stack matches (or slightly outmatches) the as-dep. and high-T RMG refs. despite a ~1Å thicker EOT (see. Fig. 7a).

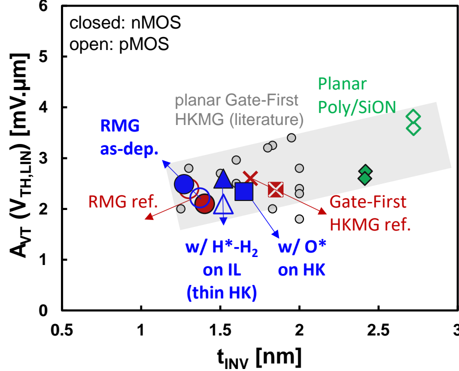

Fig. 9. V_{th} mismatch (A_{VT}) as evaluated with matched pairs (Pelgrom plot) of nMOS and pMOS device populations with gate areas in the range 0.01-1µm^2 and L_g's in the range 0.07-1µm. No increase of stochastic variability is observed in the low-T RMG gate stacks, irrespective of the applied treatments.

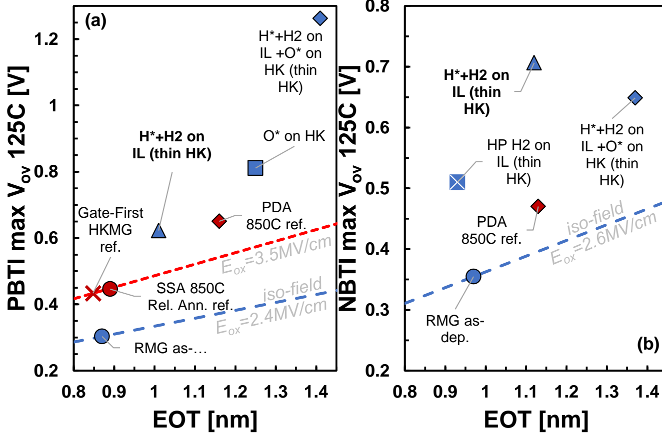

Fig. 10. BTI maximum operating overdrive of long channel (L_g=10µm) (a) nMOS and (b) pMOS as estimated with fast-sensing (t_{sense}=1ms) eMSM stress sequences at various stress V_g's (failure criterion: ΔV_{th}=6.65mV after 1ks stress at 125°C, corresponding to 50mV at 10 years). The H*-H$_2$ IL treatment yields best NBTI and PBTI at 1nm EOT.

benchmark, due to the ~3Å penalty associated with the IL regrowth, which cannot be compensated by a tolerable HK thickness reduction. A similar consideration applies to the gate stack subject to both H*-H$_2$ IL treatment and O* HK treatment (total EOT penalty ~5.5Å).

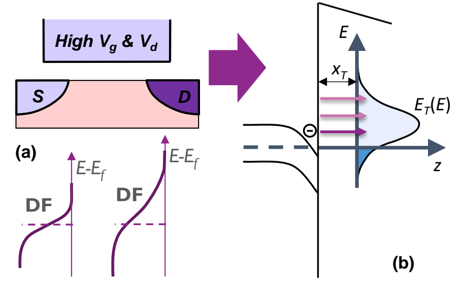

Fig. 11. (a) Sketch of the non-equilibrium carrier energy distribution function (DF) towards the drain side of a short L_g device stressed with high V_g and high V_d (Channel Hot Carrier stress). (b) Highly energetic carriers can get trapped also in dielectric defect levels at higher energies.

This first demonstration of low thermal budget RMG gate stacks in a scaled CMOS transistor platform allows us to investigate also the stochastic device variability, by utilizing statistical V_{th} datasets of matched pairs across wafer [13]. No degradation of the matching parameter (A_{VT}) is observed in the devices with low thermal budget RMG as compared to high-T counterparts, irrespective of the deployed treatments (Fig. 9).

Fig. 10 reports the BTI reliability benchmark of long channel transistors. Consistently with the MOS capacitor results presented in Section II, excellent pMOS NBTI reliability is achieved with the H*-H$_2$ IL treatment (Fig. 10b). Interestingly, the same gate stack also yields the best nMOS PBTI/EOT tradeoff (Fig. 10a), ascribed to the improved IL quality beneficial also for suppressing charge trapping into HK electron traps. In scaled L_g devices stressed at high V_g and V_d, the non-equilibrium carrier energy distribution at the channel drain side is expected to cause charge trapping in a wider energy range of dielectric defect levels (Fig. 11) [14]. Degradation maps [15] measured at various V_g/V_d stress combinations allow to estimate the "safe operating area" (SOA) of each nMOS flavor by taking into account also Channel Hot Carrier degradation (Fig. 12). Due to the large defect density in both the IL and HK when omitting the high-T "reliability anneal", the as-dep. RMG ref. shows a small SOA compared to the high-T counterpart (Fig. 12b vs. a). The H*-H$_2$ IL treatment improves the overall reliability (Fig. 12c) thanks to improved IL quality and suppressed tunneling towards HK defects, yielding a nMOS SOA comparable to the high-T RMG ref. The operating V_{DD} enhancements induced by the various treatments, as estimated from the SOA of each gate stacks, are reported in Fig. 13: once again the H*-H$_2$ IL treatment results in the best reliability/EOT tradeoff, matching the high-T refs. at comparable EOT.

V. Conclusions

We discussed novel low thermal budget RMG gate stack solutions, based on hydrogen and oxygen radical treatments. A H* IL treatment at T≤300˚C reduces the density of H-E' defects in SiO$_2$, resulting in improved pMOS NBTI reliability, increased eWF due to a reduction of the IL positive fixed charge, and reduced gate leakage, at the cost of 1-3Å inherent EOT penalty related to the removal of OH groups lowering the k-value of the chemOx IL. An early H$_2$ sintering anneal at 400-450˚C before HKMG deposition provides a limited amount of H* radicals without plasma processing, by cracking of the hydrogen molecule at native interface P_b defects, resulting in a

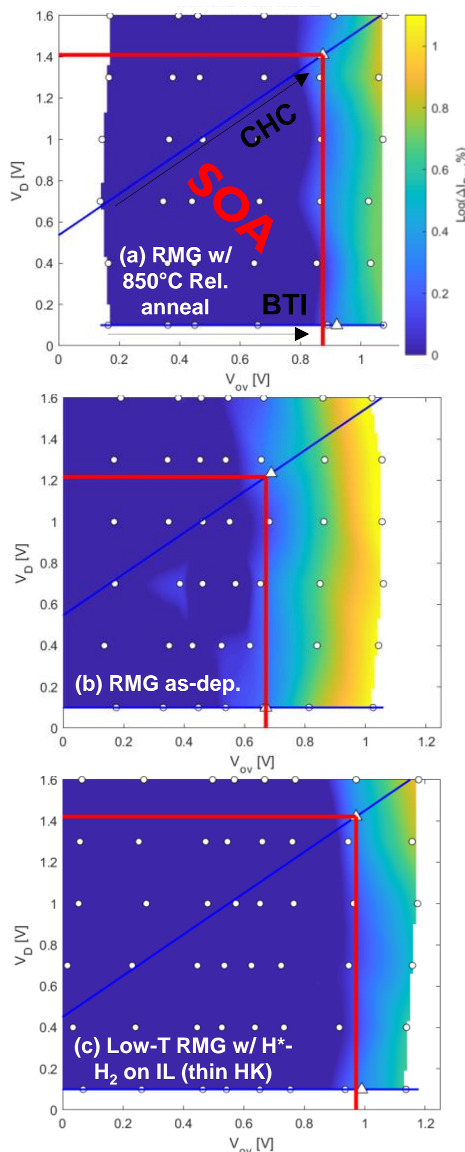

Fig. 12. Degradation map measured (a) in a ref. high-T RMG short L_g nMOS for different V_g/V_d bias combinations (each circle demarcates a tested condition). The device "safe operating area" (SOA, red rectangle) is determined within the stress V_{DD} (triangles) inducing a 2% I_{Dsat} drop after 0.5ks of stress at 25°C on the BTI (high V_g, low V_d) or on the CHC (V_g=V_d) cutlines. (b) The SOA is substantially reduced when omitting the high-T reliability anneal, but (c) is recovered with the H*-H_2 low-T IL anneal.

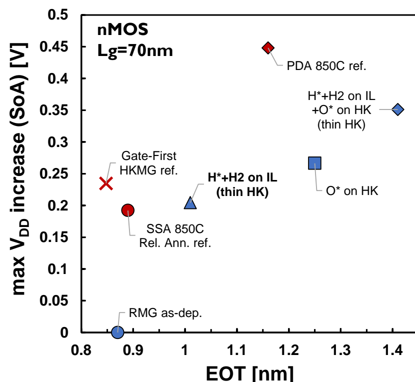

Fig. 13. Benchmark plot of the nMOS SOA V_{DD} increases (as estimated from the degradation maps, cf. Fig. 12) achieved with the various gate stack treatments, referred to the as-deposited RMG ref.

sizable improvement of the IL quality with a minimum EOT penalty of ~1Å. An O* HK treatment reduces the density of V_o defects in HfO_2, resulting in an improved nMOS PBTI reliability; however, this treatment induces an unavoidable EOT penalty of 2-3Å due to re-oxidation of the Si surface. Low thermal budget RMG gate stacks employing (combinations of) these radical treatments were deployed on a planar CMOS transistor platform and benchmarked against conventional high-T gate stacks. The H*/H_2 IL treatment was shown to provide a complete low-T RMG CMOS solution, due to the improved IL quality resulting in improved pMOS and nMOS performance and reliability. By deploying this IL treatment all the key electrical metrics of a ref. high-T RMG stack were matched (or outmatched), including hole and electron mobilities, NBTI and PBTI reliability, V_{th} matching, short channel nMOS performance and Safe Operating Area (Channel Hot Carrier reliability). The improved IL quality allowed also to scale the HK thickness to 1.3nm, partially compensating for the EOT penalty associated with the k-value decrease of the chemOx IL. The low thermal budget gate stack innovations presented here are expected to simplify the RMG integration in advanced device architectures (e.g., nanosheets), and to become enablers for upcoming CMOS technology innovations, such as Sequential-3D integration and CFETs.

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