EUV Single Patterning Validation of Curvilinear Routing

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ABSTRACT

Transistor pitch scaling drives the evolution of chip design. The late arrival of EUV lithography prompted the adoption of multiple patterning using 193i to continue transistor scaling. To facilitate multiple patterning integration schemes, the 2D design style was abandoned and unidirectional design style became dominant. As transistor scaling continues further, the demand on routing resources can exceed their supply leading to routing congestion [1]. Exploration on 1.5D or curvilinear routing to resolve higher Metal 2 usage was studied [2]. Nowadays, EUV lithography re-introduced single patterning for the most advanced nodes. At the same time, Multi Beam Mask Writer (MBMW) enables true curvilinear masks [3]. The use of curvilinear routing can potentially resolve routing congestion and more relax design rule check by combining EUV lithography and MBMW. This paper focuses on the challenges in optical proximity correction (OPC) on a design with curvilinear routing. Wafer data will be evaluated to assess quality. The target design is a D-flipflop using 2D and curvilinear features in a local interconnect layer to reduce the congestion. The base pitch of this design was scaled from 40nm to 32nm. The test design was then OPCed using Model Based OPC and Inverse Lithography Technique. Finally wafer data and process window analysis across the pitch range from different OPC variations will be revealed.

Keywords: EUV single patterning, curvilinear routing, pitch 32, ILT

1. INTRODUCTION

1.1 Design restrictions on interconnect layers and its impact on resistance-capacitance (RC) performance and design rule check (DRC)

Figure 1 briefly shows the evolution of metal routing over time. The routing style initially used in order technology nodes was bidirectional, that has been changed to unidirectional with time for advanced nodes. This is mainly because of changing in integration scheme to achieve smaller device thus leading to the need of more complex metal processing. The reduced metal critical dissensions also lead to reduced cross-sectional area of the metals. Curvilinear routing could be introduced to overcome some of these challenges because it allows more direct pin connection and reduces number of vias. It has potential to improve the timing closure as well as provide more cross-sectional areas in required upper metal layers. It will also allow more relax DRC by having omnidirectional routing. This could be implemented if manufacturability of such curvilinear schemes become a practical reality.

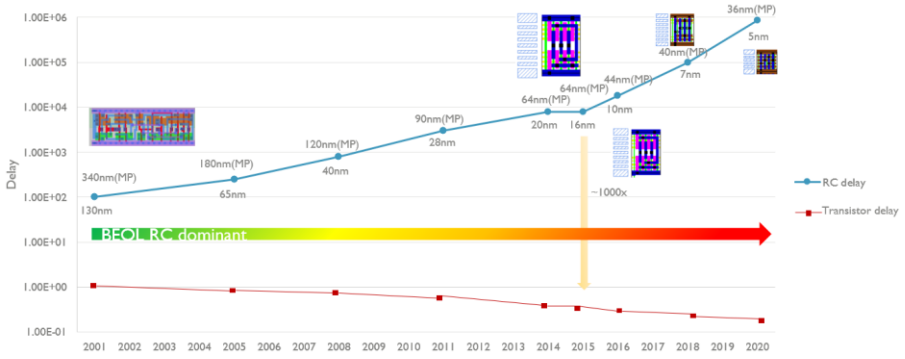

Figure 1. Evolution of BEOL layer routing towards sub-14/10nm nodes and growing gap between transistor delay and RC delay.

Adapted graph from [4], IEEE,2013.

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1.2 Single expose EUV on P32 unidirectional routing, emergence of MBMW and cost of ownership

Extreme ultraviolet (EUV) lithography has emerged as a promising solution for the single exposure of sub 193i feature resolution limit and complex geometries, including curvilinear shapes. Imec studied an option to use single exposure EUV (SE EUV) to replace M1 as M2 for Self-Align-Double-Patterning+block and Self-Align-Quadruple-Patterning+block respectively [5]. It shows viability of SE EUV in iN7 node (foundry N5 equivalent) for Back-end-of-line (BEOL) layers which has design rules based on 42nm pitch for Metal 1 and 32nm pitch for subsequent Metal 2 and metal 3. The process of BEOL layers was investigated in full SE EUV patterning (litho and etch). Figure 2 shows that the design being investigated is restricted to unidirectional type of routing which indeed the case for iN7 node design rules. SE EUV is foreseen to be currently achievable down to 32nm pitch but limited to 18nm T2T. The proven SE EUV for pitch 32nm become the reference for the design experiment of our learning where the pitch is scaled between 40nm and 32nm.

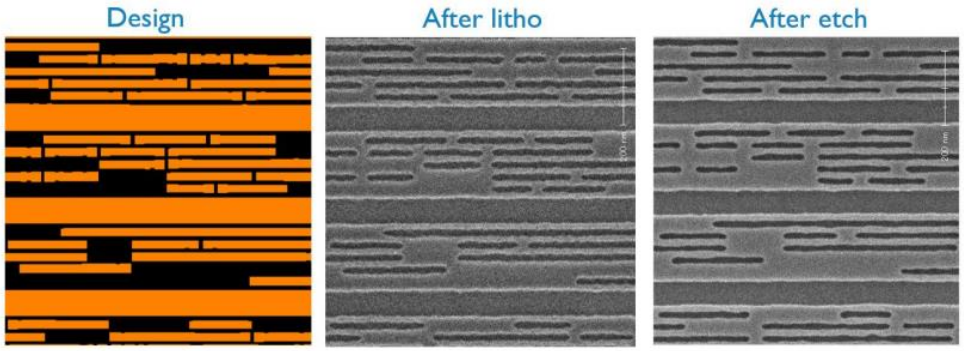

Figure 2. M2 1D design intent with pitch 32nm, 24nm T2T and SEM wafer image after litho and etch by using SE EUV [5].

The successful work of SE EUV patterning in replacing multi-patterning of 193i for BEOL layers requires heavily on the precision of the mask writer, because the features size is smaller for EUV masks. Furthermore, curvilinear features have more vertices thus significantly increase data size. The readiness of MBMW overcomes this challenge in practical reality and making it a critical component. The raster scan methods used by MBMW enable write time independent of data complexity, which makes it have reasonable writing time compared to variable shape beam (VSB) writer. Figure 3 shows the writing time of MBMW is independent of shot count, which is correlated to number of vertices required to compose the features but areas, whereas write time required by VSB depends on both. Since MBMW is mainly used for EUV technology, the turn-around-time (TAT) remains longer than VSB writer in 193i because exploding of data volume in EUV mask.

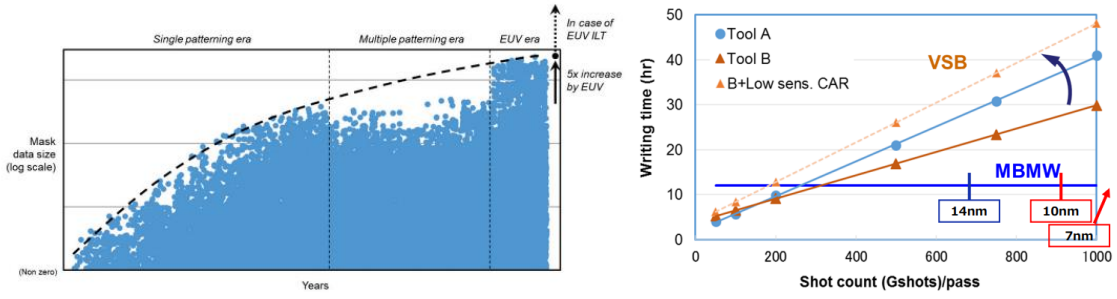

Figure 3. Mask data volume over the years (left)[3]. Writing time comparison between VSB and MBMW as a function of the shot count. Shot count is linearly related to data size (right) [6]

Combination of EUV technology and MBMW for manufacturability of advance technology nodes enable potential use of curvilinear features on the design. Furthermore, replacement of 193i multi-patterning for BEOL layers can be replaced by SE EUV thus have an impact in reducing wafer cost [5].

2. METHODOLOGY

An experimental curvilinear metal routing design is created within iN5 standard cell library by scaling up the pitch range from 32nm to 40nm for BEOL layers. The reason for this due to better routing optimization with buried power rail architecture and SE EUV is viable with pitch down to 32nm. The direct implementation of curvilinear routing in existed standard cell library could help to describe how it will impact most likely the congestion of interconnect system at least in intracell thus relaxing the design rule. A D-flipflop cell is selected as routing optimization for MINT layer as the design of experiment (Figure 4).

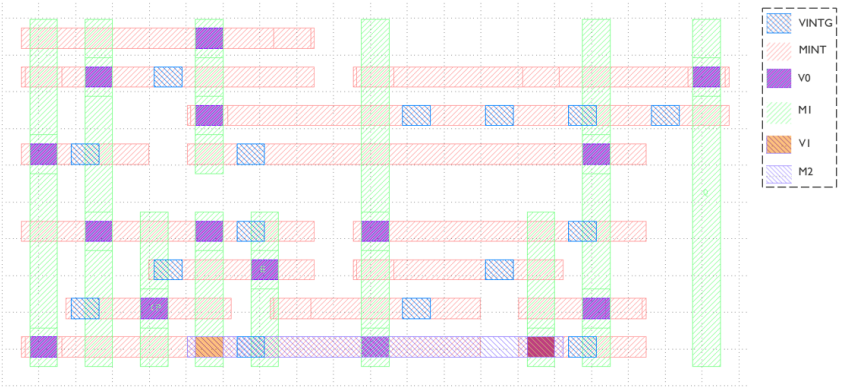

Figure 4. Interconnect layers of CKLNQD4 cell library

Routing optimization is started with classifying series of pin connections and extracting the coordinates of each pin then later shortest path connection is used for the routability (Figure 5). A priority is assigned to each series from maximum to minimum number of pins. The priority assignment is done mainly as hypothetical method to minimize cross-section area caused by lower number of pins and avoid introducing new metal layer to continue the wiring. A mathematical equation (2) can be used to define the priority of a given set of N finite series of pin connection represented by the set $S = \{s1, s2, s3, ..., sN\}$. The number of pins of each series can be represented as n_i. The priority assigned to each series can be defined as a function $P(n\_i)$ such that:

$P(n\_i) = k$, where k is an integer and $1 <= k = N$ and k represents the priority of series Si (1)

The mathematical equation to assign priority based on the number of pins in each series can be expressed as follows:

$P(n\_i) = N - rank(n\_i) + 1$, where $rank(n\_i)$ is the rank of n_i in the set S, sorted in decreasing order. (2)

In other words, the priority of a series is directly proportional to the number of pins it has, with the series having the maximum number of pins being assigned the highest priority and the series with the minimum of pins being assigned to lowest priority.

A generated routability between the assigned pins is done and the final routing is optimized by considering mask-rule-check and litho printability assumptions (Figure 6). One cross-section area is created due to the minimum number of congestions has been reached.

Figure 5. Classified series of pins connection and priority assignment (left). Extracted pins coordinate respected to priority assignment (right)

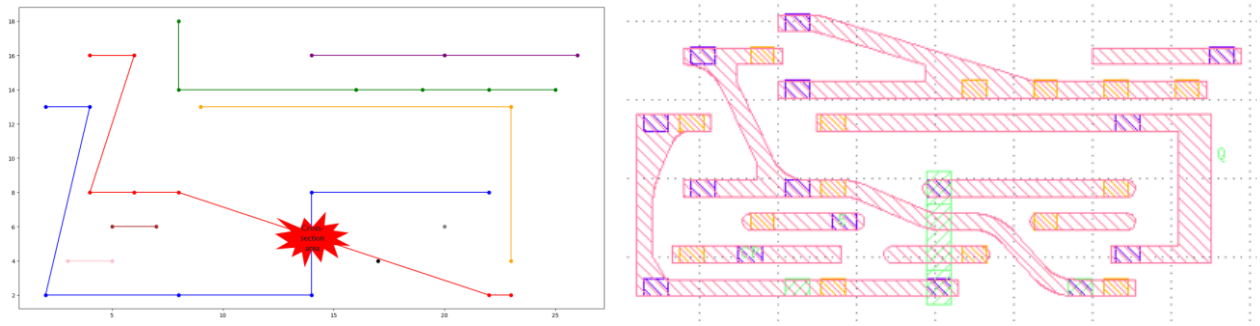

Figure 6. Generated routability pin connections (left) and drawing optimization of MINT layer considering mask rule check (MRC) and litho printability assumption (right).

Investigation on this curvilinear routing manufacturability is limited to litho process. The mask is fabricated using MBMW along with mask process correction (MPC) applied. Wafers are single exposed using ASML NXE3400 scanner with an optimized source generated by commercial SMO tool.

Dark field photomask is used. Patterns of photomask are transferred onto the wafer with positive tone development (PTD) process to form trenches topography by using CAR resists.

FEM wafer is exposed to validate the printability process and combination of measurement tools are used.

1. CD SEM metrology using Hitachi CG6300 to obtain 10 images per die locations.
2. Image averaging to reduce CD SEM image noise for contour extraction.
3. MetroLER is used for further measurement and metric analysis such as overlap process window (OPW), exposure latitude (EL), depth of focus (DoF) and line edge roughness (LER).

3. EXPERIMENTAL RESULTS

3.1 Optimized routing overview

Implementation of the routing optimization method is applied to the existed iN5 standard cell library to review the overall impact across cell libraries. The routing replacement by curvilinear shape could reduce the wiring congestion due to restriction of unidirectional type of routing. Therefore, DRC is relaxed and more routing areas for the required upper metal layer. Figure 7 shows the overview of comparison between pre-optimized and post-optimized MINT routing. The number of cross-sectional areas is proportional to number of wires required for each cell. M1 and M2 wirings are reduced by optimizing unidirectional type of routing into curvilinear at all angles by 82% and 100% respectively across the cell library.

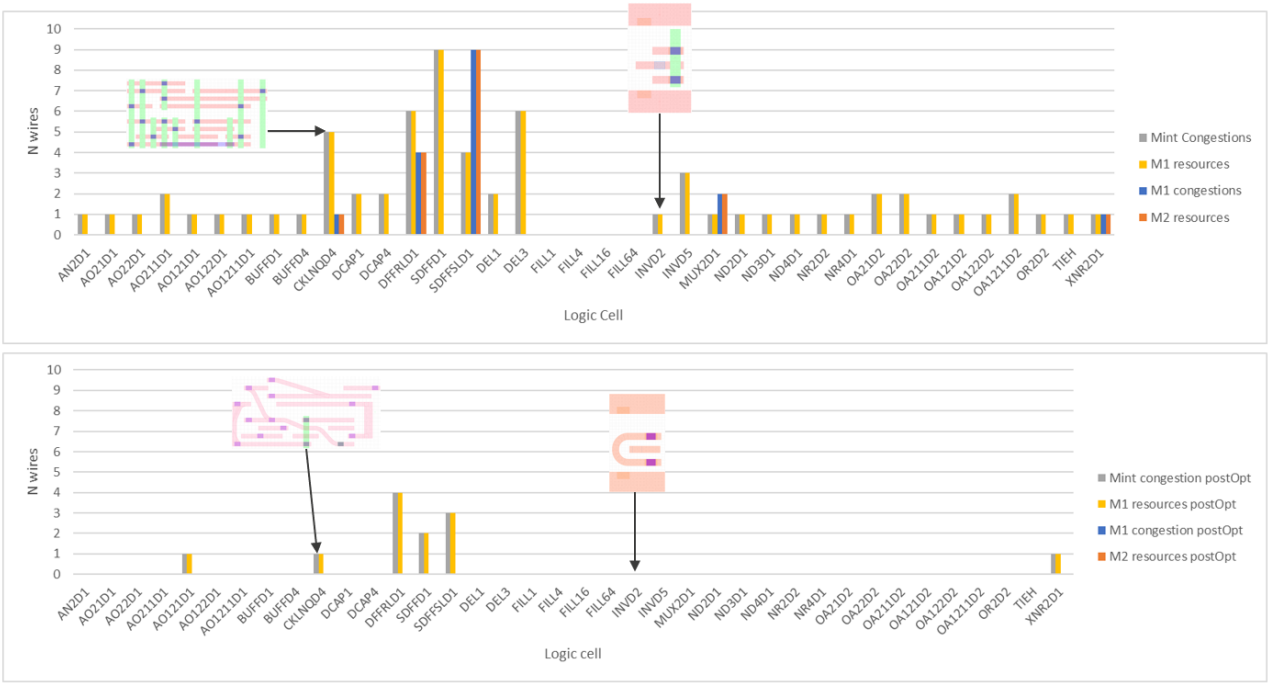

Figure 7. pre-optimize MINT routing (top) and post-optimize MINT routing (bottom) across standard cell library.

3.2 Mask data analysis

CD measurement analysis is performed between target input mask and the actual printed mask seen on SEM image based on cutlines placement. The estimation is considering the noise reduction by averaging SEM images to obtain better contour extraction and grid snapping occurrence on extracted contour. Figure 8 shows the delta of measured CD on the extracted contour is around -2nm compared to ILT (inverse lithography technique) mask design. All the assist feature is shown manufacturable with minimum 2D feature size approximately 9.4nm by 13.4nm generated by minimum width and space of sub-resolution-assist-feature (SRAF) 8nm set in ILT recipe (Figure 9).

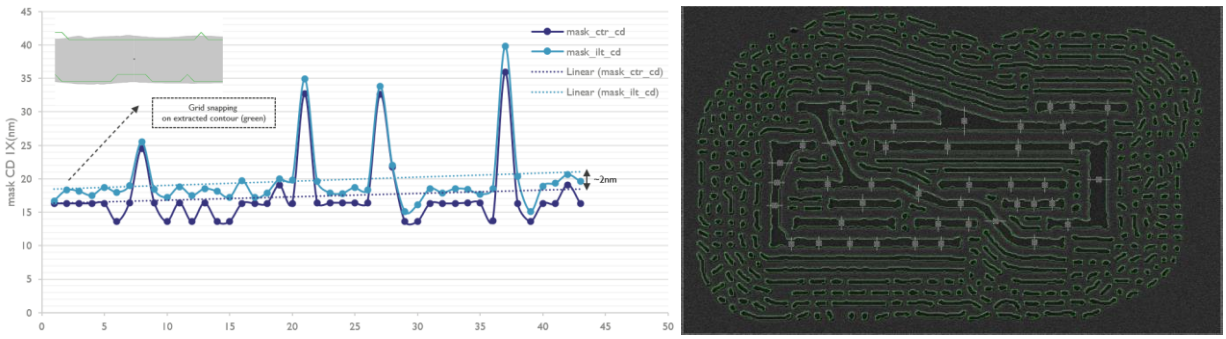

Figure 8. Mask CD distribution between ILT design and extracted contour in 1X (left). Overlayed mask SEM image and extracted contour with marker information for cutlines measurement (right)

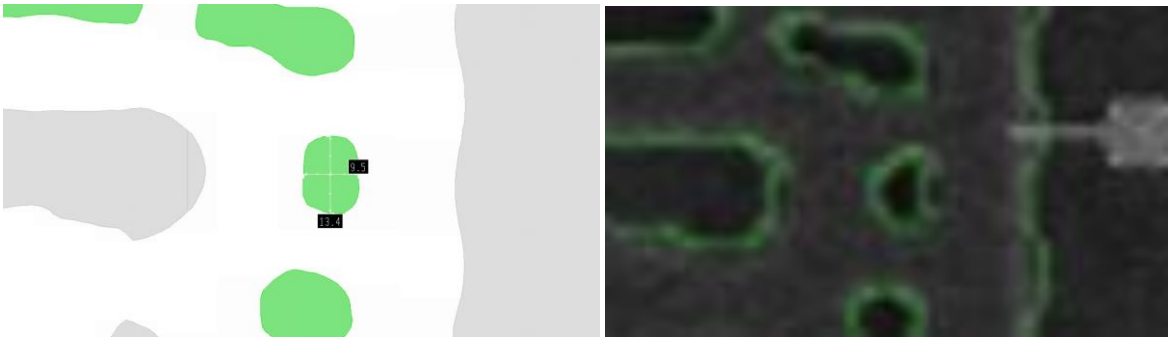

Figure 9. smallest 2D feature size of SRAF generated by ILT (left) and its mask SEM image (right). Minimum width and space are 8nm in the recipe.

3.3 Conventional model based OPC (MBOPC) and ILT implementation and simulation

Conventional MBOPC works with edge fragmentation and only compatible on Manhattan edges. Therefore, Manhattanizing and staircasing is implemented with the step size 10nm for P40 and 8nm for P32 on curvilinear features prior applying the edge fragmentation and correction. The chosen step size is considered after tuning in the recipe to get the best convergence.

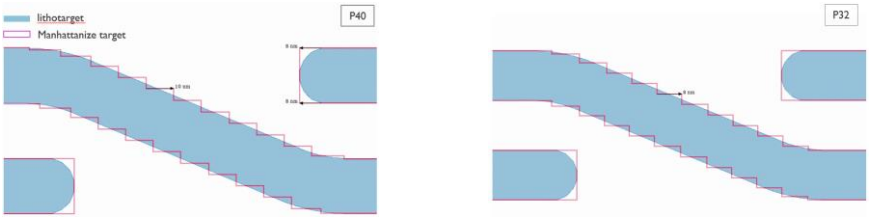

Figure 10. Manhattanized target with 10nm step-size for P40 (left) and 8nm step-size for P32 (right)

In the other hand, the nature of ILT where the correction applied is not based on edge fragmentation, but as a set of sub-resolution features rather than a set of geometric shapes. It is effective to be implemented on curvilinear design without manipulating the target design in prior because it works based on pixel intensity, as the optimization process involve adjusting the intensity of the pixel to achieve the convergence of target.

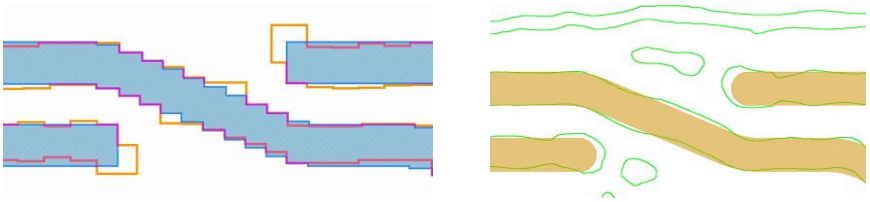

Figure 11. MBOPC on manhattanize target (left) and ILT mask on curviliniar target (right) on P32

Figure 12 shows printability after litho on pitch 40nm is visually observed between simulation and wafer. Both conventional model-based OPC and ILT showed no micro-bridging or line-end-pull-back (LEPB). Considering the ILT to be computational expensive and known to have longer runtime thus MBOPC still seems to be reliable to be implemented for P40. However, ILT showed better convergence on non-manhattan feature compared to conventional MBOPC solution (Figure 13).

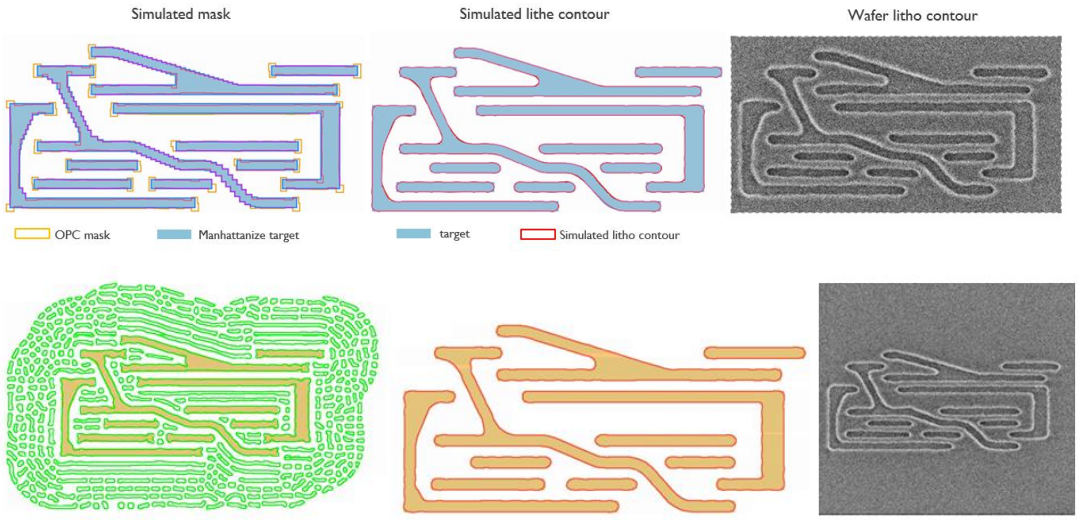

Figure 12. Simulated mask of MINT curvilinear routing with MBOPC mask, simulated litho contour and SEM image after litho (top) and ILT solution (bottom) on P40.

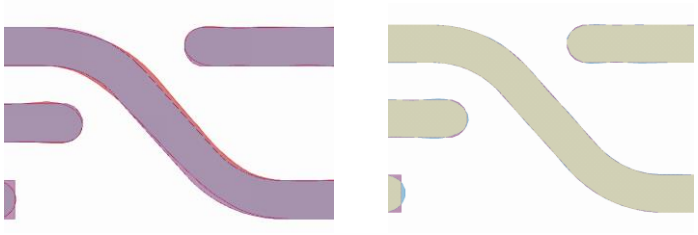

Figure 13. Simulated contour to target of conventional MBOPC (left) and ILT (right) with pitch 40nm.

Line-end-pull-back (LEPB) started to appear as pitch getting smaller down to 32nm observed in simulation output (Figure 14). This can cause interconnection issue when there is a contact overlay. In this case, designer can be informed not to draw rounded-corner-to-angled-line (RC2AL) less than ~15nm. An illustration to define such RC2AL can be described in Figure 15. The distance measurement is search based on radius of a point which placed on corner region against the intersection of external edge. Minimum value of the search can be an input for design rule manual (DRM).

Furthermore, P40 and P32 are investigated to observe the printability of ILT solution on litho wafer. ILT shows better convergence to lithotarget down to P32 where LEPB started to appear using conventional MBOPC.

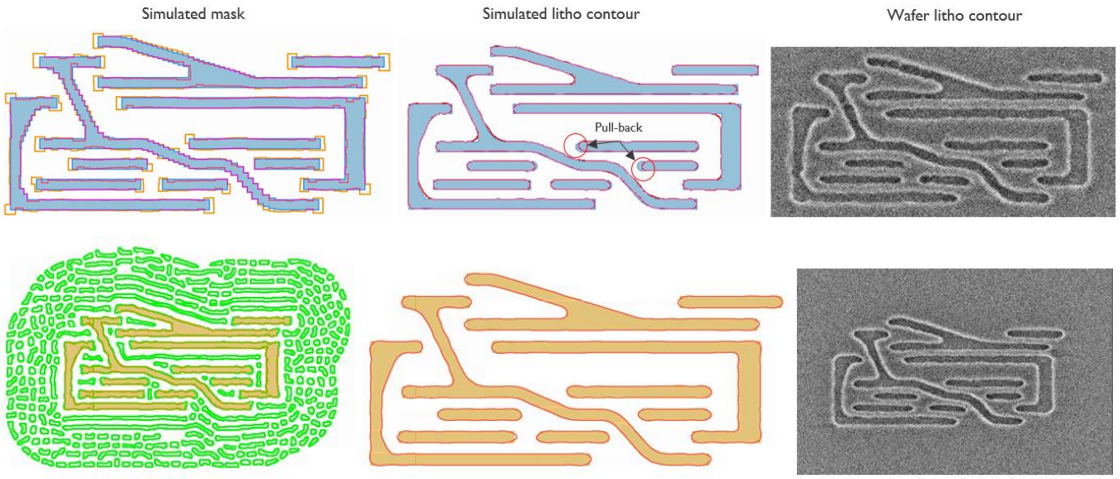

Figure 14. Simulated mask of MINT curvilinear routing with MBOPC mask, simulated litho contour and SEM image after litho (top) and ILT solution (bottom) on P32.

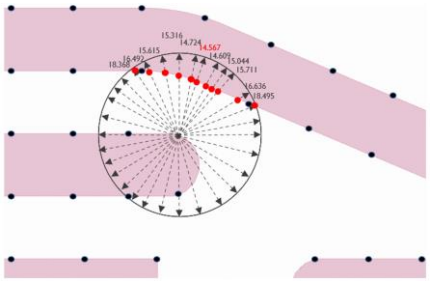

Figure 15. Minimum distance of rounded-corner-to-angled-line based on radius based point search

The SRAF placement of ILT is based on typical litho model through process condition and the same nominal model is used for conventional MBOPC implementation.

Edge placement error (EPE) on simulation result is done by comparing both MBOPC and ILT performance for pitch 40nm and 32nm. ILT tends to give lower defect frequency compared to MBOPC by ~20%. ILT shows smaller EPE range with ~1.5nm for pitch 40nm (Figure 16) and ~2nm for pitch 32nm whereas MBOPC gives EPE range ~2.5nm and 3.5nm respectively (Figure 17). EPE is increasing for both MBOPC and ILT as the pitch getting smaller.

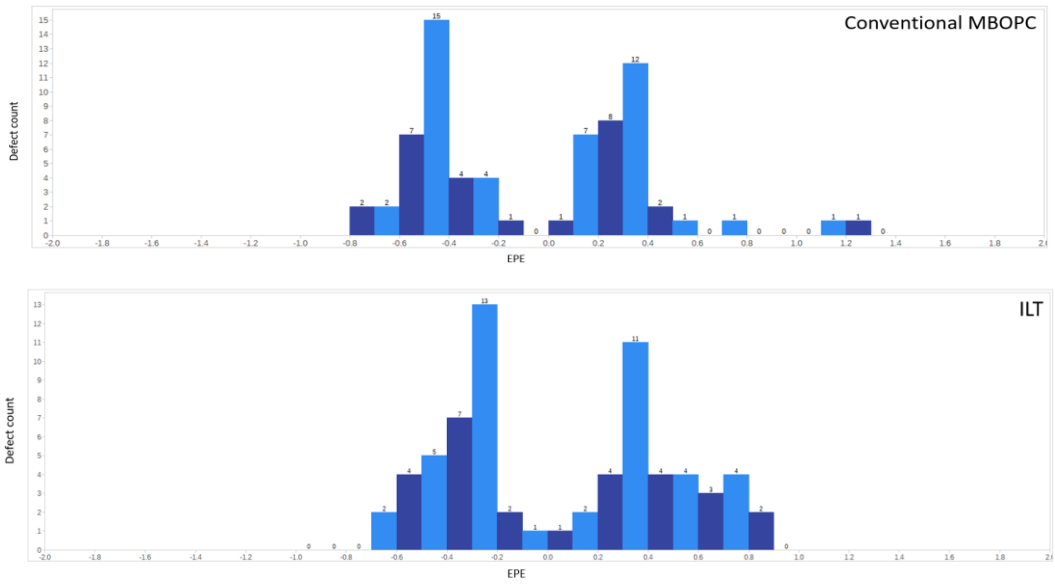

Figure 16. Edge placement error (EPE) statistic between MBOPC and ILT with P40

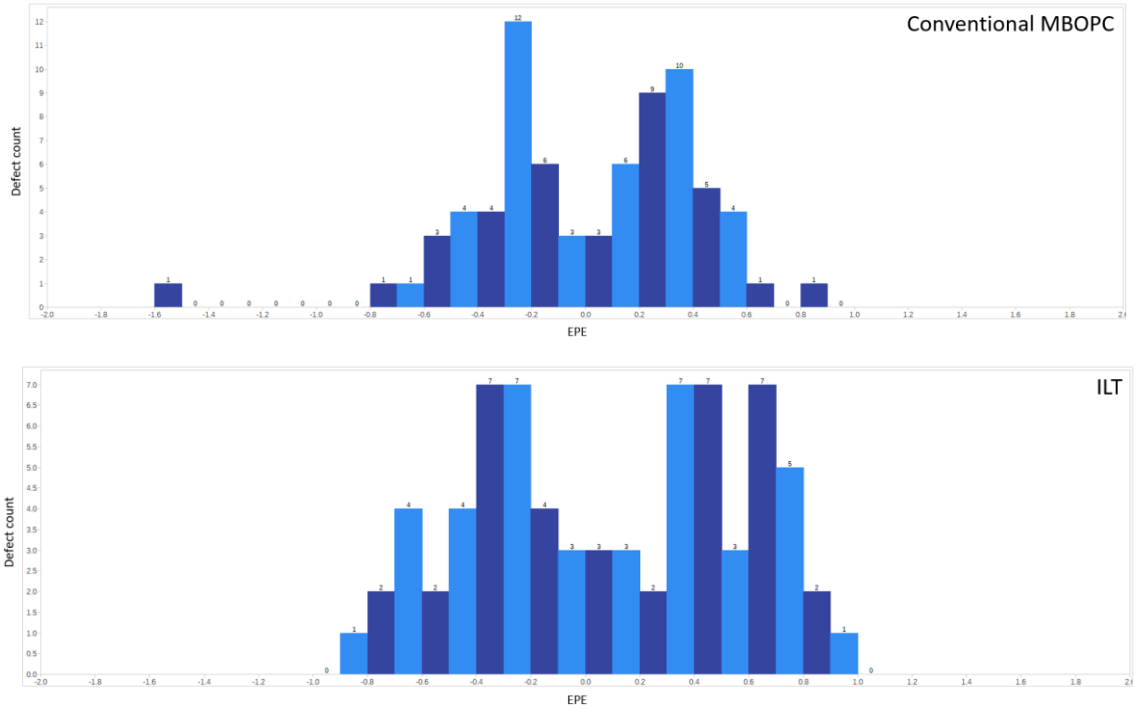

Figure 17. Edge placement error (EPE) statistic between MBOPC and ILT with P32

3.4 Overlap Process Window (OPW) of litho wafer data.

Nominal dose of 77mj/cm^2 is used to expose FEM wafer. We used a probabilistic process window [7] to estimate the best process condition. Local measurement is done on four different gauges with distinguished feature configurations (Figure 18). These gauges are considered as parametric structures for analysis.

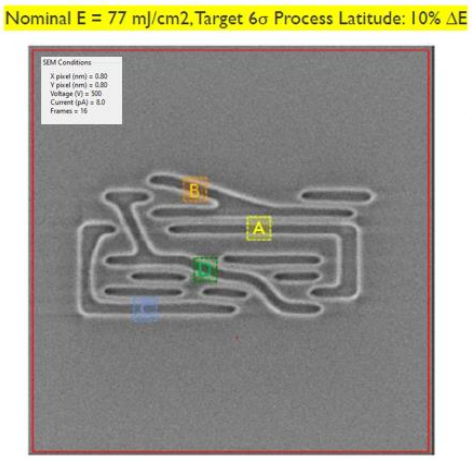

Figure 18. Parametric features A, B, C and D for CD based process window analysis.

Figure 19 shows defect process window for pitch 40nm which conventional MBOPC solution is mainly limited to micro-bridging defects in under-expose area whereas ILT is limited to SRAF printing in over-expose area. If we look at the ED plot (Figure 20), conventional MBOPC solution provides more depth-of-focus (DoF) than ILT by ~30nm difference. However, ILT gives more Exposure-Latitude (EL) than conventional MBOPC by ~5% difference.

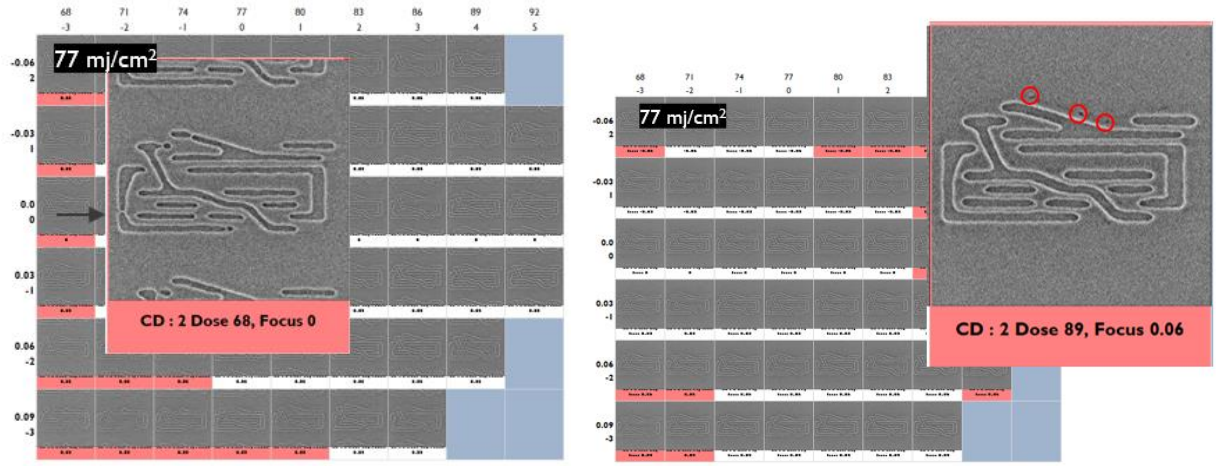

Figure 19. Defect process window based on conventional MBOPC (left) and ILT (right) solution for pitch 40nm.

The probabilistic process window uses ±3σ process errors within the fraction-in-specification 60nm DoF and 10% Exposure Dose. Figure 21 shows the probabilistic process window which define the best process condition for pitch 40nm test design is in ~-6nm defocus and ~3% exposure dose (75 mj/cm^2) for ILT solution while conventional MBOPC would need ~12nm defocus and ~5% delta dose (81 mj/cm^2).

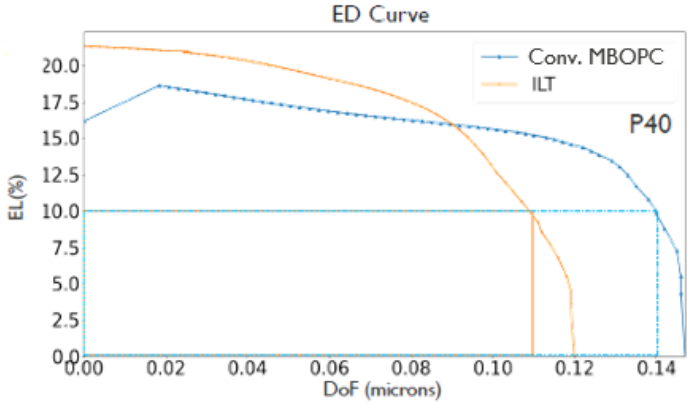

Figure 20. ED curve of ILT and conventional MBOPC solution for pitch 40nm.

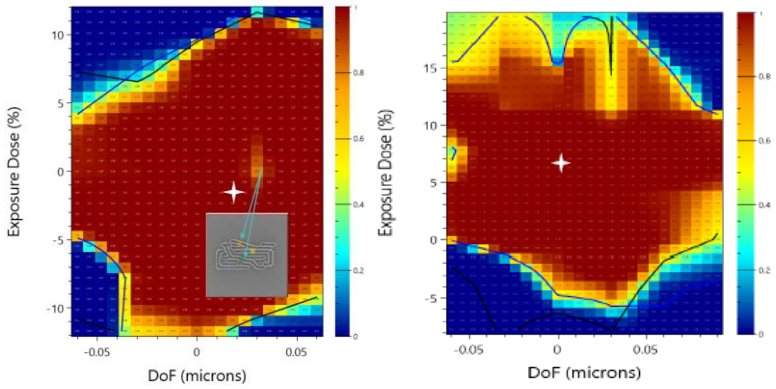

Figure 21. Probabilistic process window of ILT (left) and conventional MBOPC (right) for pitch 40nm

Overlap process window for pitch 32nm is observed on same condition and parametric features as pitch 40nm. Both ILT and conventional MBOPC solution would require higher energy dose compared to pitch 40nm. Figure 22 shows that conventional MBOPC does not give OPW while ILT solution could still maintain the OPW within our specification. The result indicates ILT outperform conventional MBOPC, which allows more precise SRAF insertion by introducing curvilinear features.

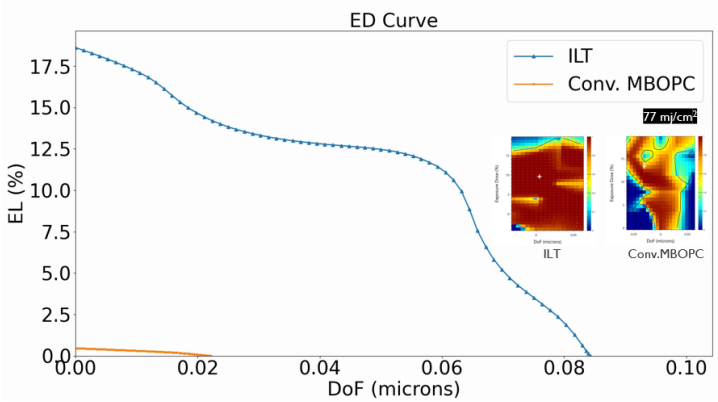

Figure 22. ED curve of ILT and conventional MBOPC solution for pitch 32nm.

Furthermore, we analyse OPW of ILT solution through pitch from 32nm to 40nm (Figure 23). The DoF is dramatically dropped by ~30% towards pitch 32nm due to SRAF printing. Although ILT solution maintains to obtain OPW within the specification but it could be improved with more calibrated SRAF printability model.

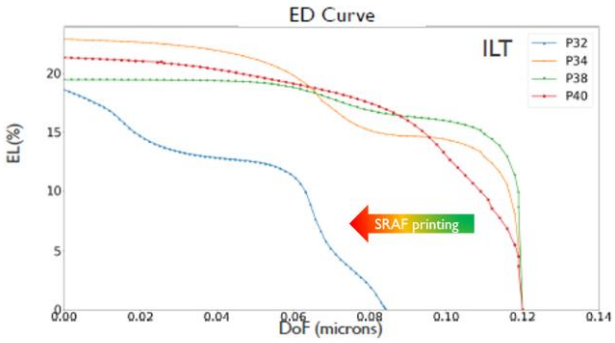

Figure 23. OPW for ILT through pitch.

3.5 Line edge roughness (LER)

The unbiased LER measurement is considered on top of the averaged image contour. Assuming the error of the averaged image is systematic and linear, we consider only the unbiased measurement after the noise removal of averaged image. The LER is locally observed on the line structure from the test design which has isolated edges on one side and dense edges on the other side (Figure 24) within the measurement window size of 50nm (width) by 300nm (length). Figure 25 shows the edge roughness is lower towards pitch 32nm for isolated edge but higher on dense edge. We also look at the impact of ILT and conventional MBOPC solution on the edge roughness between pitch 32nm and 40nm. Figure 26 shows conventional MBOPC and ILT seems to have negative correlation but does not have strong correlation to the pitch at dense edge. In the other hand, ILT could gain lower edge roughness than conventional MBOPC at isolated edge.

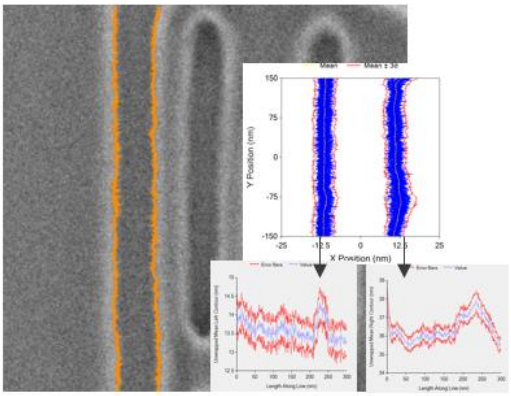

Figure 24. The LER is locally observed on the line structure from the test design which has isolated edges on one side and dense edges on the other side within the measurement window size of 50nm (width) by 300nm (length)

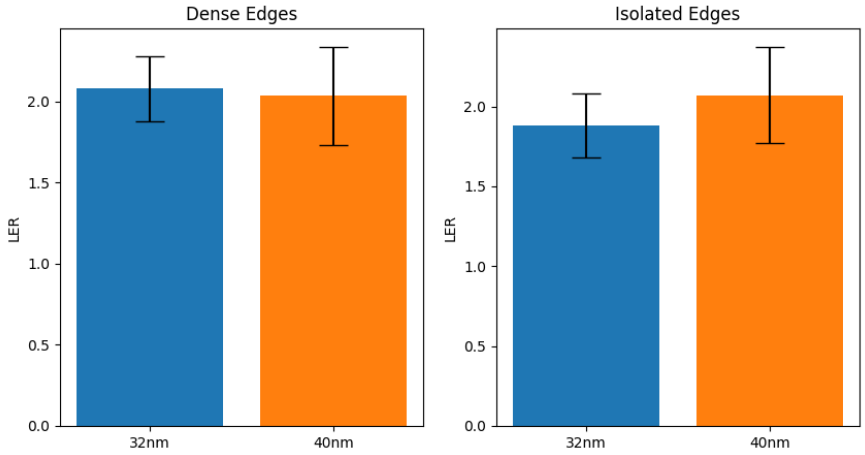

Figure 25. The edge roughness between pitch 32nm and 40nm respected to dense edge (left) and isolated edge (right)

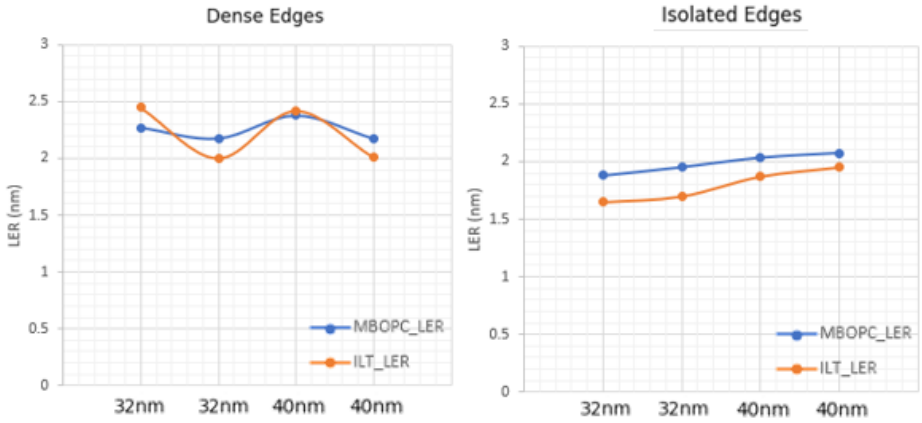

Figure 26. The edge roughness between pitch 32nm and 40nm based on ILT and conventional MBOPC solution respected to dense edge (left) and isolated edge (right)

4. CONCLUSIONS

Curvilinear with all angle routing is experimented on standard cell level within iN5 platform with buried power rail by optimizing MINT routing. The optimized routing overview across cell library shows significant reduction of M1 and M2 usage by 82% and 100% respectively compared to Manhattan based routing. The pitch is scaled from 32nm to 40nm to accommodate the proven of single expose EUV with 0.33NA on pitch 32nm to replace 193i multi-patterning on BEOL layers. Curvilinear routing has been validated to be manufacturable on wafer with single expose EUV from P40 and P32 thus more relax DRC should be allowed in order of magnitude. Linear correlation of measured CD is shown on the extracted contour but with Δ~-2nm compared to ILT mask design due to thresholding. SRAF presence on ILT could give OPW down to pitch 32nm in lower dose, lower EPE defect frequency with smaller EPE range and lower roughness on isolated edges. But it would need a robust SRAF printability model and generation control if not the SRAF will highly become limiter and negatively impact OPW. Conventional MBOPC gives comparable OPW to ILT on pitch 40nm even without assist features therefore absent of SRAF could increase DoF. Furthermore, ILT is useful as solution for better convergence on area limited by MRC where LEPB starts to occur when using rectilinear based correction (conventional MBOPC). This study can be extended to future nodes when requiring high-NA EUV to pattern sub 30nm pitch if design started to implement curvilinear routing in practical reality.

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