High-Speed SiGe BiCMOS Circuits for Optical Communication

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***Abstract*—This paper presents an overview of SiGe BiCMOS circuits for next-generation optical communication links targeting 100 GBd PAM4 modulation per wavelength to support 4-lane 800Gb and 8-lane 1.6Tb Ethernet. Signal generation at these rates is challenging. For this, an analog multiplexer making use of return-to-zero (RZ) modulation is presented. The explicit RZ generation enables equalization of the interleaved signal. Higher equalization orders are obtained with a 120 GBd PAM4 4-to-1 multiplexer with a mixed-signal 7-tap feedforward equalizer. The equalizer consists of a combination of digital delay cells and analog delay cells enabling a compact and power efficient solution. Quad-channel modulator drivers and receivers finish the required high-speed circuits. Based on traveling-wave architectures high gain-bandwidth products are realized.**

Keywords—optical transceivers, driver, equalizer, transimpedance amplifier, multiplexer

I. Introduction

High-speed communication standards are investigating the scaling from 800G to 1.6T to support ever increasing demands of data intensive applications such as cloud services, virtual reality, high-performance computing and 5G/6G. The emerging 800G Ethernet implementations can be regarded as a wider version of 400G Ethernet, i.e., the standard relies on the same 50 GBd PAM4 interconnects but doubles the amount of lanes from four to eight. A similar trend was observed in the initial 400G transceivers where first 8 lanes at 25 GBd were implemented before the lane rate was doubled towards 50 Gbps. Supporting 200 Gbps per lane is required to continue this trend by first enabling 4-lane 800G and in a next stage 8-lane 1.6T [1]. Progress on the maximum throughput per lane of a transceiver typically comes from technology evolutions combined with architectural innovation in system and integrated circuit (IC) design. These innovations comprise the invention and realization of new circuits and architectures, more efficient multiplexing or modulation schemes, digital signal processing, etc.

Recent transmitters in advanced CMOS and FinFET nodes [2], [3] provide extensive transmit-side FFE capabilities up to 64 GBd. Speed limitations in these technologies will make the transition to >100GBd a challenge. Alternatively, InP-based multiplexers [4] manage to reach >100Gbaud easily. InP also offers the possibility to create high-swing output drivers [5], necessary to efficiently drive optical modulators. However, InP solutions lack the ability to introduce more complex equalization of the signal. BiCMOS based transmitters enable the integration of more complex circuits with respect to InP technologies, are capable to deliver high signal swings required for optical drivers and promise increased bandwidth compared to CMOS and FinFET.

SiGe TIAs have been designed for very high bandwidth. For example, [6] realizes 92 GHz in a single stage but with limited gain. Reference [7] demonstrates a 65GHz bandwidth and 71 dBΩ shunt feedback TIA. This approach is however less scalable to higher frequencies as the transimpedance limit dictates that the open loop gain of the amplifier should increase with the square of the bandwidth. As such a shunt-feedback TIA also has a strong roll-off above its bandwidth.

The remainder of this paper will give an overview of recent SiGe transmitter and receiver circuits developed at Ghent University – imec. The next section will present 100 GBd capable drivers and signal generating circuits. Section III presents preliminary results on traveling-wave receiver circuits and section IV will formulate a conclusion.

II. 100 GBd Transmitter Circuits

Today, DSP and digital-to-analog converters (DACs) are intensively used to create waveforms and to apply transmit-side equalization or pulse shaping for example. When scaling to 100 GBd or higher, analog bandwidths in excess of 60 GHz are required. Such high bandwidths are very challenging to realize in CMOS DACs. For this reason, we have investigated different approaches to generate high baud-rate signals. We present an analog interleaver, followed by a compatible linear driver design. An alternative mixed-signal approach comprises a PAM-4 multiplexer and mixed signal feed forward equalization circuit.

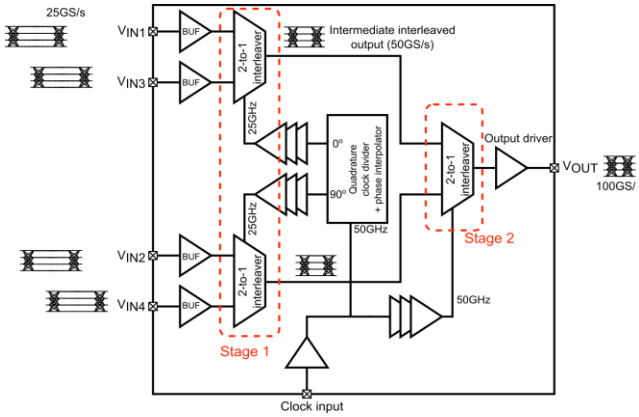

Fig. 1: Analog 4-to-1 interleaver

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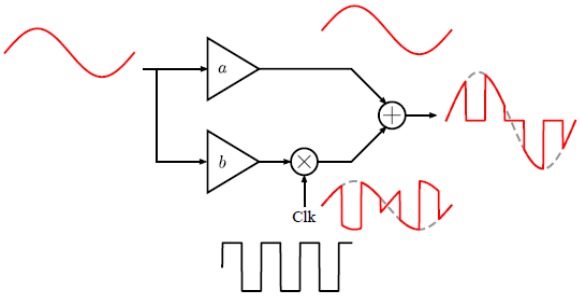

Fig. 3: Return-to-zero generation

A. *100 GBaud Analog Interleaver*

To overcome the bandwidth limitations of CMOS DACs, an analog interleaver can be employed to combine two or four sub-rate DAC outputs into a single 100GBd output [4], [8], [9], [10]. Such a circuit can be considered as a very fast selector or switch, taking samples one after the other from the different DACs. The analog interleaver architecture consists of three 2-to-1 sub-interleavers as shown in Fig. 1. The circuit requires a 50GHz clock for the final stage; the 25GHz clocks for the first stage are created on-chip using quadrature clock dividers.

Conventional high-speed current-mode logic (CML) implementations suffer from clock feedthrough. In the proposed topology, the interleaving is done in two steps. First, each of the incoming data streams is translated explicitly into (non-overlapping) return-to-zero (RZ) pulses by suppressing the signal during half the symbol period. The RZ generator is conceptually depicted in Fig. 3. The signal is split in two branches. A first branch only undergoes linear amplification while the second branch is also multiplied with a {-1, +1} clock signal. If the gain in both branches is equal, the output signal will be suppressed while the clock is negative and passed through the other part of the clock period. Two signals can be interleaved by generating RZ signals with complimentary clocks. As such, the zero periods will be interleaved. Summing the RZ signals yields the interleaved signal. In this way, the clock feedthrough in both RZ paths has opposite phases (as the RZ generators are driven by anti-phase clocks) and is cancelled in the summing node. Moreover, the explicit RZ generation (unlike conventional analog multiplexing) allows for pre- and de-emphasis as the signal suppression is realized by summing the incoming signal with the same signal multiplied by the clock. Introducing a programmable gain in both branches of the RZ generator gives a 1-tap feedforward equalizer. The response of the RZ generator is

$$a + b + (a - b)z^{-1}$$

More details on the concept and implementation can be found in [8], [9]. The die micrograph (55nm SiGe BiCMOS) is depicted in Fig. 2. The die size is around 2 mm^2 and the main high-speed interfaces and building blocks are indicated. The 100 GBd PAM-4 eye diagram was measured with a 70 GHz sampling oscilloscope. The interleaver can also be used to make arbitrary waveforms. The resulting effective number of bits (ENOB) is more than 4 bits up to 40 GHz. In these experiments,

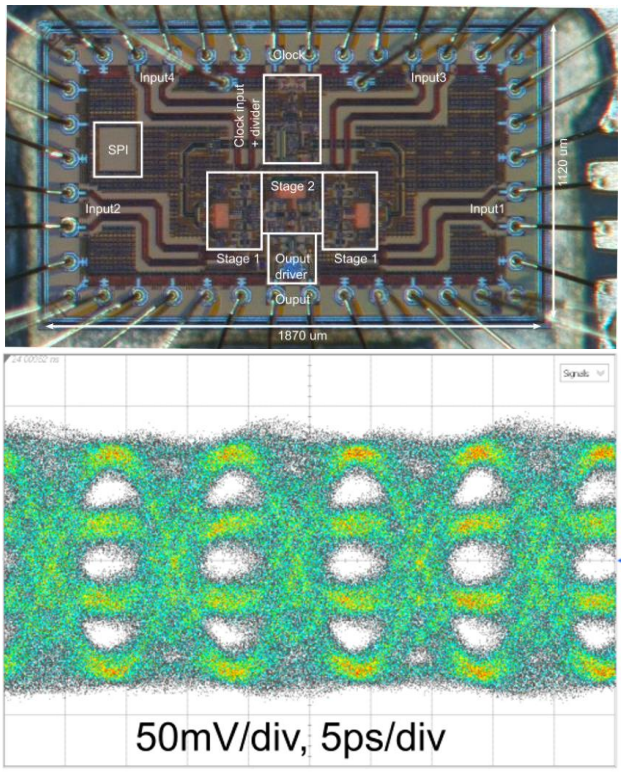

Fig. 2: Die micrograph and 100 GBd PAM-4 output

the chip was mounted in a cavity of a dedicated Megtron 6 test board and wire bonded directly to PCB transmission lines. 1.85 mm connectors were used at the output to connect with the remote sampling heads of the scope via very short cables. The equalizer embedded in the interleaver chip was configured to overcome the losses introduced by the bond wires, transmission lines, connectors and cables, yielding the wide-open eye diagram depicted in Fig. 2. The measured bandwidth is 73 GHz and 400 mVpp output swing is obtained, sufficient to act as predriver for a dedicated high-swing modulator driver. The power consumption is 700 mW in 4-to-1 mode.

B. *100 GBd Linear Modulator Driver*

Fig. 4 shows a quad-channel linear MZM driver [11] that has a bandwidth of around 68.7 GHz with a programmable gain of 8

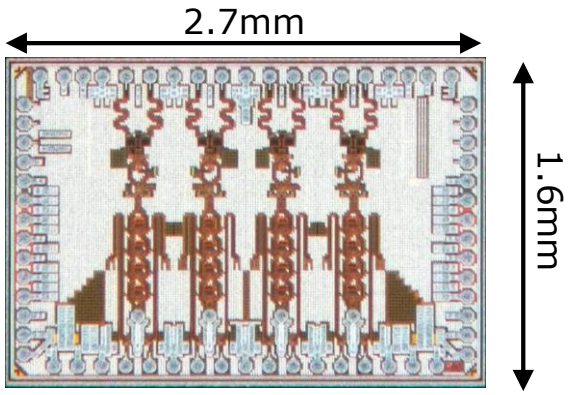

Fig. 4: 4-Channel Linear Broadband Modulator Driver

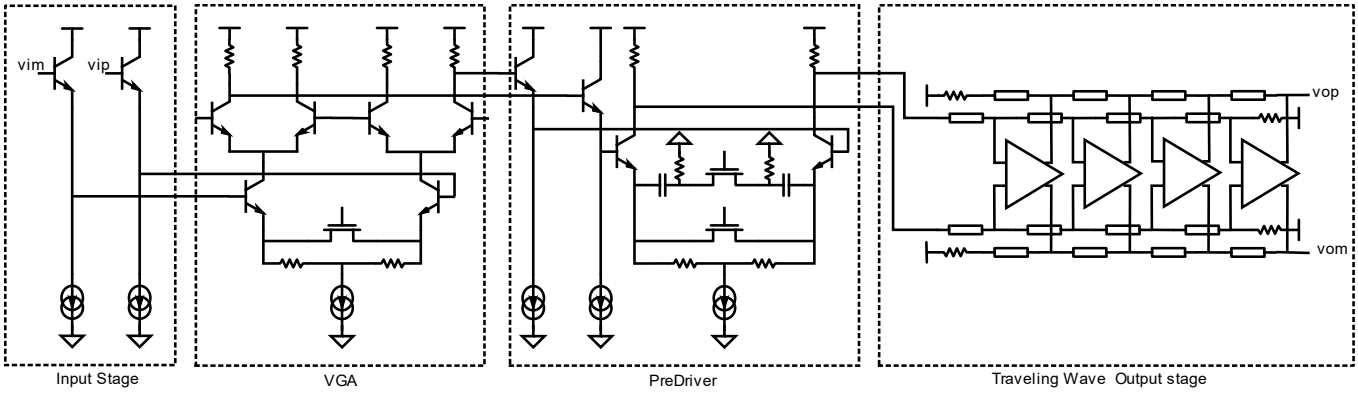

Fig. 5: Schematic of a single channel of the Linear broadband Modulator driver

to 21 dB. The amplifier offers a differential output swing of 4 Vpp with a THD of 3% at 1 GHz. High bandwidth, gain and linearity are realized using combination of lumped and traveling-wave amplifier stages as can be distinguished from the die micrograph and the schematic in Fig. 5. Traveling-wave designs have demonstrated very high bandwidth in InP drivers [12], but the SiGe implementation enables much more controllability, enabling a high gain tuning range without bandwidth degradation. The gain is separated over a lumped VGA and pre-driver stage with nominal gains of 5.3 and 4.1 dB followed by a traveling wave output stage with 12 dB of gain. The VGA gain is controlled using a Gilbert cell, and a mosfet in its linear region controls the peaking of the stage. The predriver has both emitter degeneration and peaking using switchable mosfets. The VGA and pre-driver have a 3V supply while the output stage is fed from a 4V supply. This to increase the energy efficiency. The differential small signal gain with swept gain settings are shown in Fig. 6. Fig. 7 shows clear 100 GBaud PAM4 eye diagrams measured at the output of the driver. The figure showcases a differential peak-to-peak output swing of 3.6V and a level separation mismatch ratio (RLM) of 0.975. The driver is ideal suited to amplify the interleaved signals from the AMUX presented in the previous paragraph. The MZM driver power consumption is around 725 mW per channel.

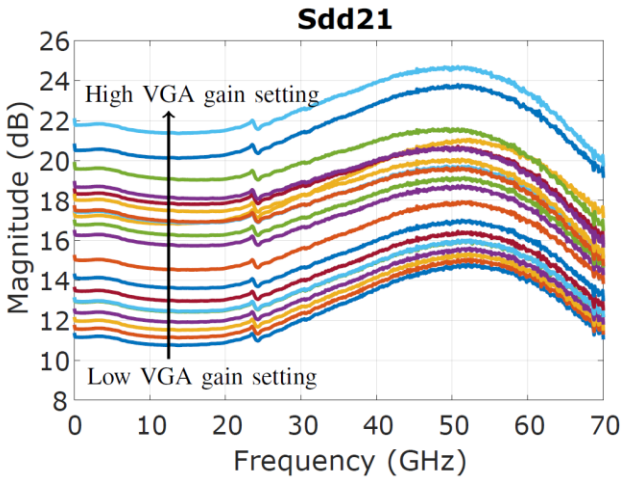

Fig. 6: MZM Driver differential gain measurements.

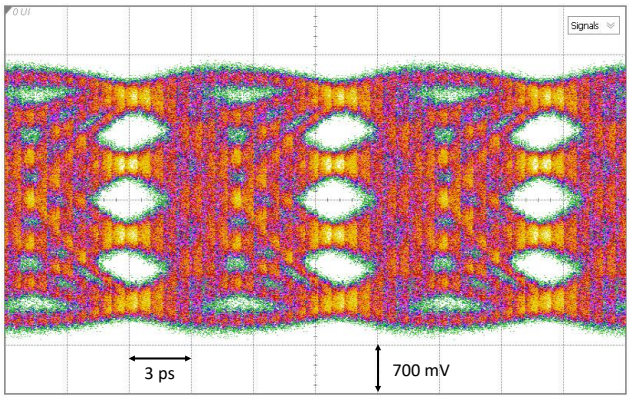

Fig. 7: 100 GBaud PAM4 eye diagrams at output of the MZM Driver

C. PAM-4 Multiplexer with 7-TAP FFE

Although the analog interleaver has some equalization functionality, this is still limited and pre-equalization of the interleaver input signals is required. This can be done digitally before the signals are generated with a DAC [13]. Alternatively, feed-forward equalization in the transmitter has been implemented with traveling-wave designs [14]. However, this typically leads to a large chip area. Transmission line segments are used to create the delay between the different gain segments of the FIR filter. Active delay solutions as demonstrated in [15] are power consuming. To overcome this, we proposed a mixed-signal FIR filter which we implemented in a full PAM-4 multiplexer[16].

The 120 Gbaud PAM-4 transmitter IC, shown in Fig. 10, receives 4 PAM-4 inputs of which it first decodes the data to remove any signal distortion in amplitude or phase. The resulting most and least significant bits (MSB, LSB) of the incoming PAM-4 signals are then retimed using two 90 degrees out of phase quarter-rate clocks (CLK/2 and CLK/2 90º), and the 4 MSB and 4 LSB signals are separately multiplexed and filtered using two independent 7-tap FFEs, one for the MSB and one for the LSB. The two quarter-rate clocks are derived from an externally supplied half-rate clock (CLK) which is divided on-chip. Using phase interpolators (PI), the phases of both quarter-rate clocks can be fine-tuned. The MSB and LSB signals are filtered separately and combined in the output stage to obtain a full-rate PAM-4 signal. An output driver amplifies

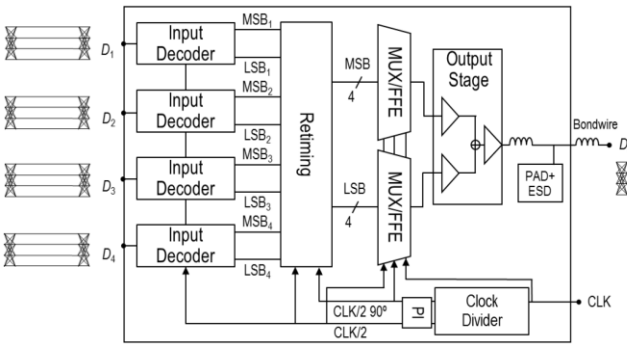

Fig. 10: PAM-4 multiplexer with 7-tap FFE.

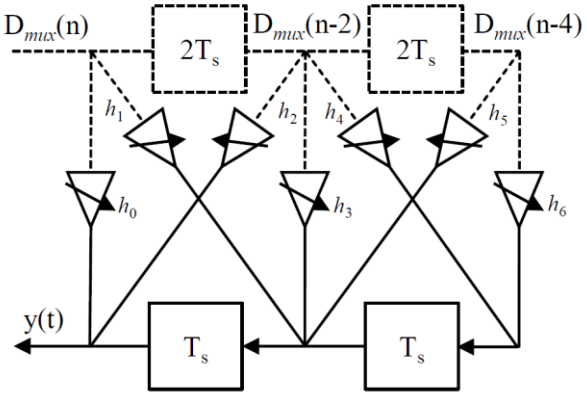

Fig. 11: Mixed-signal Equalizer

the PAM-4 signal to drive a 100Ω differential load. The four PAM-4 levels are created by scaling the overall gain in the two separate FFEs. The advantage of the FFE architecture, depicted in Fig. 11, is the efficient use of both digital and analog delay structures to obtain >100Gbaud operation with a large amount of filter taps in a compact configuration. The 7-taps filter contains a digital feedforward delay line which delays the signal with two unit intervals, and a feedback active analog delay line. The 7-taps filter only requires 2 active delay cells and the variable gain amplifiers are all driven with digital signals, reducing their linearity requirements. More details on the concept and implementation can be found in [16].

The die micrograph (55nm SiGe BiCMOS) is depicted in Fig. 8. The die size is around 3 mm^2 and the main high-speed interfaces and building blocks are indicated. The 100-120 Gbaud PAM-4 eye diagrams were measured with a 100 GHz sampling oscilloscope. In this experiment, the chip was flip-chip assembled directly on a dedicated Megtron 6 test board. Ardent TR70 connectors were used to provide the input data from a Keysight Arbitrary Waveform Generator whereas 1.85 mm connectors were used at the output to connect with the remote sampling heads of the scope via very short cables. The FFE equalizer was configured to overcome the losses introduced by the transmission lines, connectors and cable, yielding the open eye diagrams up to 120 Gbaud as shown in Fig. 9. A 0.5 Vpp output swing was obtained after a channel with a loss of 8 dB at 60 GHz. This is sufficient to act as predriver for a dedicated high-swing modulator driver. Without channel (or 0dB loss), the output swing could be up to 1.2Vpp.

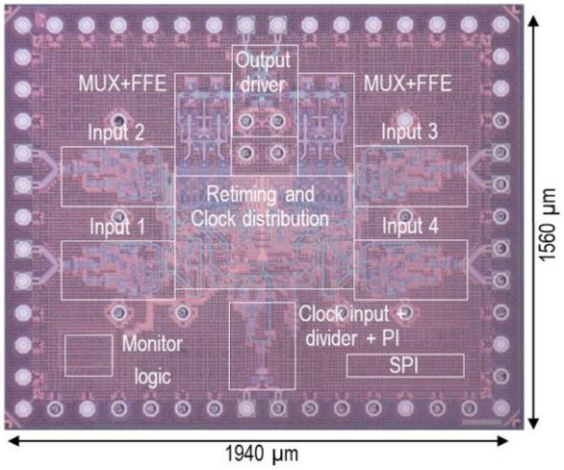

Fig. 8: Die micrograph of PAM-4 Multiplexer with 7-tap FIR

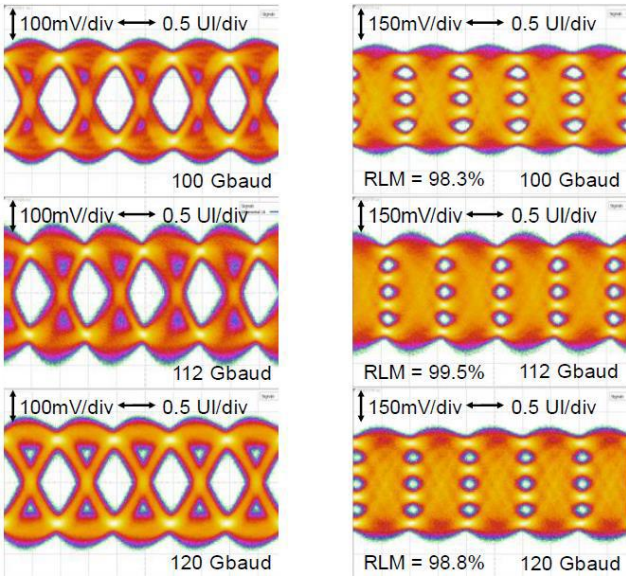

Fig. 9: NRZ/PAM-4 outputs at 100, 112 and 120 GBd.

The total power consumption is 2W when the input decoders are configured for NRZ and 2.16W when configured to decode PAM-4. From this power, approximately 680mW is consumed in the analog part (VGAs, delay circuits and output stage), 300mW in the MUX and retiming and 560mW for clock distribution.

III. 100 GBd Receiver Circuits

Fig. 12 shows a quad-channel TIA designed in 55nm SiGe BiCMOS. A single TIA consists of single-ended input traveling wave stage with 8 gain cells followed by two differential traveling wave gain stages that provide tunable gain and peaking. This signal is provided to a traveling wave output stage that was designed for a linear output swing of 650 mVpp with < 5% THD at 1 GHz. The gain stages and output stage each have 4 gain cells. Offset compensation around the gain cells realize single ended to differential conversion as can be seen in Fig. 13.

The electrical response of the TIA was evaluated by probing the die and measuring the s-parameters with a VNA which was calibrated till the probe tips. The derived transimpedance gain

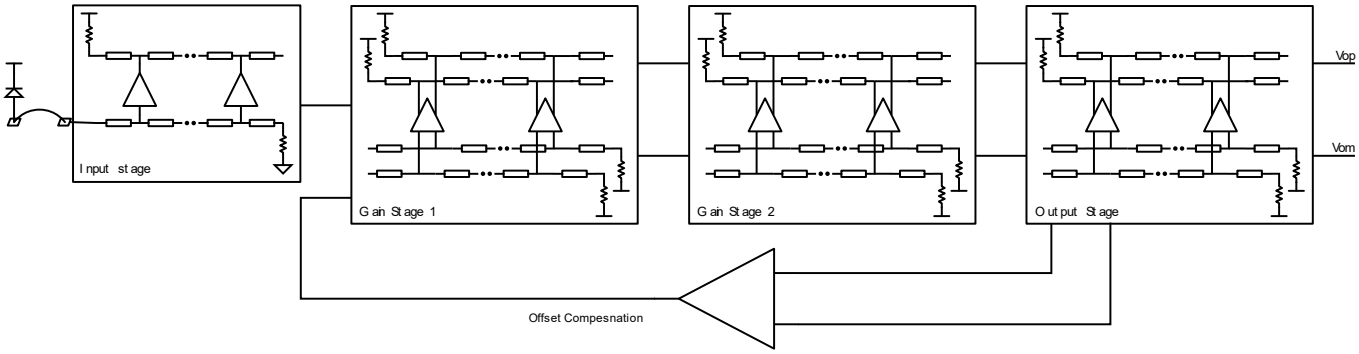

Fig. 13: Schematic of a single channel of the Linear broadband Modulator driver

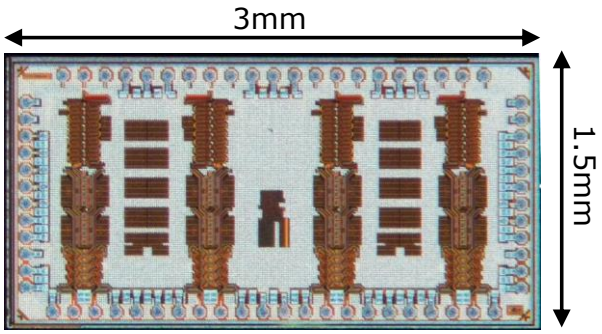

Fig. 12: Quad-channel 100 GBaud TIA

is shown in Fig. 14. The measurements show a gain of 76.8 dBΩ at 1 GHz and a 3 dB bandwidth of 62 GHz. The power consumption is around 500 mW per channel. With respect to modulator drivers, the bandwidth is reduced to trade off noise performance. Similar as for the driver design shown in II.B, high bandwidth is realized using a traveling wave design, performance metrics are compared to a shunt-feedback TIA [7], however, the traveling-wave design shows a much smoother roll-off enabling higher baudrate operation with proper equalization.

To demonstrate the performance, the TIA was wirebonded with a silicon photonic integrated circuit fabricated in imec's iSIPP50G platform containing a grating coupler and germanium photodiode. Recorded eye diagrams of a 100 GBaud PAM4 signal are shown in Fig. 15. Fig. 15(a) shows the output of a XPDV3120R photodiode used as reference receiver. This signal is measured with an input optical power of 9 dBm with 8.1 dBm optical modulation amplitude, the received signal shows a BER of 2E-8. Fig. 15(b) shows the signal at the output of the TIA. For this, the optical input power was first reduced to 0 dBm. The eyes are clearly closed, however after applying a 5 tap feedforward equalizer, the eyes in Fig. 15(c) are obtained, improving the BER from 2E-2 to 8E-5. The RLM degraded from 0.979 for the reference receiver to 0.931.

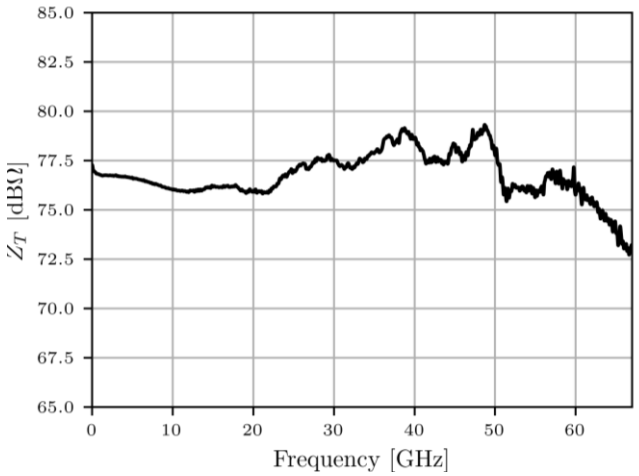

Fig. 14: Measured electrical frequency response of the TIA

IV. Conclusion

In this paper we present different SiGe BiCMOS circuits targeting 100 GBaud per wavelength optical communication links. SiGe offers very high-speed bipolar transistors ideal for the data path of these high-speed circuits combined with performant MOSFETs used for control and tunability. This enables implementation of complex circuitry such as the presented analog multiplexer and PAM-4 multiplexer with built-in mixed signal FFE. Four channel implementations of modulator drivers and receiver circuits have been shown completing the required circuits for 800 GbE high speed links.

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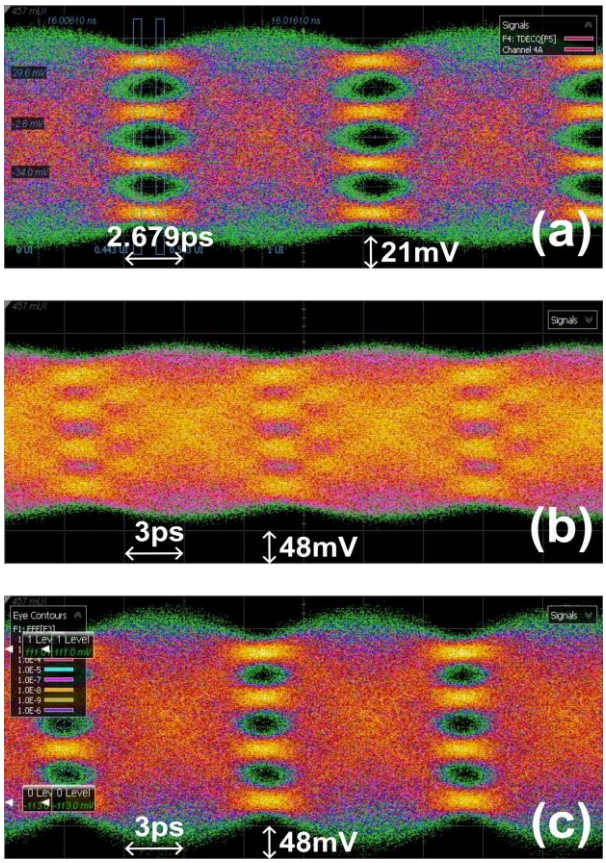

Fig. 15: Measured 100 GBaud PAM 4 eye diagrams of (a) reference receiver with 9dBm optical input power, (b) at the output of the TIA with reduced optical input power (0dBm) and (c) after applying a 5-tap equalizer on the TIA output signal.

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