A Linear Modulator Driver With Over 70-GHz Bandwidth 21.8-dB Gain and 3.4-Vppd Output Swing for Beyond 120-GBd Optical Links

Shengpu Niu, Riaz Ahmed, Joris Lambrecht, *Member, IEEE*, Jakob Declercq, Marijn Verbeke, *Member, IEEE*, Michiel Verplaetse, *Member, IEEE*, Bart Moeneclaey, *Member, IEEE*, Cheng Wang, Joris Van Kerrebrouck, Nishant Singh, Johan Bauwelinck, *Senior Member, IEEE*, and Xin Yin, *Senior Member, IEEE*

***Abstract*— This article investigates a linear differential modulator driver for optical communication links beyond 120 GBd. The driver was implemented in a 55-nm SiGe BiCMOS technology with an f_T/f_{MAX} of 330/370 GHz, featuring a traveling wave output stage driven by a lumped variable gain amplifier (VGA) and a predriver. The fabricated IC achieved a maximum low-frequency gain of 21.8 dB with more than 10-dB gain control capability and a 3-dB bandwidth of over 70 GHz. Power measurement results show the driver is able to deliver a constant output swing of 3.56 Vppd while keeping the THD below 2%, with the differential input swing varying from 0.3 to 1.03 Vppd at 1 GHz. In the large-signal measurement, the chip delivered 72, 106, 112, and 128 GBd pulse amplitude modulation-4 (PAM-4) signals with differential output swings of 4, 3.59, 3.434, and 3.425 Vppd, respectively. The chip's total power consumption is 725 mW, resulting in a power efficiency of 2.83 pJ/bit. Overall, this is the first time an optical modulator driver reported the ability to accommodate such a wide input swing and demonstrated the operation at a data rate of 256 Gb/s. These features make it a desired candidate for beyond 120-GBd optical links.**

***Index Terms*— Modulator driver, pulse amplitude modulation-4 (PAM-4), SiGe BiCMOS, traveling wave.**

I. Introduction

THE increasing demand for data-intensive applications such as cloud services, artificial intelligence training, virtual reality, high-performance computing, and 5G/6G has been driving the development of new technologies and integrated circuits for faster optical transceivers. Nowadays, the typical high-baud rate optical transmitters rely on digital signal processing (DSP), a digital-to-analog conversion (DAC), a modulator driver, and an optical I/Q modulator [1], [2], [3]. The next-generation (coherent) transmitters use dual-polarization, I/Q modulation, and pulse amplitude modulation (PAM) techniques to boost the overall transmitting data rate to exceed 800 Gb/s [1], [2]. This requires the integrated RF components to feature a wide bandwidth and a low THD.

In typical (coherent) transmitters, the output of the CMOS DAC is usually incapable of driving a high-speed Mach–Zehnder modulator (MZM) directly because the DAC output swing is lower than the required V_π of the MZM [4], [5], which could be around 5 V. In modern MZM designs, designers have to trade off modulation efficiency and bandwidth performance, targeting high-speed data transmission [6], [7]. Therefore, a broadband driver with a sufficiently high drive swing is essential for the MZM to achieve good electro-optical modulation efficiency without sacrificing too much bandwidth performance.

The output swing of modulator drivers in CMOS is usually below 3 Vppd [2], [8], [9] as it is limited by the device breakdown voltage, which is technology-dependent. In recent years, drivers designed in technologies such as SiGe BiCMOS [10], [11], [12], [13], [14], [15], and InP DHBT [16], [17], [18] have been investigated because they have a collector-to-emitter breakdown voltage BV_{CEO} over 1.5 V and f_T/f_{MAX} above 300 GHz. Those drivers achieve excellent performances: a low-frequency gain of more than 20 dB [2], [10], [13], a 3-dB bandwidth of over 67 GHz [10], [12], [13], [14], [18], and an output swing of beyond 4 Vppd [10], [11], [15] with a data rate of more than 90 Gb/s.

The drivers designed in the lumped architecture can achieve high gain and large output swing. However, a tradeoff exists between a driver's output swing and bandwidth. To avoid too much bandwidth degradation, some techniques have been exploited, for example, a peaking of over 5 dB [11], [13], using an open-collector output stage [2], [11], [13] and removing electrostatic discharging (ESD) diodes in the high-speed path. However, those techniques have obvious drawbacks, such as excess peaking leading to a large amount of group delay variation, open collector topology implying high sensitivity

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Shengpu Niu, Joris Lambrecht, Jakob Declercq, Marijn Verbeke, Bart Moeneclaey, Cheng Wang, Joris Van Kerrebrouck, Nishant Singh, Johan Bauwelinck, and Xin Yin are with the IDLab Design Group, Department of Information Technology, Ghent University—imec, 9052 Ghent, Belgium (e-mail: Shengpu.Niu@UGent.be; Xin.Yin@UGent.be).

Riaz Ahmed was with the IDLab Design Group, Department of Information Technology, Ghent University—imec, 9052 Ghent, Belgium. He is now with the Bayawever Technologies BV, 9000 Ghent, Belgium.

Michiel Verplaetse was with the IDLab Design Group, Department of Information Technology, Ghent University—imec, 9052 Ghent, Belgium. He is now with Nokia Bell Labs, 2018 Antwerp, Belgium.

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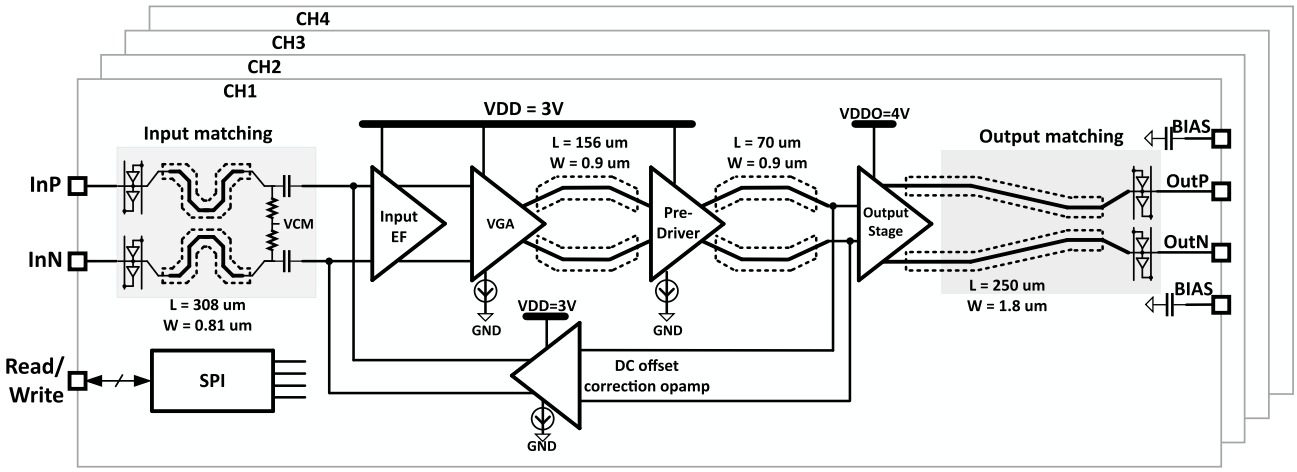

Fig. 1. Diagram of the proposed driver.

to assembly parasitics, and no ESD cells, meaning poor ESD protection. An attractive topology capable of acquiring high gain and high bandwidth is the traveling wave amplifier (TWA) architecture [14], [15], [19], [20], [21], [22]. But the full TWA drivers [10], [14], [15] consume a large amount of power to obtain a high gain and a large output swing as their output load impedance is usually limited to 50 Ω. To better balance the gain and bandwidth while minimizing the total power consumption, a traveling wave output stage driven by a lumped variable gain amplifier (VGA) and a predriver approach is proposed in this article, in which only the high-gain output stage is a TWA, but all the preceding structures, VGA and predriver, are lumped. Hence, the total gain is accumulated like a lumped structure but avoids too much bandwidth deterioration.

A driver must have good linearity to support a high-order amplitude modulation format. The traditional drivers achieved good linearity but worsened rapidly if the input power exceeded a certain point [10], [11], [12], [13], [14], [15], [16], [17], [18]. The input power was limited to a small range in those drivers to keep good linearity and deliver the targeted output power. The applicable scenarios will be widely extended if the driver can keep good linearity when delivering a constant output power, even if its input power varies widely. However, this has not been investigated enough in the previously published works. This chip exploited the gain control capability of the VGA to use it to linearly amplify or attenuate the input signal according to the input power level to always bring the input signal power to a preferred linear input range of the next gain stage. Therefore, the final output remains constant with good linearity within a wide input power range.

This article investigates a linear differential modulator driver for optical communication links beyond 120 GBd. The main purpose of this article is to demonstrate a broadband linear driver implementation. The remainder of this article is organized as follows: the circuit design and implementation are discussed in Section II. Section III discusses the measurement results. Finally, Section IV concludes this article.

II. Circuit Design

The chip targets to achieve a low-frequency gain of 10–20 dB, a 3-dB bandwidth of over 70 GHz, and an output swing beyond 3 Vppd, with THD below 2%, while accommodating an input swing of 0.3–1 Vppd. Fig. 1 illustrates the architecture of the proposed driver. The data path consists of an input matching network, an input buffer, a VGA, a predriver, a traveling wave output stage, and an output matching network. The IC was designed and fabricated in a commercial 55-nm SiGe BiCMOS technology with an f_T/f_{MAX} of 330/370 GHz and a core device collector–emitter and collector–base breakdown voltages, BV_{CEO}/BV_{CBO}, of 1.5/5.4 V, respectively.

At the circuit level, the VGA and predriver were designed to have a maximum nominal low-frequency gain of 5.3 and 4.1 dB with more than 10-dB gain control capability. The output stage has a fixed gain of 12 dB. The 3-dB bandwidth of each stage was optimized to achieve an overall chip bandwidth of over 70 GHz. The VGA, predriver, and output stages' output swings were targeted at 0.56, 0.89, and 3.56 Vppd with the corresponding THD lower than 1%, 1.5%, and 2%, respectively. To prevent degradation of the chip's linearity caused by offset, a dc offset compensation and a common-mode control loop were implemented. It senses the dc offset at the inputs of the output stage, amplifies the difference, and adjusts the inputs of the input buffer. The common-mode voltage of the input buffer inputs is biased to 2.4 V by the common-mode control loop to counter the process, voltage, and temperature variations. To reduce the total power consumption, only the output stage differential amplifiers are powered by a 4-V supply, whereas a 3-V supply powers the input buffer, VGA, predriver, and the output stage gain cell input emitter followers. A serial peripheral interface (SPI) was designed to control each stage's gain, peaking, and biasing using the digital programmable settings.

A. Input and Output Matching Network

The input and output matching networks were designed to minimize the interface reflections for a wide frequency band. In modern broadband circuit design, the parasitic capacitance

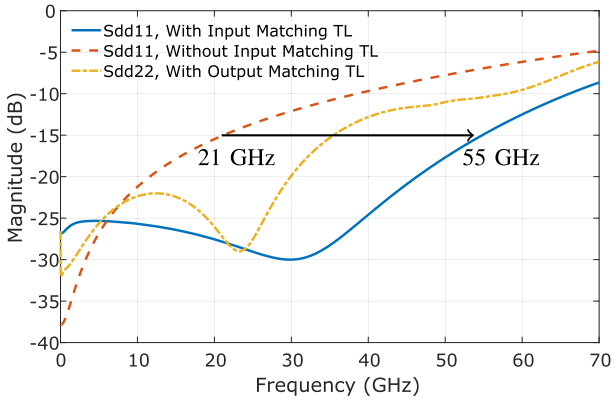

Fig. 2. Simulated reflections of input and output matching networks, Sdd11 and Sdd22.

originating from the I/O ESD cells and bondpads can be one of the limitations of the achievable bandwidth. The microstrip transmission lines (TLs) in the input matching network, as shown in Fig. 1, were implemented using a thick metal with a width of 0.81 μm and a length of 308 μm to absorb the parasitic of ESD diodes and bondpads, avoiding too much signal loss at high frequencies. The equivalent parasitic capacitances of the ESDs and the bondpads are 12 and 30 fF, respectively. Fig. 2 illustrates the simulated chip input and output return loss, Sdd11 and Sdd22. It shows that Sdd11 exceeds -15 dB for frequencies over 21 GHz if there is no input matching TL. In contrast, Sdd11 is improved to stay below -15 dB with frequencies up to 55 GHz by placing an input TL in the input matching network. In the output matching network, an output TL with a length of 250 μm and a width of 1.8 μm was implemented for a similar reason. The Sdd22 stays below -10 dB for frequencies up to 58 GHz, as shown in Fig. 2.

B. Variable Gain Amplifier

To control the gain of the driver, a VGA is used to attenuate or amplify the signal from input to prevent underdriving or saturating the next stage. An amplifier with tunable degeneration resistors implemented by MOS transistors is often used to realize such functionality. It is simple and power-efficient. However, changing the degeneration resistors also leads to the changes in zeros or poles in the circuit frequency response, resulting in a variable peaking. This is undesired in some cases, as too much peaking results in a large group delay distortion. Furthermore, the resolution of the tunable gain in this solution is limited by the MOS transistor layout footprint. A Gilbert cell topology VGA is another good candidate to provide such variable gain attenuation. A wide linear tunable range with fine steps can be obtained by controlling the ratio of signal current conducted to the signal path or the dummy branch in this topology. More importantly, it provides a more stable peaking in the frequency response. However, it is less power-efficient and more complicated to implement. In this article, we chose a Gilbert cell VGA with variable degeneration resistors to balance the gain tunable range, design complexity, power consumption, and peaking variation. The tunable degeneration resistors and the Gilbert cell control this solution's coarse and fine gain steps, respectively.

Fig. 3 shows the schematic with the core devices' size of the proposed VGA, which succeeds the input buffer. The proposed VGA provided a linear tunable gain from -5 to 5.3 dB by tuning the bias voltages vcasc_m and vcasc_p and switching the gate voltage V_G<3:0> of the shunt MOS resistors $N1$<3:0> as shown in Figs. 4 and 5. Fig. 4 also shows the simulated THD and VGA gain where the VGA output swing was forced at 0.56 Vppd with the input swing swept from 0.31 to 1 Vppd at 1 GHz. To keep a constant output, the configured VGA gain decreases with its input swing increasing. However, the THD exceeded 1% at an input swing of 1 Vppd. This is because the VGA gain, in this case, is -5 dB, which is already close to the lower limit of the linear tunable range. The simulated frequency responses of the dc block, input buffer, and VGA combined together using the same gain settings in Fig. 4 are shown in Fig. 5. The 3-dB bandwidths are all over 100 GHz, and their corresponding peaking range is from 0.4 to 1.7 dB within the frequencies below 100 GHz. A 50-pH inductor L_1 was implemented to introduce a 1.2-dB peaking at 40 GHz to compensate for the loss of the predriver at the same frequency as illustrated in Fig. 6. The power consumption of the VGA is 37.8 mW from a 3-V supply.

C. Predriver

The predriver is a lumped differential amplifier with an output impedance of 50 Ω driving the output stage's 50-Ω input impedance. It was designed with a 3-dB bandwidth of over 70 GHz and a nominal low-frequency gain of 4 dB to further bring the signal swing from the previous 0.56–0.89 Vppd with THD lower than 1.5%. Finally, the predriver was implemented as a differential amplifier driven by emitter followers, as illustrated in Fig. 3. Considering the equivalent loading is only 25 Ω, the impedance of the degeneration resistor R_{e2} was chosen to be 11 Ω and the tail current was 26.7 mA to simultaneously meet the targeted 4-dB low-frequency gain and linearity requirement. To be able to control better the output swing, linearity, and peaking, the predriver was designed with a 2-bit variable gain control capability and a 1-bit peaking functionality, controlled by the MOS gate voltages V_{GR}<1:0> and V_{GC}, respectively. A large-sized resistor R_3 is connected between C_{e1} inner plate and ground to avoid an arbitrary dc voltage on this inner plate. A 30-pH inductor L_3 is used to boost the bandwidth further. The simulated predriver transfer functions with different gain and peaking configurations are illustrated in Fig. 6. It shows that the predriver has a bandwidth of 77 GHz and a peaking of 0.8 dB at a configuration where the gain setting is high, and the peaking functionality is enabled. The power consumption of the predriver is 108.6 mW from a 3-V supply.

D. Traveling Wave Output Stage

The output stage amplifies the incoming signal to the final output with a swing of 3.56 V with a THD lower than 2%. This requires the output stage to have a nominal gain of

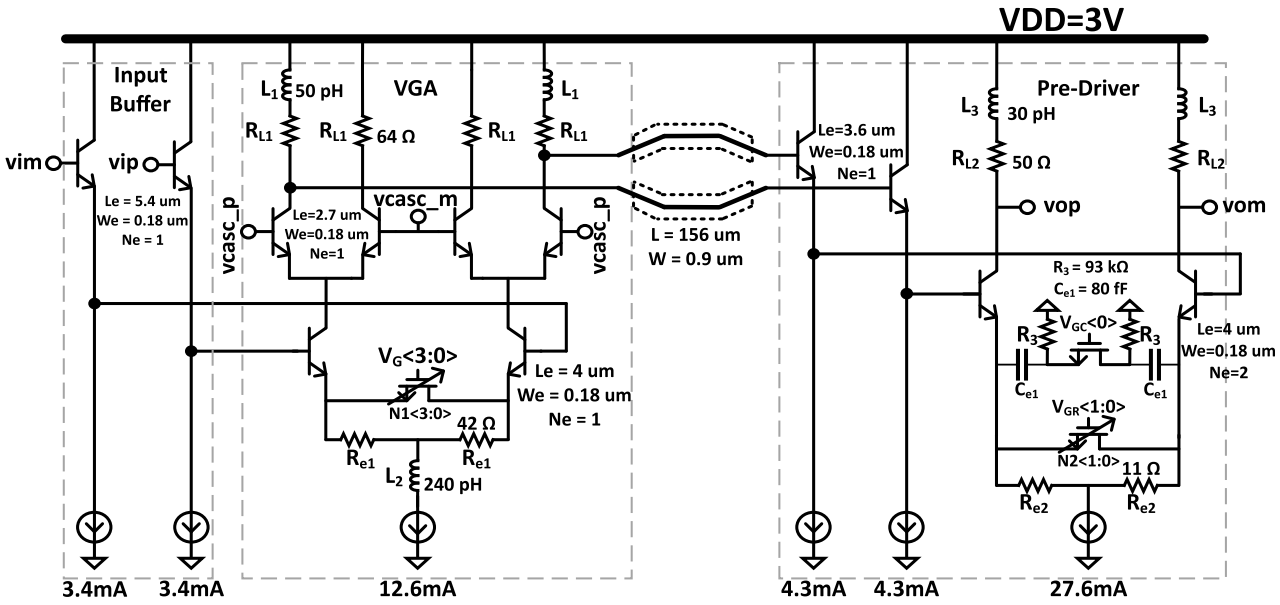

Fig. 3. Input buffer, VGA, and predriver schematic. For bipolar, *Le*, and *We* are the emitter length and width, respectively. *Ne* represents the number of emitters.

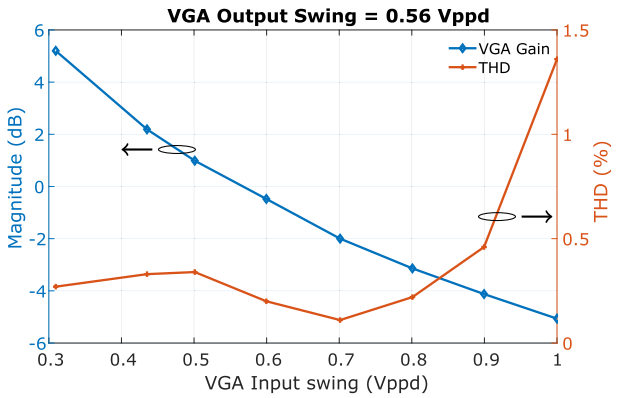

Fig. 4. Simulated VGA gain and THD at an output swing of 560 mV.

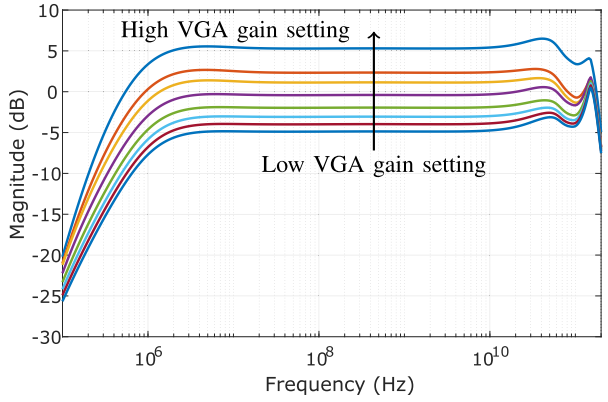

Fig. 5. Postlayout simulated transfer functions of dc block, input buffer, and VGA combined with different VGA gain settings.

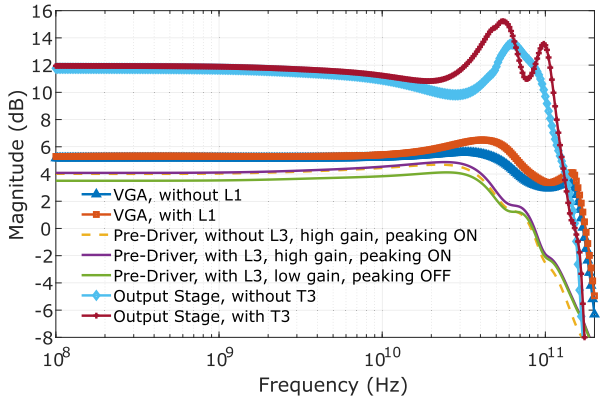

Fig. 6. Postlayout simulated VGA, predriver, and output stage transfer functions with and without bandwidth-boosting techniques.

12 dB. However, high gain is the largest contributor to low electrical bandwidth. The TWA topology is a good candidate for a high gain and bandwidth. The fundamental idea is to split the high-gain stage into smaller sized low-gain units and distribute the input and output parasitic capacitors along with the TLs [19], [20], [21], [22]. In this way, the total gain and the output swing add up with the number of gain cells without sacrificing bandwidth, which is now mainly determined by the TLs' frequency response [14].

The schematic of the output stage is shown in Fig. 7(a). It has four identical cascode gain cells connected by the input and output TL sections. T_1 and T_2 are normal TWA TLs with a characteristic impedance of approximately 50 Ω over a wide frequency band. The output stage was implemented with a peaking of 3 dB at 55 GHz to compensate for the loss of the predriver, which is 2 dB at 55 GHz, as shown in Fig. 6. The peaking is obtained by introducing an extra narrow width TL section T_3. In addition, T_3 was optimized while considering the parasitics originating from the wide, high-current resistor R_{L4} layout to avoid bandwidth degradation. T_3 helps boost the output stage gain within frequencies from 20 to 65 GHz, as shown in Fig. 6.

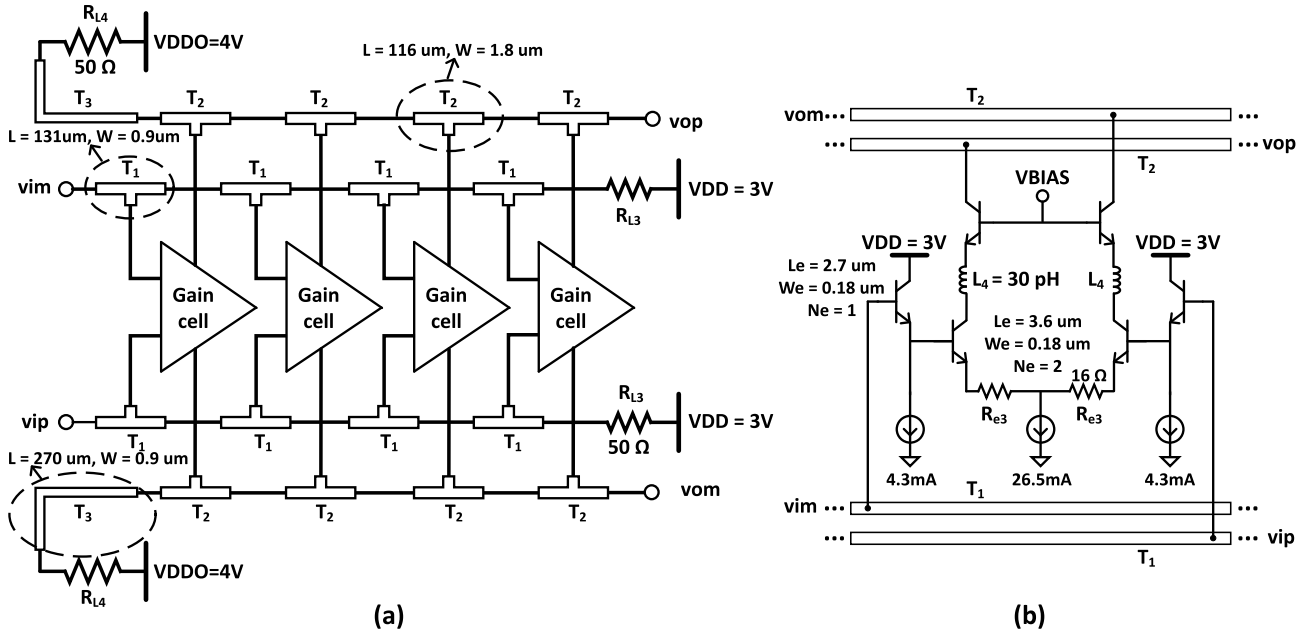

Fig. 7. (a) Block diagram of the four-stage traveling wave output driver. (b) Schematic of a single gain cell.

The single gain cell schematic is shown in Fig. 7(b). A pair of input buffers drive the large-sized transistors in the differential pair. The use of input buffers is essential to reduce the capacitance seen from the input TL. The interconnection inductor L_4 in the gain cells introduces inductive peaking at frequencies from 30 to 70 GHz, boosting the bandwidth further. To guarantee enough headroom for an output swing of 4 Vppd without increasing the total power consumption, the output dc voltage was designed to be biased at 4 V with an external RF bias tee. The voltage of VBIAS was set to 3 V, and this can avoid the cascode transistors entering the saturation region for a single-end output peak-to-peak voltage swing of 2 V. The internal loading resistors R_{L3} and R_{L4} are both 50 Ω. To ensure a 4-Vppd output swing with 25-Ω equivalent loading, the tail current of one gain cell is 26.5 mA, resulting in a total current of 106 mA. To set the output stage in the linear range with an input swing of 0.89 Vppd, the resistance of the degeneration resistor of R_{e3} was chosen as 16 Ω. The simulated transfer function of the output stage in Fig. 6 exhibits a gain of 11.8 dB at 1 GHz and a 3-dB bandwidth of over 100 GHz.

A 156-μm-long, 0.9-μm-wide TL connects the VGA and the predriver to minimize signal loss and avoid excess peaking. Similarly, the predriver and output stage are connected by a 70-μm-long and 0.9-μm-wide TL. The power consumption of the output stage is 527.2 mW.

III. Measurement Results

Fig. 8 shows the die micrograph and indicates the main blocks. The die measures 2.51 × 1.7 mm and includes four identical channels to drive four MZMs. Only one channel was measured because only one GSSG probe can be placed on each side. The chip's low-speed SPI and dc pads were wire-bonded to a printed circuit board (PCB). The driver outputs were biased at 4 V through the external RF bias tees during all the measurements. The power consumption of the measured channel in all the measurements presented below is 725 mW.

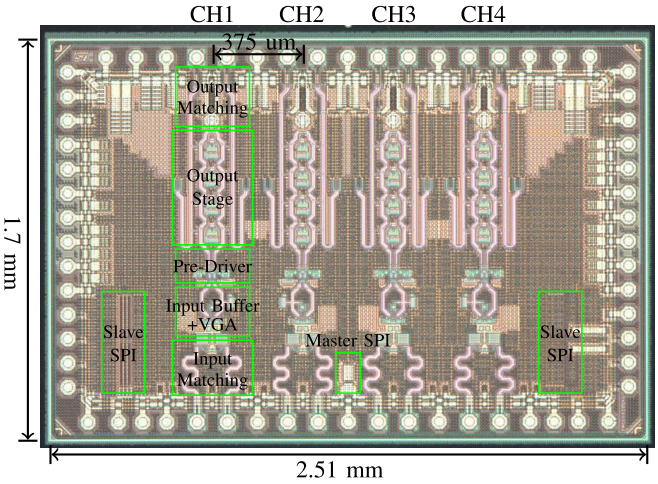

Fig. 8. Driver die photograph.

A. S-Parameter Measurements

The presented S-parameter and power measurements were conducted using an N5247B PNA-X. The S-parameter was characterized from 10 MHz to 70 GHz. Multiple S-parameter curves were obtained by tuning the VGA and predriver gain settings. As shown in Fig. 9, the differential input and output reflections, Sdd11 and Sdd22, are below −7 and −8 dB up to 70 GHz, respectively. The simulated Sdd11 and Sdd22 are presented and compared with their measured counterparts in the same figure, showing that the measured results matched well with the simulated ones.

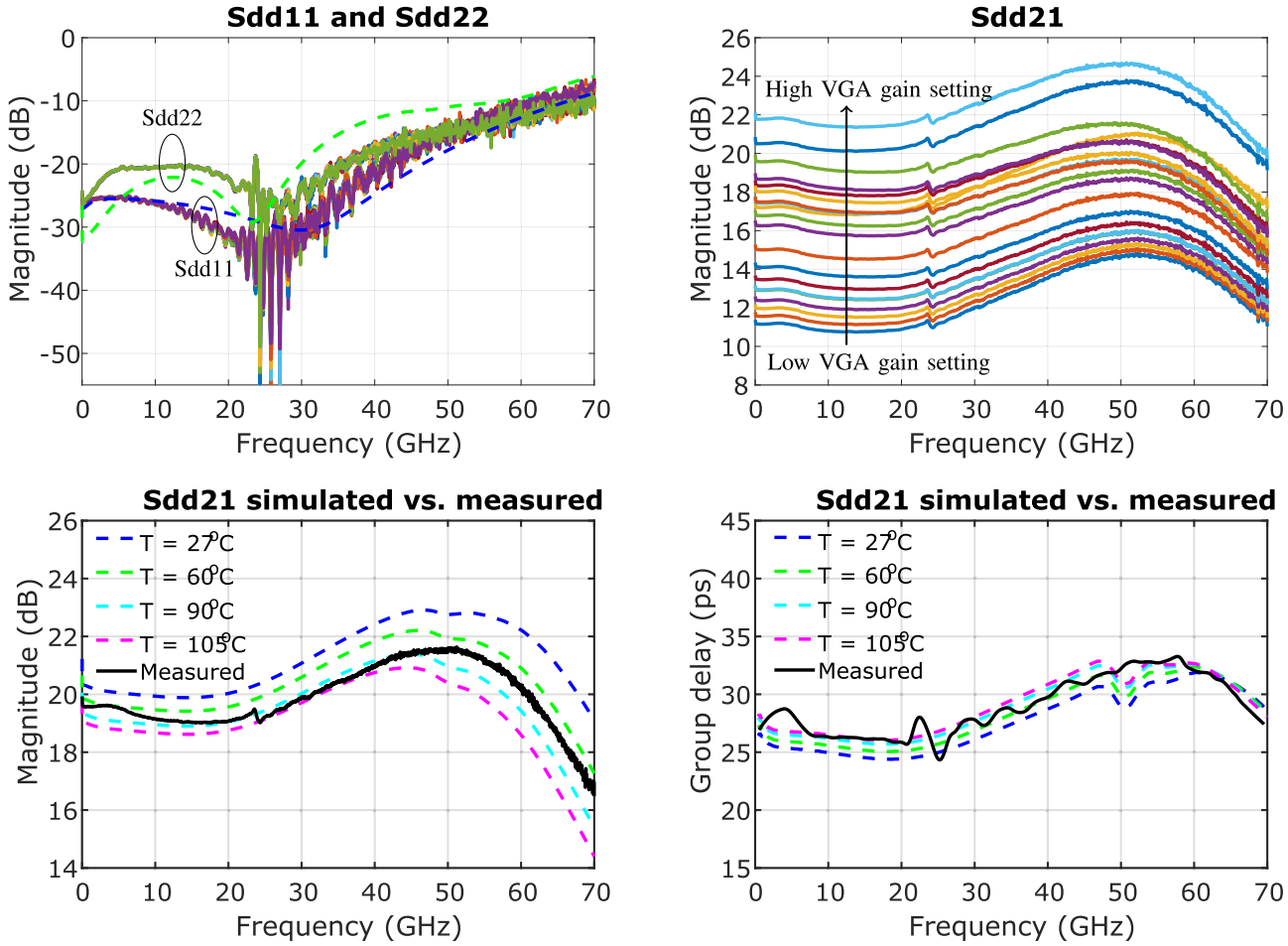

Fig. 9. Measured differential *S*-parameter results and a comparison between postlayout simulations (dashed) and measurement (solid).

The differential small-signal gain Sdd21 was presented in the upper right figure in Fig. 9. The low-frequency gain ranges from 11.2 to 21.8 dB, all with 3-dB bandwidths above 70 GHz. The Sdd21 peaks at a frequency of around 50 GHz, with the peaking value changing from 2.6 to 4.1 dB in the Sdd21 curves. This peaking can be used to compensate for the loss from MZM and the electro-optical packaging when transmitting 100-GBd data. There is a small disturbance of Sdd21 at around 24 GHz caused by the setup calibration. It had been observed with around plus 0.1-dB gain deviation from 0 dB at the same frequency when the probes were landed on a differential TL with a delay of 2 ps to check the measurement reference plane after calibration. This phenomenon also distorted the group delay of the measured Sdd21, as shown in Fig. 9 bottom right.

The third curve from the top of the measured Sdd21 in Fig. 9 top right is compared with its postlayout simulated counterpart. The measured Sdd21 magnitude matches well with the simulated results at a temperature of 90°. Apart from the abnormal rise and fall at 24 GHz, the measured Sdd21 group delay has a variety of less than 9 ps, echoing the simulation results.

B. Power Measurement

The power measurement used the same setup and chip settings as the *S*-parameter measurement. The top left figure in Fig. 10 depicts the measured differential output power at 1 GHz. The measured THD at 1 and 10 GHz and the simulated THD at 3, 5, and 20 GHz, regarding the differential input and output swings, are presented in the top right and bottom left figures in Fig. 10. The bottom right figure in Fig. 10 summarizes the THD performance and shows the driver is able to deliver a constant differential output swing of 3.56 Vppd but keeps the THD below 2% and 5% at 1 and 10 GHz, respectively, with the differential input swing changing from 0.3 to 1.1 Vppd. The corresponding power gain ranges from 11.2 to 21.6 dB and matches well with the measured small-signal gain at 1 GHz depicted in Fig. 9. The differential output swing at Pout 1-dB compression point (DOP1dB) at 1 GHz varies from 4.75 to 5.15 Vppd (DOP1dB equals 14.5–15.2 dBm) with a corresponding differential input swing from 0.47 to 1.47 Vppd. The simulated THD with the same 3.56-Vppd output swing regarding the input swing at 1 and 10 GHz is compared in the bottom right figure in Fig. 10.

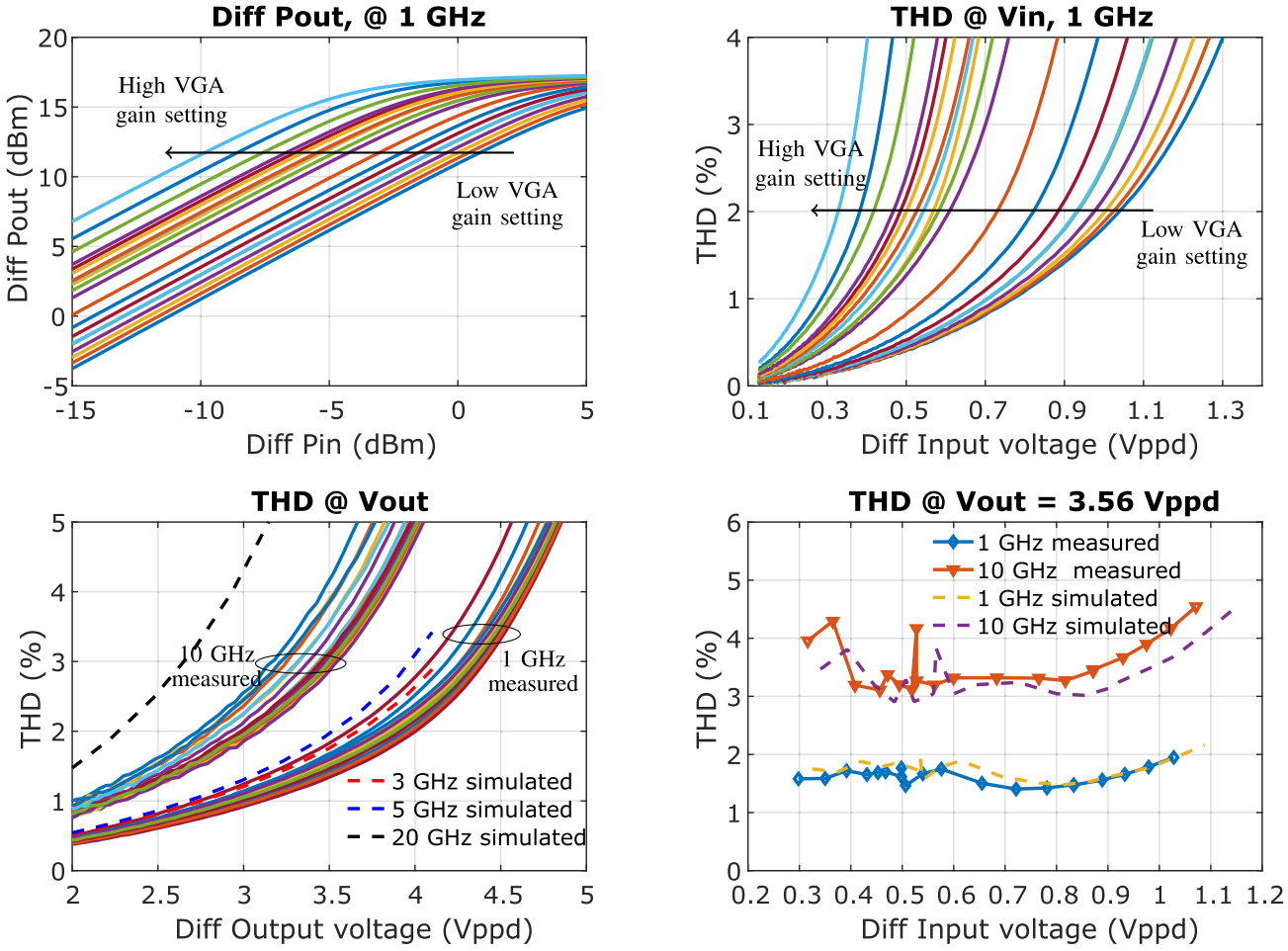

Fig. 10. Measured (solid) and postlayout simulated (dashed) THD and output power (Pout) with differential input and differential output. The simulated THD at 3, 5, and 20 GHz was with the chip configured at the highest gain setting.

The chip can be used to drive a single-ended (SE) modulator. Fig. 11 analyzes the THD with differential input and SE output. Similar to the differential output case, when delivering a constant SE output of 1.75 V, the THD stays below 2% and 5% at 1 and 10 GHz, respectively. The THD is always dominated by the third harmonic in both differential and SE outputs, as shown in the bottom right figure in Fig. 11.

C. Large-Signal Measurement

The large-signal measurements were conducted to mimic a realistic use case. The measurement setup and the measured results are shown in Figs. 12–14. A PRBS-15 input was generated with a 256-GS/s, 70-GHz bandwidth, arbitrary waveform generator (AWG) and applied to the input of the driver through RF cables and probe. One dc to 67 GHz, 10-dB attenuator was placed between the chip output and the sampling head input in each data out branch to avoid saturating the sampling heads. The remote sampling heads have a bandwidth of 75 GHz and a maximum differential tracking swing of 1.6 Vppd. Finally, the eye diagrams were captured by the oscilloscope. The losses from the AWG source, cables, and probes versus frequencies were calibrated using AWG IQ tools before chip measurement. Eye diagrams on the top left of Figs. 12 and 14 are two kinds of reference eyes called back-to-back (B2B) and Thru measurements. Those reference eyes were used to examine the eye quality that can be applied to the chip. In the B2B measurement, the AWG was connected to the sampling scope using the same setup, only without probes. In contrast, in the Thru measurement, the two RF probes landed on a differential TL with a delay of 2 ps. From Fig. 14, it can be clearly observed that the RF probes deteriorated PAM-4 eye qualities applied to the chip. Taking the 106-GBd PAM-4 eye diagram as an example, the B2B case measured a peak-to-peak of 82.45 mV, but the Thru measurement only measured a peak-to-peak of 60 mV with a relatively closed eye.

Figs. 12 and 14 show the measured driver differential output non-return to zero (NRZ) and PAM-4 eye diagrams without postprocessing. The setting with a low-frequency gain of 19.5 dB at 1 GHz in the *S*-parameter measurement was used here. The eye amplitudes of the measured NRZ signals in Fig. 12 are 4.1, 3.95, 3.5, and 3.03 Vppd for the signal Baud rates of 100, 112, 128, and 144 GBd, respectively. To assess the eye quality, the measured 100-GBd NRZ eye is taken as an example, and it has 7.8-ps eye width, 1.82-V eye height, 14.7-dB signal-to-noise ratio (SNR), and 365-fs root mean square (rms) jitter. At 128 GBd, the measured NRZ eye

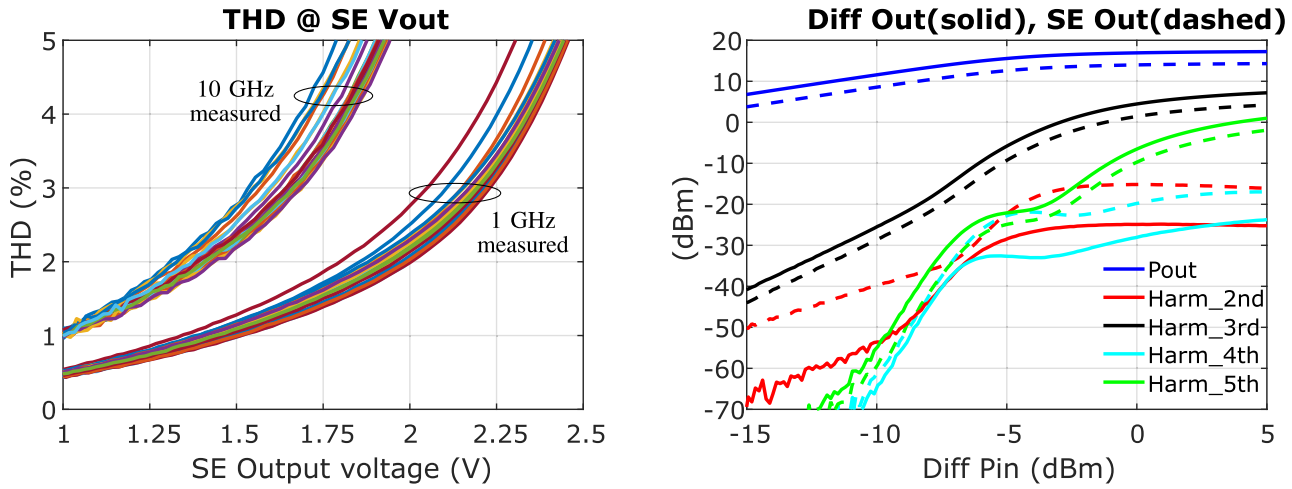

Fig. 11. Measured THD with differential input and SE output (left) and one harmonic comparison between differential output and SE output at 1 GHz using the highest gain setting (right).

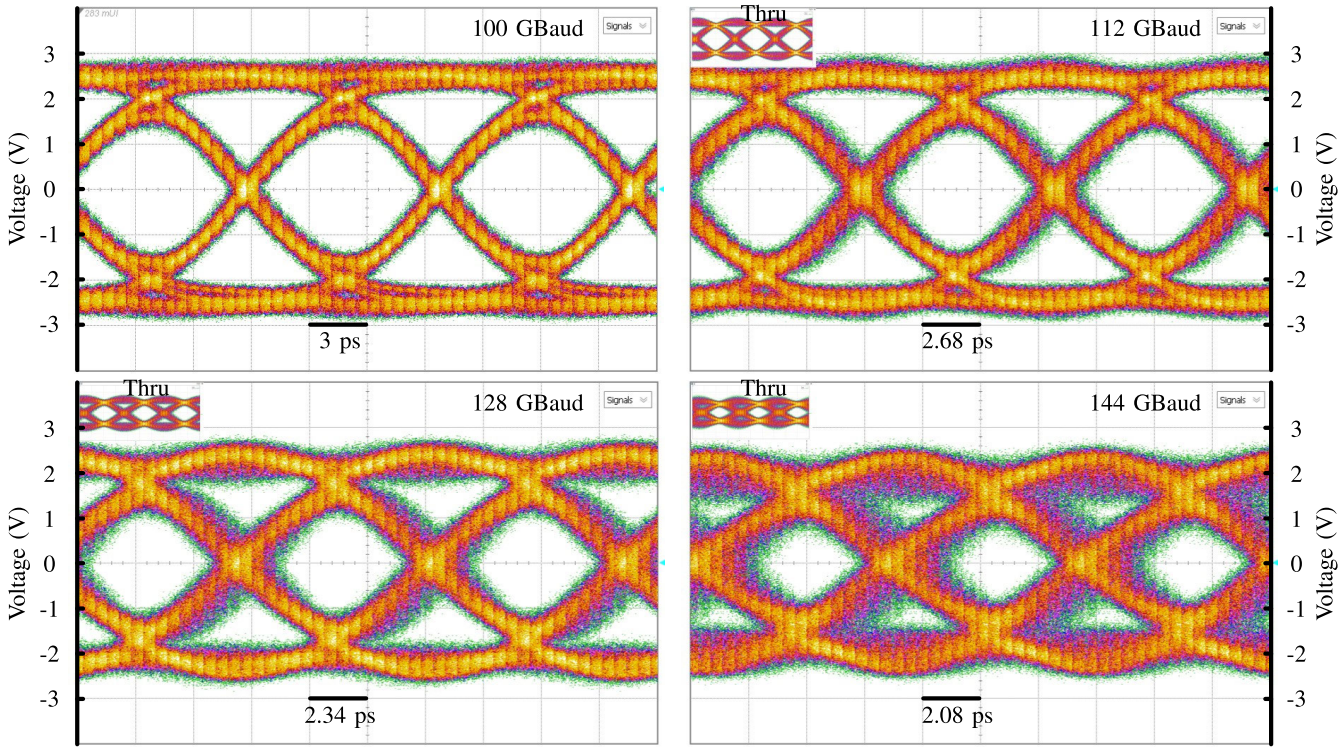

Fig. 12. Measured NRZ eye diagrams with 100-, 112-, 128-, and 144-GBd rates.

remains open with a 4.13-ps eye width, 1.47-V eye height, 14.2-dB SNR, and 614-fs rms jitter. For comparison, the SNR, eye width, and rms jitter values in the Thru measurement at 128 GBd are 16.6 dB, 3.75 ps, and 677 fs, respectively.

The measured PAM-4 eye diagrams in Fig. 14 were aimed at observing the linear behavior performance of the driver. Based on the IEEE 802.3cu standard, taking a hit ratio of $1.0E-2$, the measured peak-to-peak swings are 4, 3.59, 3.434, and 3.425 for baud rates of 72, 106, 112, and 128 GBd, respectively. The PAM-4 eye linearity was characterized by ratio level mismatch (RLM) measurement using IEEE 802.3 Clause 94 definition. The RLM values of those PAM-4 eyes are 0.934, 0.975, 0.973, and 0.972 for the data baud rates of 72, 106, 112, and 128 GBd, respectively. The 72-GBd PAM-4 eye diagram achieved the highest PAM-4 eye swing but with the lowest RLM value, corresponding to the skew observed between the upper and lower eyes compared with the middle eye. This indicates the driver probably entered the saturation region with an output swing of 4 Vppd.

D. Performance Comparison

The performance comparison of the proposed driver with the state-of-the-art designs is presented in Table I. The

TABLE I
PERFORMANCE COMPARISON WITH OTHER STATE-OF-THE-ART DRIVERS

	[13]	[18]	[2]	[14]	[15]	[10]	[12]	**This work**
Driver type Open collector?	Lumped Yes	Lumped N.A.	Lumped Yes	Distributed No	Distributed No	Distributed No	Hybrid No	**Hybrid** **No**
Low-frequency Gain (dB)	21	14.4	13-22.5	16.9	12.5	20.75	14-16.5	**11.2-21.8**
Elec.3dB Bandwidth (GHz)	>67	106	48	>110	90	>70	>67	**>70**
Gain x Bandwidth (GHz)	>752	556	640	>770	380	>763	>448	**>861**
Maximum peaking (dB)	20	6.2	N.A.	<1[c]	>2[c]	2	<2[c]	**4.3**
Output Swing (Vppd) @ PAM-4 or NRZ Baud rate (GBaud) Z_O (Ω)	4.5[a]	3 PAM4 80 100	N.A.	3.21[a]	4 PAM4 45 50	4.4 PAM4 64 50	2.8 NRZ 120 25	3.425[b] PAM4 **128** **50**
THD (%)@ Output Swing (Vppd)	N.A.	N.A.	2.2@1 GHz 1.5	N.A.	<5 @1 GHz 3[d]	4[d]@4 GHz 4.5	<2.5 @1 GHz 3.4[d]	**<2@1 GHz** **3.56**
OP1dB diff (dBm)	14 @1 GHz	12 @1 GHz	N.A.	14.1 @60 GHz	13.5[c] @1 GHz	14.25[d] @4 GHz	16.7 @1 GHz	**15.2** **@1 GHz**
Measured NRZ Baud rate (GBaud)	N.A.	N.A.	N.A.	120	120	120	120	**144**
Measured PAM-4 Baud rate (GBaud)	N.A.	80	N.A.	N.A.	45	64	N.A.	**128**
Power consumption (W)	0.35	0.74	0.225	0.509	0.55	1.1	0.96	**0.725**
Power efficiency (pJ/bit)	N.A.	4.63	1.41	4.24	4.58	8.59	8	**2.83**
FOM (GBaud)	N.A.	1.22	N.A.	N.A.	3.27	2.82	4.9	**5.18**
Technology	90-nm SiGe BiCMOS	0.7-um InP DHBT	65nm CMOS	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	55-nm SiGe BiCMOS	55-nm SiGe BiCMOS	**55-nm** **SiGe** **BiCMOS**
f_T/f_{MAX} (GHz)	310/370	370/430	N.A.	470/700	300/500	320/350	320/370	**330/370**

[*] *a, calculated from Po1dB. b, Defined by peak to peak based on the IEEE 802.3cu standard. c, read from the presented charts. d, read and estimated from the presented charts.*

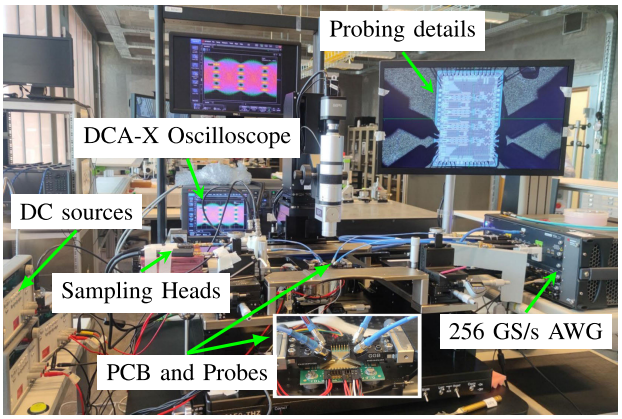

Fig. 13. Large-signal measurement setup.

lumped drivers proposed in [2], [11], and [13] achieved a low-frequency gain of over 15 dB, but their output stages were designed with an open-collector topology, which intrinsically has 6 dB more gain than the one with the internal 50-Ω output matching resistors. Based on TWA topology, [10], [12] presented drivers with bandwidths of over 67 GHz and low-frequency gains of more than 16 dB. However, their power consumption is 1.1 and 0.96 W, 50% and 32% higher than the driver proposed in this article. Using the technology with f_T/f_{MAX} of 470/700 GHz, [14] achieved a quite high bandwidth and medium gain, but the measured eye swing is less than 1.6 Vppd. In addition, the published works seldom discussed ESD diodes in their high-speed in/out path and the corresponding input and output matching networks. The chip can indeed get more bandwidth if there are no ESD diodes. However, ESD diodes are important to protect sensitive chips or systems from electrical overstress failures in-package integration. The proposed driver designed the specified input and output matching networks to alleviate the bandwidth degradation caused by the ESD diodes and bandpads. The *S*-parameter measurement results show the chip obtained a maximum low-frequency gain of more than 20 dB and a bandwidth of over 70 GHz with internal 50-Ω output matching resistors. More importantly, with a tunable gain of more than 10 dB, the driver can deliver a constant output swing of 3.59 Vppd and keep the THD lower than 2% at 1 GHz while the input swing changes with more than 700 mV. This is the first time a driver reported the ability to accommodate such a wide input swing. The proposed driver acquired the measured data rate of 256 Gb/s under a power consumption of 725 mW, resulting in a 2.83-pJ/bit power efficiency. The power consumption breakdown of the complete chip is shown in Fig. 15. The output stage consumes the highest power as it is responsible for delivering a signal with a high swing and good linearity.

The overall performance comparison is represented by the figure of merit (FOM), as defined in (1) [18]. Where DR is the maximum measured PAM4 baud rate, $V_{\mathrm{out,pp}}$ is the differential output swing at DR, Z_O is the differential output impedance at DR and $V_{\mathrm{out,pp}}$, and P_{dc} is the dc power consumption of the circuit. The proposed driver achieved the highest FOM of 5.18 GBd in the comparison table.

$$\mathrm{FOM} = \frac{\mathrm{DR}.V_{\mathrm{out,pp}}^2}{8.Z_O.P_{\mathrm{dc}}} \tag{1}$$

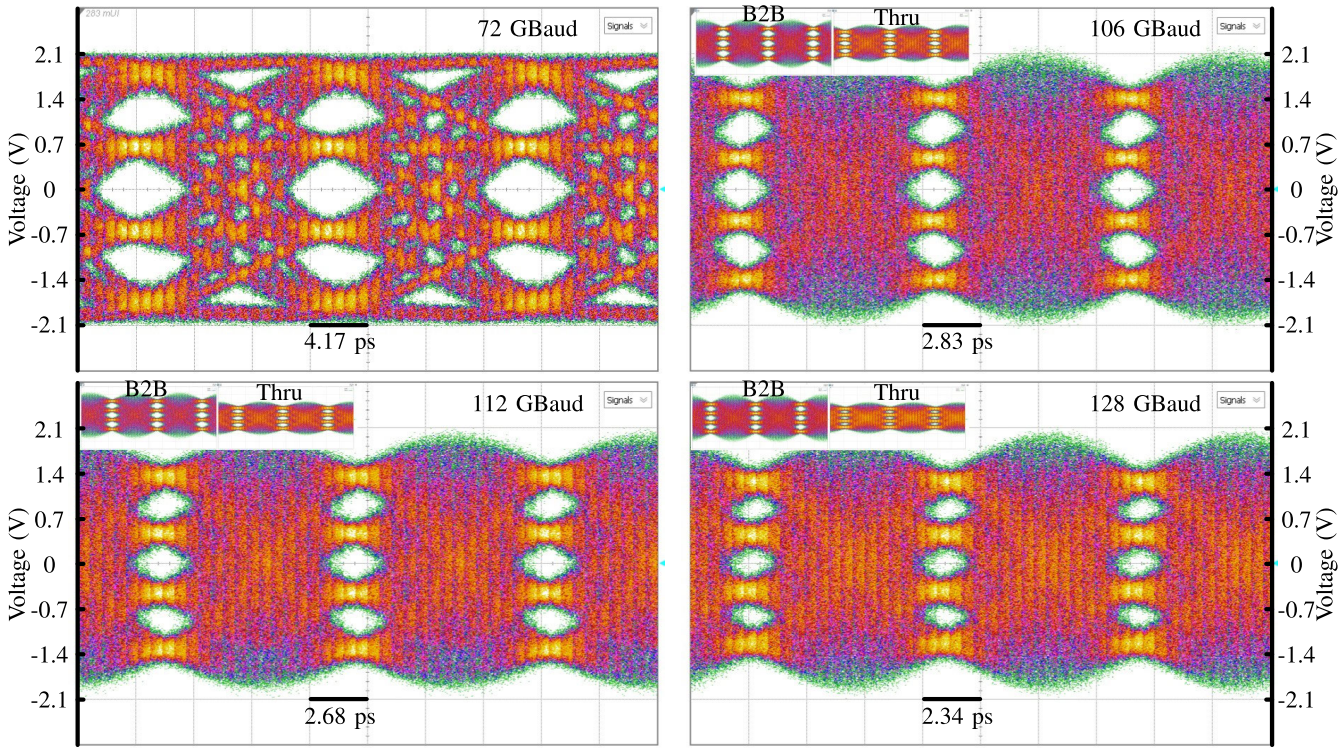

Fig. 14. Measured PAM-4 eye diagrams with 72-, 106-, 112-, and 128-GBd rates.

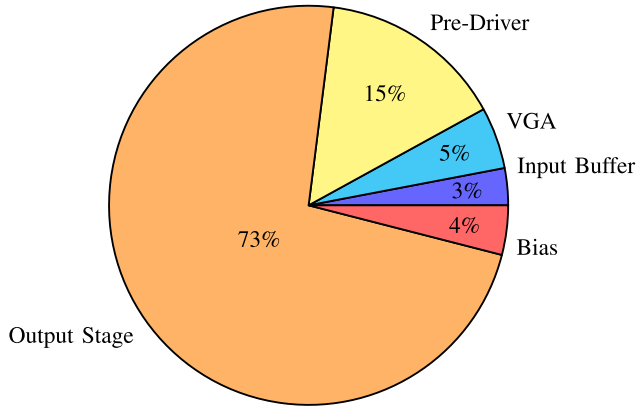

Fig. 15. Power consumption breakdown of the complete chip.

IV. Conclusion

This article presents a linear differential modulator driver for optical links beyond 120 GBd. It was designed with a lumped VGA, predriver, and a TWA output stage to better balance gain, bandwidth, and power consumption. To improve the linear input swing range, a Gilbert cell VGA with variable degeneration resistors was implemented to control the signal power level delivered to the main gain stage. The fabricated chip was fully characterized by *S*-parameter, power, and large-signal measurements. The *S*-parameter measurement results show the driver obtained a maximum low-frequency gain of 21.8 dB with more than 10-dB gain control capability and a 3-dB bandwidth beyond 70 GHz. Power measurement results show the driver exhibits good linearity with a THD below 2% with a constant output swing of 3.56 Vppd at 1 GHz, though the input swing changed over 700 mV. The proposed driver measured a 128-GBd PAM-4 eye diagram with a swing of more than 3 Vppd under a total power consumption of 725 mW. This corresponds to a 2.83-pJ/bit power efficiency or an FOM of 5.18 GBd. To the best knowledge of the authors, the fabricated modulator driver reported the highest operating data rate of 256 Gb/s with a swing of more than 3 Vppd. It also achieved the best power efficiency or FOM in non-CMOS drivers.

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Shengpu Niu received the B.Sc. and M.Sc. degrees in electronic engineering from the University of Electronic Science and Technology of China, Chengdu, China, in 2015 and 2018, respectively. He is currently pursuing the Ph.D. degree at the IDLab Design Group, Department of Information Technology, Ghent University—imec, Ghent, Belgium.

In 2018, he joined the IDLab Design Group, Department of Information Technology, Ghent University—imec. His research interests include designs of high-speed and ultra-wideband TXs and RXs for wireline communications in SiGe BiCMOS technologies.

Riaz Ahmed received the B.Eng. degree (Hons.) in electronic and microelectronic engineering from Brunel University London, Uxbridge, U.K., in 2007.

He joined the Fujitsu Microelectronics Europe Mixed Signal IC Division, where he was a Design Engineer on several high-speed data converters in CMOS processes from 65- to 7-nm nodes. Subsequently, he worked as a Senior Researcher at Kandou Bus on high-speed SERDES developments before joining the IDLab Design Group, Ghent, Belgium. His research interests include high-speed data converters for wireline applications.

Joris Lambrecht (Member, IEEE) received the Ph.D. degree in electrical engineering from Ghent University, Ghent, Belgium, in 2019, with a focus on high-speed transimpedance amplifiers.

Since 2020, he has been with imec, Leuven, Belgium, as a Senior Researcher, working on high-speed analog and mixed-signal IC design. His research interests include digital-to-analog conversions (DACs), analog-to-digital conversions (ADCs), transceiver front-ends, and photonic integrated circuits (PICs) for high-speed optical/electrical transceivers.

Jakob Declercq was born in Kortrijk, Belgium, in 1997. He received the B.Sc. degree in engineering and the M.Sc. degree in electrical engineering from Ghent University, Ghent, Belgium, in 2018 and 2020, respectively. He is currently pursuing the Ph.D. degree at Ghent University, where he is associated with the IDLab Design Group, a research group associated with imec, Leuven, Belgium.

His current research interests include opto-electronic receiver chip design for high-speed broadband intensity modulation direct detection (IMDD) and coherent optical communication systems.

Marijn Verbeke (Member, IEEE) received the M.S. and Ph.D. degrees in electrical engineering from Ghent University, Ghent, Belgium, in 2013 and 2018, respectively.

After completing his Ph.D. degree, he worked for two years as a System on Chip Design and Validation Engineer with Nokia, Antwerp, Belgium. He is currently a Senior Researcher at imec, Leuven, Belgium, focusing on high-speed IC design. His technical research interests include analog/digital/mixed-signal circuit design, system-level analysis, and digital signal processing, with a primary focus on clock and data recovery and high-speed optoelectronic circuits, particularly for (optical) transceivers.

Michiel Verplaetse (Member, IEEE) was born in Ghent, Belgium, in 1993. He received the M.Sc. and Ph.D. degrees in electrical engineering from Ghent University, Ghent, in 2016 and 2020, respectively, with a focus on high-speed analog equalization structures.

From 2016 to 2021, he was a part of the imec-IDLab Research Group, Ghent, focusing on analog design research in high-speed communication applications. In 2021, he joined the Fixed Networks Department, Nokia Bell Labs, Antwerp, Belgium, working on high-speed optical access systems and hardware design. He has authored and coauthored numerous peer-reviewed journal, conference papers, and patent applications.

Bart Moeneclaey (Member, IEEE) was born in Ghent, Belgium, in 1988. He received the M.Sc. and Ph.D. degrees in electrical engineering from Ghent University, Ghent, in 2011 and 2018, respectively.

He is currently a Senior Researcher with imec, Leuven, Belgium, working on high-speed analog and mixed-signal IC design. His research interests include data converters and transceiver front-ends for high-speed wireline and optical communication systems.

Cheng Wang received the B.Sc. degree in microelectronics from Xidian University, Xi'an, China, in 2017, and the M.Sc. degree in microelectronics from Fudan University, Shanghai, China, in 2020.

From 2018 to 2020, he was an Analog IC Design Engineer Intern at PhotonIC, Shanghai, for SPAD-based LiDAR transceivers. From 2020 to 2021, he was an Analog IC Design Engineer with Goodix, Shanghai. He is currently pursuing the Ph.D. degree at the IDLAB-Design Group, Ghent University (UGent)—imec, Ghent, China, for researching and developing simplified coherent burst mode receivers for high-speed passive optical network (PON) applications. His research interests include optical-electrical high-speed analog IC design.

Joris Van Kerrebrouck received the M.Sc. degree in electrical engineering from Ghent University, Ghent, Belgium, in 2014.

He joined the IDLab Design Group, Ghent University—imec, where he focuses on high-speed electrical/optical transceivers. His current research interests include high-speed SiGe BiCMOS analog circuits and optoelectronic systems.

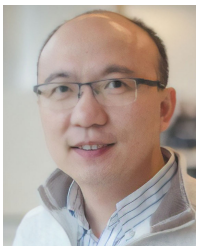
Nishant Singh received the B.E. degree in electrical and electronic engineering from the University of Botswana, Gaborone, Botswana, in 2013, the M.E. degree in microelectronic engineering from the University of Pretoria, Pretoria, South Africa, in 2017, and the Ph.D. degree from Ghent University (UGent), Ghent, Belgium, in 2023.

He was with the Carl and Emily Fuchs Institute of Microelectronics (CEFIM), University of Pretoria. He is currently with the IDLab Design Group, UGent—-imec. His research interests include electromagnetic design and monolithic integration of high frequency and optical communications systems for low-cost high-capacity networks.

Johan Bauwelinck (Senior Member, IEEE) received the M.Sc. and Ph.D. degrees in electrical engineering from Ghent University, Ghent, Belgium, in 2000 and 2005, respectively.

Since October 2009, he is currently a Professor with the IDLab Research Group, Department of Information Technology (INTEC), Ghent University, and imec, Leuven, Belgium, where he is leading the Design Lab since 2014 (currently 35 people strong). His research interests include high-speed, high-frequency (opto-)electronic circuits and systems for optical communication and sensing. He was and is very active in EU-funded projects such as Streams, Teraboard, POETICS, HandheldOCT, Sprinter, Lolipop, ESA Protobix, and MSCA Nitelidar. He has promoted 28 Ph.D. students and coauthored more than 350 publications and ten patents.

Prof. Bauwelinck co-chaired the Technical Program Committee of the European Conference on Optical Communications (ECOC) in 2020. In 2022, he became an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS.



Xin Yin (Senior Member, IEEE) received the Ph.D. degree in electronic engineering from Ghent University, Ghent, Belgium, in 2009.

Since 2007, he has been a Staff Researcher with imec, Leuven, Belgium. Since 2013, he has also been a Professor with the Department of Information Technology (INTEC), Ghent University. He was and is active in European and international projects such as PIEMAN, EUROFOS, MARISE, C3PO, DISCUS, Phoxtrot, MIRAGE, SPIRIT, WIPE, Teraboard, STREAMS, PICTURE, QAMeleon, 5G-PHOS, UniQorn, PlasmoniAC, POETICS, NEBULA, BeQCI, QSNP, EQUO, MWP4SPACE, and GreenTouch Consortium. He has authored and coauthored more than 250 journals, book chapter, and conference publications in the field of high-speed electronics and fiber-optic communication. His research interests include high-speed opto-electronic circuits and transceiver subsystems for datacom/telecom/6G, and ultralow-noise front-end and mixed-signal integrated circuit design for neuromorphic and quantum applications.

Dr. Yin is a member of the ECOC and Optica APC Technical Program Committee (TPC). He has led a team including international researchers from imec, Bell Labs USA/Alcatel-Lucent and Orange Labs France, which Won the GreenTouch 1000x Award in recognition of the invention of the Bi-PON protocol and sustained leadership.