# Route Toward Commercially Manufacturable Vertical GaN Devices

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***Abstract*— To make vertical GaN-based trench gate MOSFET devices commercially manufacturable, 200 mm engineered substrates with a poly-AlN core are a good substrate choice. The poly-AlN core, matched in thermal expansion to GaN, allows to grow high-quality thick GaN layers. Up to 11 $\mu$m-thick GaN stacks were grown crack-free, with excellent control over the wafer warp. Breakdown values of 900 V were reached for the vertical p/n-junction. Full device processing was completed in a CMOS-compatible pilot line without any wafer breakage, demonstrating the mechanical strength of these substrates. On module level, a new gate trench profile combining a smooth sidewall and round corners, is presented. While a smooth sidewall is important for the ON-state performance of the devices, the rounded corners are beneficial for the OFF-state operation. A semi-vertical test vehicle was used to demonstrate the ON-state of the fabricated power transistors. For devices with an effective gate width ($W_{G,eff}$) of 180 mm and an active area of 1.4 mm$^2$, an ON-state resistance could be achieved of 8 m$\Omega \cdot$ cm$^2$. By scaling the source contact length down, the device footprint could be decreased further. It is shown that for devices with a $W_{G,eff}$ of 60 mm this value could be further improved with best performing devices showing a 6.2 m$\Omega \cdot$ cm$^2$ ON-state resistance.**

***Index Terms*— GaN, manufacturability, power, trench gate MOSFET, vertical devices.**

## I. Introduction

IN POWER electronics, GaN technology is being applied in a wide range of applications due to its faster switching speeds and excellent voltage-blocking capability in comparison to Si-based conventional technology. For applications, targeting operating voltages up to 650 V, lateral $p$-GaN high-electron-mobility transistor (HEMT) devices are mature [1], [2], and products are available on the market [3], [4]. Yet lateral HEMTs have a fundamental limit regarding the trade-off between the breakdown voltage and the device footprint due to the increased gate-to-drain distance needed to achieve high voltage robustness. Moreover, with increasing breakdown voltage, it gets more difficult to spread the OFF-state potential difference between the gate and drain. Hence, higher electric field peaks are present in the top part of the device, between the gate and drain, which affect mainly the long-term reliability of the devices. Since the main current flow is close to the surface, electron trapping at surface states and trap creation by hot electrons due to the presence of high electric fields become a serious concern. Therefore, vertical GaN devices have gained a lot of interest in research for application voltages beyond 650 V. With the main voltage drop being spread vertically over the epitaxial stack, the device footprint is independent of the target voltage and excellent ON-state resistance values can be achieved in combination with high voltage blocking capability, as shown in [5], [6], [7], [8], [9], and [10]. Today, most of the available research for the fabrication of vertical GaN devices is on GaN substrates with limited substrate size and high cost, and devices are mostly fabricated in lab environments. He et al. [9] presented fabricated devices on 100 mm GaN substrates, which extends the GaN wafer diameter further compared to the typically used 50 mm substrates. With this work, we propose a route toward commercially manufacturable vertical GaN devices using large diameter 200 mm engineered substrates, which are scalable to 300 mm, as well as a CMOS compatible pilot line. This work is a continuation of what was reported in [11], [12], [13], and [14]. As a substrate choice, for vertical or quasi-vertical transistors, in literature Si substrates are being explored as a cheap alternative to GaN substrates, allowing large substrate diameters [15], [16], [17], [18], [19]. Large Si substrate size in combination with a thick epitaxial stack is however expected to make the wafers fragile and increases the challenges to fabricate the devices without wafer breakage, due to the thermal and the lattice mismatch between GaN and Si. Therefore, in this work, we select engineered substrates, namely Qromis Substrate Technology (QST[1]) wafers, which consists of a polycrystalline ceramic core (poly-AlN), covered by several encapsulation layers on top of which is a $SiO_2$ bonding layer and a single crystalline Si layer which serves

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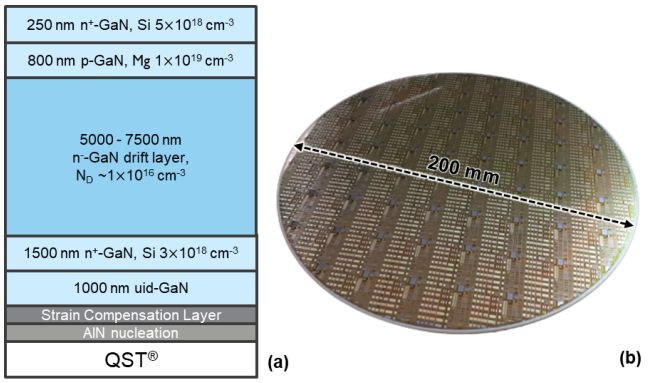


Fig. 1. (a) Schematic representation of epitaxial stack on engineered poly-AlN substrate and (b) picture of fully processed 200 mm device wafer.

TABLE I
XRD FWHM OF GaN <102> AND GaN <002> PEAKS

| Drift layer thickness (μm) | Total stack thickness | GaN<102> FWHM (arcsec) | GaN<002> FWHM (arcsec) |
|---|---|---|---|
| 5 | 8.5 | 331 | 165 |
| 7.5 | 11 | 314 | 155 |

as the top layer for the MOCVD growth [20]. The higher mechanical strength of poly-AlN core, matched in thermal expansion to GaN, allows to grow very thick GaN layers on 200 mm substrates [21], [22], [23], [24] without making the wafers fragile, opening a path toward manufacturable vertical GaN devices. These substrates have SEMI standard specifications.

This article consists of three sections. First, we describe the GaN epitaxy on 200 mm QST[1] substrates. Next, the CMOS compatible device fabrication with focus on manufacturability will be discussed, and finally, the results on device footprint scaling are reported.

## II. GaN Epitaxy on Large Diameter Substrates

By choosing a large diameter substrate, the amount of power transistors that can be processed on a wafer increases and the cost per fabricated device decreases. On the selected QST[1] engineered substrate (Fig. 1), thanks to higher mechanical strength of the poly-AlN core, thick crack-free GaN layers could be grown, reaching a total thickness up to 11 $\mu$m. The GaN layers were grown by means of MOCVD using an AIX G5+ C Planetary Reactor[1] from AIXTRON. The stack consists of a 200 nm AlN nucleation layer, a strain-compensating layer, a 1 $\mu$m unintentionally doped (uid)-doped GaN layer for defect reduction, a 1.5 $\mu$m $n^+$-GaN bottom contact, a 5–7.5 $\mu$m-thick $n^-$-GaN drift layer, an 800 nm Mg-doped p-GaN inversion channel layer, and a 250 nm $n^+$-GaN top contact layer, as depicted in Fig. 1.

Owing to the aforementioned strong mechanical strength of the poly-AlN core, for GaN layers with a thickness up to 11 $\mu$m, no wafer breakage was observed either during MOCVD growth and wafer screening or during device fabrication in the 200 mm pilot line. On top of that, good

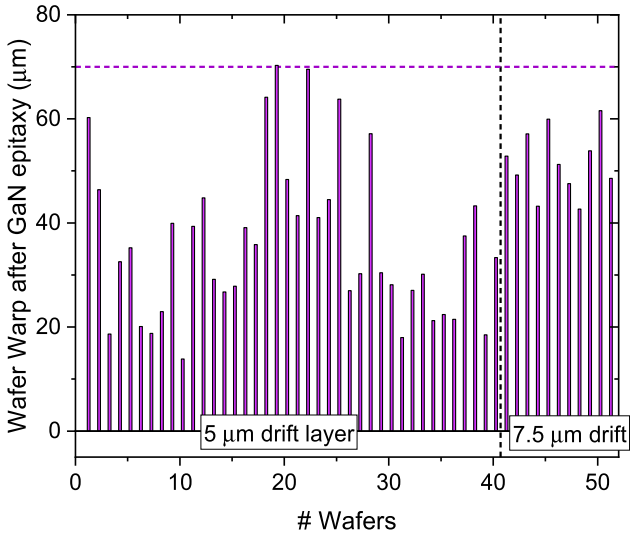


Fig. 2. Wafer warp of 200 mm engineered substrates with poly-AlN core after GaN epitaxy.

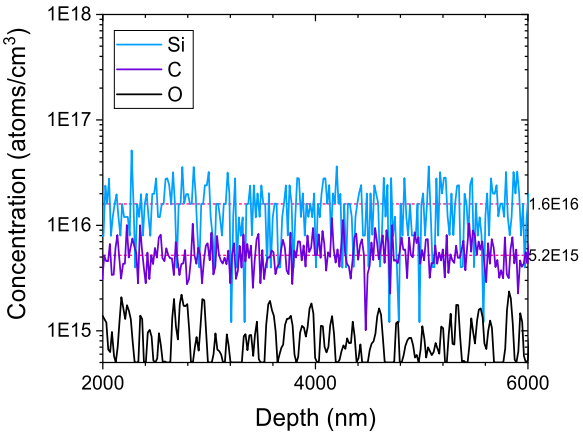


Fig. 3. SIMS analysis of Si, C, and O concentration in drift layer part of GaN epitaxial stack on engineered QST[1] substrates.

control of the wafer shape was obtained, keeping the wafer warp consistently below 70 $\mu$m after GaN epitaxy for all wafers as depicted in Fig. 2. Good crystal quality of the grown GaN layers was also obtained, as illustrated by the X-ray diffraction full-width half maximum (XRD FWHM) values in Table I, where for the GaN<102> peak values as low as 331 and 314 arcsec were extracted for an 8.5 and 11 $\mu$m-thick stack, respectively. For the GaN<002>, peak values as low as 165 and 155 arcsec were extracted, respectively. The crystal quality of these types of stacks can be improved further by using an epitaxial lateral overgrowth (ELOG) in the lower part of the stack. For further details on the ELOG technique, the reader is referred to [25]. Our work related to the ELOG technique is extensively reported in [26]. XRD values as low as 273 and 211 arcsec for the GaN<102> and GaN<002> were obtained, respectively, for layers with a 5 $\mu$m thick drift layer [26]. Due to the improvement in the GaN<102> FWHM value, we observed a significant decrease in the amount of edge dislocations present in the GaN stacks [26].

To obtain good voltage-blocking capability in reverse bias, a low Si concentration of $1.6 \times 10^{16}$ cm$^{-3}$ was

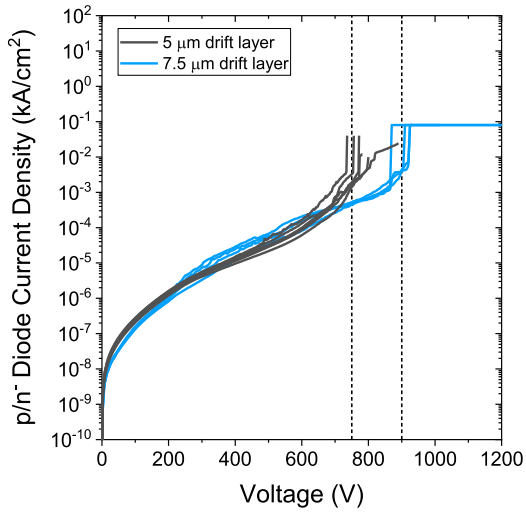


Fig. 4. Reverse J-V characteristic of p/n$^-$-diode, comparing epitaxial stacks with 5 and 7.5 $\mu$m-thick GaN drift layers.

targeted in the drift layer. As a MOCVD reactor is used, during the drift layer growth, it is important to achieve good suppression of the background C-doping. From SIMS analysis (Fig. 3), a background C concentration of $\sim$5.2 $\times$ 10$^{15}$/cm$^3$ is demonstrated, which results in an active net donor concentration (N$_D$) of about $\sim$1 $\times$ 10$^{16}$ cm$^3$ in the drift layer. Electrical validation of the grown stacks was performed by testing the vertical p/n-junction. To fabricate these diodes on wafer, the same termination method is used as in transistor processing, using a shallow mesa and N-implant outside the active area of the p-contact. In the isolated area, contact with the buried n$^+$-GaN is formed from the frontside of the wafer. Breakdown voltages of $\sim$750–900 V were measured in reverse bias for a 5 and 7.5 $\mu$m-thick drift layer, respectively (Fig. 4). These hard breakdown values are higher compared to our previously reported work with 5 $\mu$m drift layer thickness, mainly due to an optimization of the GaN epitaxial stack as well as the metal contact scheme used in the diode, as discussed in [12]. The achieved hard breakdown values represent almost 70% of the theoretical breakdown of an ideal p/n-junction with a thickness of 7.5 $\mu$m and net donor concentration of $\sim$1 $\times$ 10$^{16}$ at/cm$^3$ in the drift layer considering a critical electric field of 2.5 MV/cm. For future work, by using the ELOG technique and thicker drift layers in the GaN epitaxial stack, as well as module development for optimal edge termination of the diode structures, further improvement in the breakdown voltage is expected.

## III. CMOS Compatible Processing on 200 mm Substrates

To make vertical devices commercially manufacturable, we have set up a process flow using CMOS-compatible materials in a 200 mm pilot line. This allows us to transfer the technology to production lines after the development phase has been completed. As GaN regrowth or chemical mechanical polishing (CMP) are complex and expensive processing steps, they were not considered as an option for the fabrication of this generation of devices. Yet, it is known

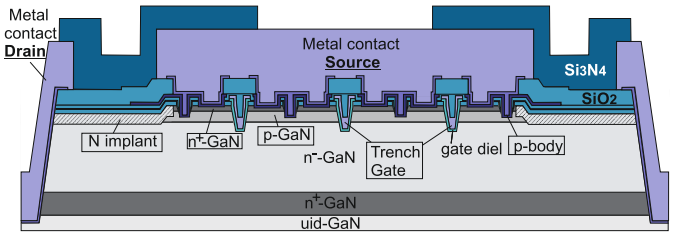


Fig. 5. Schematic representation of semi-vertical trench gate MOSFET device.

that these solutions can enable significant device performance improvement (e.g., vertical trench-gate devices with a regrown uid-GaN accumulation channel to achieve higher channel mobility [6], [10]). In this work, we fabricated trench gate MOSFET devices, with an electron inversion channel formed on p-GaN at a MOS interface.

### A. Process Flow Description

Semi-vertical trench gate MOSFET devices were fabricated as test vehicles to study the device performance in ON-state. The electrons flow from the source n$^+$ layer into the inversion channel at the p-GaN/dielectric interface, and then through the n$^-$ drift layer before being collected via a buried n$^+$-GaN layer with a deep drain contact at the frontside of the wafer. The n$^+$-GaN and p-GaN top layers are isolated from the drain by a shallow mesa etch combined with an N implant. The gate trench was processed using a 2.5 nm AlON and 100 nm $SiO_2$ bilayer dielectric, with a TiN/Ti/Al gate metal stack on top. The contacts to the source n$^+$-GaN, p-body, and drain n$^+$-GaN are made using a Ti/Al containing metal stack. A stack of $Al_2O_3$, $SiO_2$, and $Si_3N_4$ layers is used as surface passivation. A schematic representation is given in Fig. 5.

### B. Gate Trench Module Development

When considering the optimization of the ON-state performance of vertical trench gate MOSFET devices, there are two main contributors to the ON-state resistance value, being the gate channel and the drift layer. A careful design of the Mg concentration in the p-GaN layer as well as good activation are required to avoid full depletion of the p-GaN layer during OFF-state operation. Moreover, these parameters have significant impact on the channel mobility and threshold voltage (Vt) stability, as reported in [14] and [27]. In [14], a method has been presented to analyze the measured drain current to gate-to-source voltage ($I_D V_{GS}$) curves by fitting a theoretical MOS equation that includes the contribution of the series resistance (which is not negligible in these devices). The Vt, carriers' mobility, and series resistance were extracted with this methodology. It has also been observed that the interface dielectric choice and Mg activation anneal play an important role in the achieved channel mobility. In this work, the activation of the p-GaN layer is done with the gate and p-body area exposed, using a 20 min anneal in $N_2$ at 825 °C and a 1 $\times$ 10$^{19}$ Mg/cm$^3$ chemical doping concentration. For these devices, a channel mobility of $\sim$30 cm$^2$V$^{-1}$s$^{-1}$ has been extracted. A typical $J_D V_{GS}$ curve, with the fit

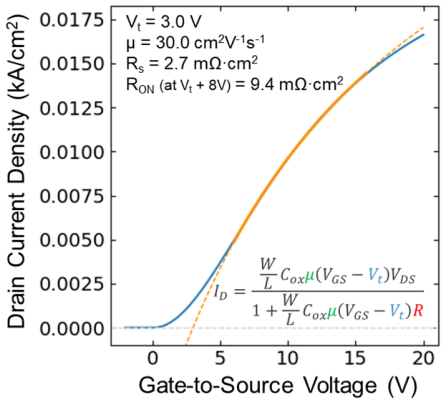


Fig. 6. Typical $J_D V_{GS}$ curve, with the fit curve from the theoretical MOS equation [14] to extract the $V_t$, the carriers' mobility, and the series resistance of the trench gate MOSFET devices.

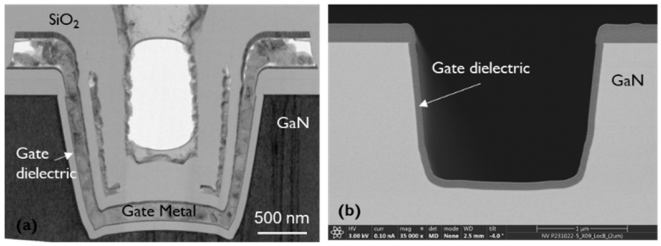


Fig. 7. (a) X-sectional TEM image of gate trench module as processed in demonstrator devices and (b) X-sectional SEM image of improved gate module with rounded corners.

curve from the theoretical MOS equation and the extracted parameters, including the channel mobility is depicted in Fig. 6. For GaN based trench gate MOSFET devices using an inversion channel, the value obtained for channel mobility is competitive with values reported in literature ranging from 10 to 40 $cm^2V^{-1}s^{-1}$ [15], [18], [28].

In the fabricated devices, an optimized dry etch and wet cleaning sequence in the gate trench was applied to obtain a smooth gate sidewall, as described in [29]. A typical image of the gate module, as processed in the demonstrator devices from which results are reported in this work, is depicted in Fig. 7(a). As it is observed that the current generation of devices shows premature breakdown in OFF-state compared to the superior p/n-diode blocking capability, a major gate module development has been performed to: 1) guarantee a smooth gate trench sidewall and 2) obtain a rounded gate trench corner, as depicted in Fig. 7(b). This was obtained by optimization of gas flows, pressure, and transformer-coupled plasma (TCP) bias power during the dry etch of the GaN. This solution is expected to lower the electric field peak in the gate trench corner and to increase the OFF-state device breakdown. In future work, the OFF-state performance of these devices will be reported.

In our devices, we make use of bi-layer gate dielectrics [30]. In the gate module, it has been observed that using a bi-layer dielectric, consisting of a thin 2.5 nm AlON and a bulk $SiO_2$ layer, gives the best performance. In the fabricated devices, a thickness of 100 nm has been selected for the

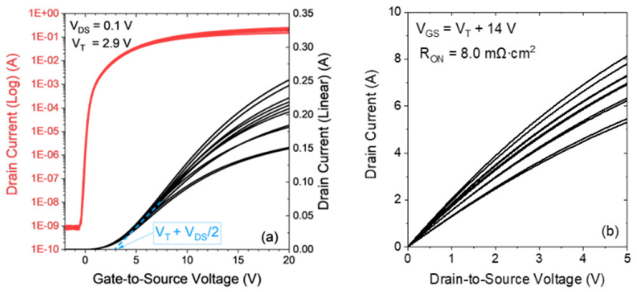


Fig. 8. (a) Transfer characteristic and (b) output characteristic of power transistor devices with $W_{G,eff} = 180$ mm.

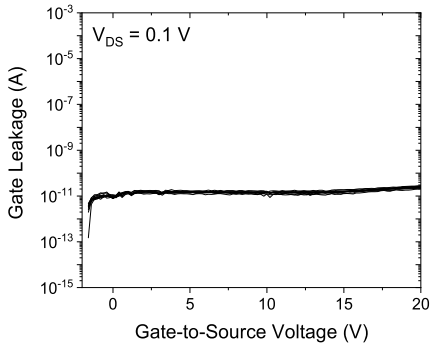


Fig. 9. Gate-to-source forward leakage current of power transistors with $W_{G,eff} = 180$ mm.

$SiO_2$ bulk dielectric. From double sweep, $I_D V_{GS}$ measurements with a fixed gate overdrive, and positive bias temperature instability (PBTI) measurements, AlON has been compared to $Al_2O_3$ and demonstrated to result in better $V_t$ stability in devices, as reported in [31]. The $SiO_2$ bulk dielectric ensures good device performance in terms of time-dependent dielectric breakdown (TTDB), as also reported in [31].

Using the gate architecture depicted in Fig. 7(a) and the process flow depicted in Fig. 5, as well as epitaxial stacks with a 7.5 $\mu$m-thick drift layer, power transistor devices with an effective gate width ($W_{G,eff}$) of 180 mm were fabricated, using a semi-vertical test vehicle, to extract the performance of large area transistor in ON-state. The fabricated transistors have an active device area of 1.4 $mm^2$. From the transfer characteristics, a $V_t$ of 2.9 V was extracted in a classical manner. The linear region in the $I_D$–$V_{GS}$ is extrapolated toward the $V_{GS}$ axis. The linear interpolation's slope is taken at the maximum transconductance. The intercept with the $V_{GS}$ axis gives $V_T + V_{DS}/2$. Note that a relatively steep subthreshold slope of 140 mV/decade is obtained. From the output characteristic, a drive current of ~6 A and a low ON-resistance of 8 $m\Omega \cdot cm^2$ were observed (Fig. 8). The gate-to-source forward leakage shows good yield in these large area power transistors and stays low for the measured range of $V_{GS}$ from −2 to 20 V, as depicted in Fig. 9.

### C. Scaling Device Footprint

In vertical devices, we aim to make the device footprint as small as possible, to ensure a low specific $R_{on}$. Moreover, the more devices that can be processed in a wafer, the

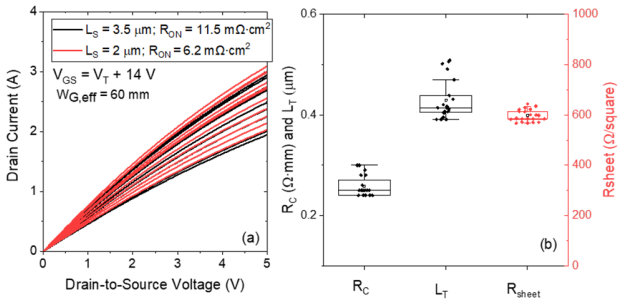


Fig. 10. (a) Comparison of output characteristics of power transistors with the source length equal to 3.5 and 2 $\mu$m and $W_{G,eff}$ = 60 mm and (b) measured values on the same wafer for the contact resistance, transfer length, and sheet resistance of the source $n^+$-GaN layer.

cheaper the transistor fabrication will be. We have chosen a design with 4 $\mu$m-thick Al metal running over the gate, which allows minimizing the gate-to-source distance. The choice of a thick Al metal ensures low resistance of the source fingers used in the devices. To scale down the device footprint further all used contact lengths, distances in between contacts and metal to contact overlaps should be minimized. In this section we present the impact of a downscaling of the source contact length ($L_S$). In the presented device in Fig. 8(a) $L_S$ of 3.5 $\mu$m has been used. In Fig. 10(a), the performance of power transistors with $W_{G,eff}$ of 60 mm and source lengths of 3.5 $\mu$m and 2 $\mu$m are compared. From the output characteristic, it is visible that the same current is reached when the same $V_{GS}$ overdrive is applied, and as the active device area decreased, a significant reduction of the ON-state resistance from 11.5 to 6.2 m$\Omega\cdot$cm$^2$ is achieved. The ON-state resistance value has been normalized by the active area of the devices including the gate and source area. To study if it is possible to further downscale $L_S$ to 1.5 or 1 $\mu$m, transfer length measurements (TLM) were done. The top $n^+$ layer of the wafer under test has a sheet resistance of 600 $\Omega$/sq, a contact resistance, and a transfer length as low as 0.25 $\Omega\cdot$mm and 0.41 $\mu$m, respectively, as depicted in Fig. 10(b). To reach these values, a Ti/Al/TiN containing Ohmic contact and low temperature anneal were used [32]. Considering the obtained transfer length in the ohmic contact, smaller contacts of 1–1.5 $\mu$m will be explored in future work. As the fabricated devices today have a semi-vertical device architecture with the drain fabricated at the frontside, an important module development in our future work is also to add the drain contact on the backside. A possible implementation of such a backside contact is shown in [33].

## IV. Conclusion

In our work, we proposed a route toward the fabrication of manufacturable vertical devices. For that, we have selected large diameter 200 mm engineered substrates. First, it was demonstrated that 11 $\mu$m-thick GaN stacks could be grown by MOCVD, with high quality, good control of wafer warp, and exhibiting excellent mechanical strength of the substrates itself, allowing trench gate MOSFET devices to be processed in a CMOS compatible process line. A 900 V breakdown has been achieved for the vertical p/n-junction. In future work, we plan to increase the drift layer thickness further and make use of stacks with the implementation of ELOG in the buffer, to improve the crystal quality of the layers further. Second, we have shown a gate trench module with smooth sidewalls as well as rounded corners at the bottom of the trench. This module will be applied in future generations of trench gate MOSFET devices. Finally, in this work, we have used a semi-vertical test vehicle to demonstrate the ON-state performance for power transistor devices, reporting values as low as 6.2 m$\Omega\cdot$cm$^2$. We do not consider this as a final product and module development is planned to access the buried $n^+$-GaN layer from the backside of the engineered substrates.

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