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Micro-transfer printing InP C-band SOAs on advanced silicon photonics platform for lossless MZI switch fabrics and high-speed integrated transmitters

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Abstract: We present an approach for the heterogeneous integration of InP semiconductor optical amplifiers (SOAs) and lasers on an advanced silicon photonics (SiPh) platform by using micro-transfer-printing (μTP). After the introduction of the μTP concept, the focus of this paper shifts to the demonstration of two C-band III-V/Si photonic integrated circuits (PICs) that are important in data-communication networks: an optical switch and a high-speed optical transmitter. First, a C-band lossless and high-speed Si Mach-Zehnder interferometer (MZI) switch is demonstrated by co-integrating a set of InP SOAs with the Si MZI switch. The micro-transfer-printed SOAs provide 10 dB small-signal gain around 1560 nm with a 3 dB bandwidth of 30 nm. Secondly, an integrated transmitter combining an on-chip widely tunable laser and a doped-Si Mach-Zehnder modulator (MZM) is demonstrated. The laser has a continuous tuning range over 40 nm and the transmitter is capable of 40 Gbps non-return-to-zero (NRZ) back-to-back transmission at wavelengths ranging from 1539 to 1573 nm. These demonstrations pave the way for the realization of complex and fully integrated photonic systems-on-chip with integrated III-V-on-Si components, and this technique is transferable to other material films and devices that can be released from their native substrate.

1. Introduction

Photonic integrated circuits (PICs) can realize complex functions in compact chip sizes while providing benefits in terms of cost, speed and power consumption over its contenders. Therefore, they are considered as promising solutions in a wide range of applications, including the power-hungry and high-capacity data- and telecommunication systems. By leveraging mature and existing advanced CMOS fabrication facilities, silicon(Si) PICs can be fabricated on 200 and 300 mm wafers with high yield. Due to the increasingly maturing SiPh platforms, essential building blocks including a wide range of high-performance passive components, Si modulators, Ge photodetectors (PDs) and SiGe electro-absorption modulators (EAMs) are readily available

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[1]. Furthermore, the high index contrast between Si and its oxide results in the possibility to implement complex PICs in very small footprints. Nevertheless, a hurdle that is impeding the expansion of the use of Si PICs is the absence of low-cost and high-performance integrated optical gain elements and light sources. Extensive research has been conducted in the past years to establish a reliable and cost-effective approach to overcome this issue. Amongst the existing methods, hetero-epitaxial growth of III-V on Si substrates is recognized as the ultimate solution. It allows for wafer-scale processing, high density integration, and significantly reduced consumption of expensive III-V material (there is e.g. no need for a thick III-V substrate) [2–5]. Impressive progress has been made in recent years, especially in the monolithic integration of GaAs/InAs quantum dot (QD) lasers due to their better defect-handling properties compared with quantum wells (QWs). A variety of state-of-the-art III-V-on-Si QD lasers have been demonstrated [6,7]. However, they are mostly stand-alone devices as the coupling of these devices to Si waveguide circuits remains challenging [8]. So this approach is still in an early stage of research, with much work to be done towards the realization of III-V-on-advanced-Si PICs. Hybrid integration of independently fabricated III-V and SiPh chips through flip-chip based micro-assembly is more straightforward [9,10]. It is therefore widely adopted in today's industry. However, the sequential procedure is time-consuming, and can require active alignment to pursue an efficient optical coupling from the laser to the passive waveguide circuits. This results eventually in a higher cost of the hybrid PICs. Meanwhile, heterogeneous integration through wafer bonding, especially multi-die-to-wafer bonding, has attracted much attention in the past decade [11]. In this case, the III-V epitaxial dies (mm-size) are first assembled on a temporary carrier wafer using mm-scale dies, and are then transferred onto the target SiPh wafer, with finished front-end layers, through wafer bonding. By introducing the III-V fabrication processes and modifying the Si back-end process flow, wafer-scale integration of complex III-V/Si PICs can be realized. This process has been adopted for commercial use since 2016 [12]. However, a dedicated back-end process flow has to be developed for each specific III-V material and it is challenging to co-integrate different III-V materials/devices on a common substrate [13]. An alternative technique that shows great potential for scalable, economical and flexible heterogeneous integration of III-V opto-electronic components on Si PICs is micro-transfer printing (μTP) [14]. This technique is developed by the Rogers group at the University of Illinois in 2004 [15]. It allows for the manipulation of micron-sized material coupons/devices using an elastomeric stamp [16]. By arranging the III-V devices on the native substrate in dense arrays, the waste of expensive III-V materials can be effectively minimized. Meanwhile, the integration can be performed in a massively parallel way by employing a stamp with a post array, whose size and pitch match those of the device array on the source wafer. The μTP process is fast with each printing cycle taking 30-45 seconds. A 3σ alignment accuracy of ± 1 μm can be achieved in a high-throughput mode while improved alignment can be obtained at lower throughput [17]. In this paper, we will first discuss the transfer printing process in general and subsequently the required adjustments to make the μTP procedure compatible with advanced SiPh platforms that feature a complex back-end layer stack. In the second half of this paper, the technique is demonstrated through the fabrication and characterization of two circuits that combine advanced SiPh with III-V SOAs. First, a high-speed C-band switch is discussed that offers sub-ns scale switching while overcoming the insertion loss by adding SOAs. Secondly, a III-V/Si transmitter is demonstrated, where a widely tunable laser and high-speed MZM are co-integrated using μTP.

2. Micro-transfer printing

Micro-transfer printing has been proposed as one of the approaches to heterogeneously integrate non-native functionalities, such as optical amplification, onto the CMOS-compatible SiPh platforms [18,19]. The concept of μTP is schematically illustrated in Fig. 1. The devices are pre-fabricated on their native substrate (the source wafer) and subsequently printed on the target

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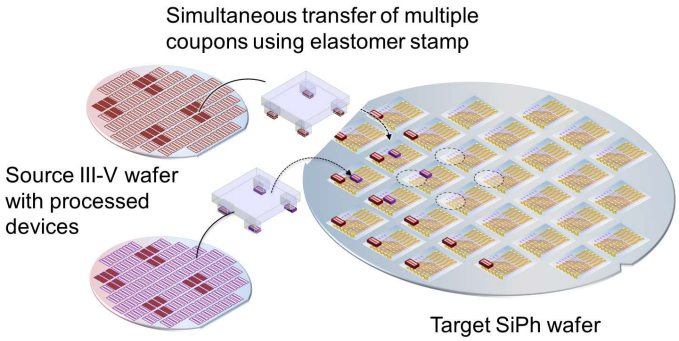
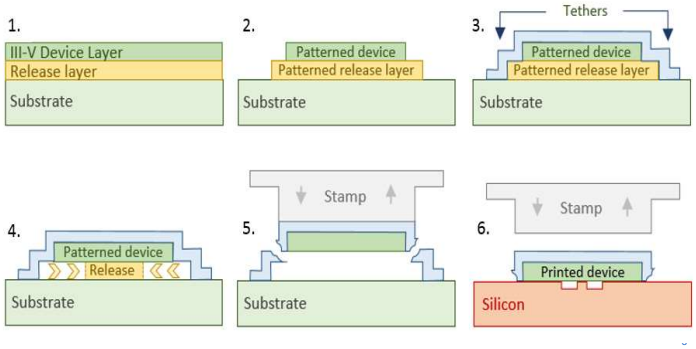
wafer, as shown in Fig. 1(a). Poly-dimethylsiloxane (PDMS) stamps with a single post (or post array) are used to print the device(s) from the source to the target wafer. µTP allows for the heterogeneous integration of devices from different source substrates on the same target substrate. Furthermore, since the source devices are prefabricated, processing on the target wafer is significantly simplified, and yield of the integration process can be improved by testing the devices on the source wafer before printing.



(a) Wafer-scale heterogeneous integration of III-V devices in a parallel manner on 200 or 300mm SiPh wafers using PDMS stamps with a post array. Reproduced with permission from J.Zhang *et al.*, APL Photonics 4, 110803 (2019); licensed under a Creative Commons Attribution (CC BY) license.



(b) µTP steps include pre-fabrication of III-V devices in dense arrays on their native substrate and micro-transfer printing onto a Si substrate. Reproduced with permission from G. Roelkens *et al.*, in 2018 IEEE Optical Interconnects Conference (OI) (IEEE, USA, 2018), pp. 13–14. Copyright 2011 IEEE.

Fig. 1. Micro-transfer printing concept.

The µTP steps are shown in more detail in Fig. 1(b). Processing of the source wafer starts from a stack that includes the III-V device layer(s), a sacrificial release layer, and a substrate (Fig. 1(b), step 1). The sacrificial release layer, e.g. InGaAs or InAlAs in the case of InP-based epitaxy, is added such that it can be selectively etched and the resulting source devices are printable. The devices are patterned on the III-V source wafer (Fig. 1(b), step 2) and encapsulated with photoresist or a dielectric layer, which is patterned with local openings to expose the release layer (Fig. 1(b), step 3). The tethers defined this way will help to support the coupons before printing but are designed to break easily and cleanly when picking up the coupon during printing. After the definition of the tethers, the release layer is selectively etched to undercut the devices (Fig. 1(b), step 4), e.g. by using cold $FeCl_3$:H_2O in the case of InP-based epitaxy [20]. After step 4, the devices are ready for transfer printing. They are picked up by laminating a PDMS

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stamp to the device or device array of interest on the source wafer and moving the stamp upwards at high retraction velocity (Fig. 1(b), step 5). As mentioned before, this step will pick up the coupon(s) and result in a clean break of the tethers originally holding the coupon(s) in place. Finally, the picked-up device(s) are automatically aligned to the printing site on the target wafer using fiducial markers and printed onto the target Si PICs through a sequence of motions of laminating the stamp on the target, applying shear displacement and slowly retracting the stamp (Fig. 1(b), step 6). While this paper focuses on the printing of III-V devices, it should be noted that the μTP concept is not limited to only III-V materials. Other potential source coupons include magneto-optic material films such as Ce:YIG (required for optical isolators/circulators) [21], $LiNbO_3$ and PZT (to implement modulators) [22,23], electronic chiplets (both control and high-speed) [24], etc.

3. Transfer printing of prefabricated III-V devices on an advanced SiPh platform

SiPh platforms are evolving rapidly to include more functionalities and enable more complex circuits while maintaining CMOS-compatibility. As a result, advanced SiPh platforms, such as imec's iSiPP50G, expand the library of available components beyond the passive structures that can be defined in the Si device layer (waveguides, grating couplers, MMIs, etc.) [25] by introducing heaters for tuning, Ge photodetectors, doped-silicon modulators, SiGe electro-absorption modulators, one or more metal layer(s), etc. Consequently, in more complicated SiPh platforms, a thick and complex back-end will be present on top of the functional layer. Hence, access to the waveguide for tight heterogeneous integration is not trivial [1]. A solution to allow for µTP of III-V devices on top of the waveguides can be found by incorporating recesses in the process flow. The recess will serve as a window in the back-end stack, reaching down to the functional Si waveguide layer. Fig. 2 illustrates how III-V devices can be printed in these recesses.

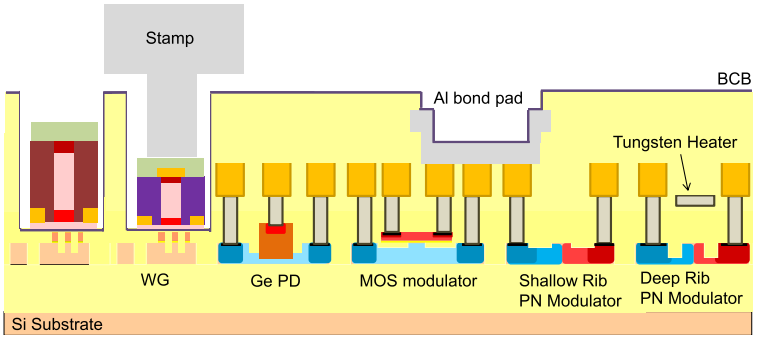

Fig. 2. Platform overview of an advanced SiPh platform (e.g. imec's iSiPP50G) with intimately integrated µTP III-V devices. Reproduced with permission from J. Zhang *et al.*, in *2022 IEEE 72nd Electronic Components and Technology Conference (ECTC)* (CA, USA, 2022), pp. 441-445. Copyright 2023 IEEE.

The process flow of integrating III-V devices on advanced SiPh platforms using µTP is illustrated in more detail in Fig. 3. The devices described in this paper were implemented on imec's iSiPP50G advanced SiPh platform, however, it should be possible to employ a similar strategy for other advanced SiPh platforms [26–28]. Processing starts from a finished SiPh wafer (or single chip) where a recess is present on top of the waveguide on which the III-V coupon needs to be printed (Fig. 3, step a). The recess does not yet reach down to the Si layer, so in the first step, a combination of RIE dry etching and buffered HF wet cleaning is applied to expose the Si device layer (Fig. 3, step b). Subsequently, a thin layer of divinylsiloxane-bisbenzocyclobutene

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(DVS-BCB) is deposited on the target wafer through spray-coating to achieve strong bonding of the printed coupon to the target substrate (Fig. 3, step c). In this work, the spray-coating of DVS-BCB films was carried out at EV group. Preparing the source wafer and picking up the coupon using a PDMS stamp (Fig. 3, step d) is identical to what was described in Fig. 1(b). In the next step, the coupon will be printed in the recess followed by a slow retraction of the stamp (Fig. 3, step e). Since the coupons are prefabricated on the source wafer, only a limited number of post-processing steps are still required. First, the encapsulation layer (e.g photoresist) is removed using RIE oxygen plasma, along with the part of the thin DVS-BCB layer that is not covered by the transfer-printed coupon (Fig. 3, step f). Secondly, the metal contacts of the coupons need to be made accessible. For the drawn device, the p-contact is already opened up after the photoresist removal and vias are defined to reach the n-contacts (Fig. 3, step g). Finally, one or more metallization steps are required to provide electrical contact between the printed device and the target advanced SiPh chip.

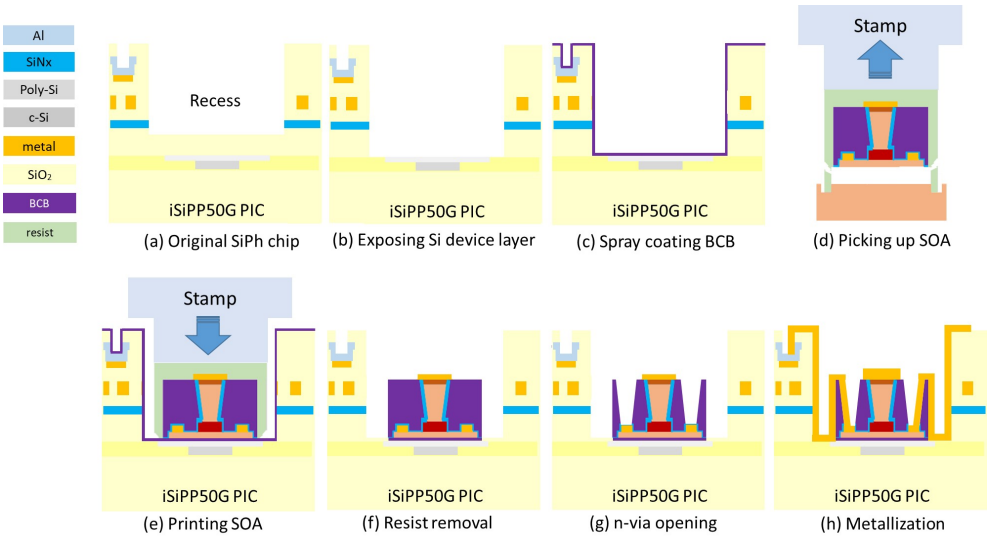

Fig. 3. Process flow for μTP of III-V devices on an advanced SiPh platform.

4. Lossless Si MZI switch with co-integrated III-V amplifier

High-speed switches are one of the key building blocks in data centers and are nowadays often implemented in the electrical domain. In this section, the fabrication and performance of C-band lossless high-speed optical switches will be discussed [29]. The fabricated devices rely on a heterogeneous approach where the switching is implemented on imec's iSiPP50G platform while the optical gain is provided using μTP of III-V SOAs following the procedure discussed in section 3. The switching functionality implemented on the SiPh chip uses a 1×2 MZI configuration with a carrier-injection-based pin-diode phase shifter (500 μm) in both MZI arms. These carrier-injection-based switches can operate at ns switching speeds with high energy efficiency and low insertion losses [30]. More advanced routing networks can be implemented by cascading multiple of these 1×2 switches. To compensate for the accumulated losses in multi-stage switches and/or the coupling loss between fiber and chip, SOAs can be integrated at the outputs of the switch(es) using μTP. Furthermore, the introduction of these SOAs improves the extinction ratio of the switch, resulting in reduced crosstalk between the output channels. In the remainder of this section, we will discuss the fabrication and characterization of a C-band

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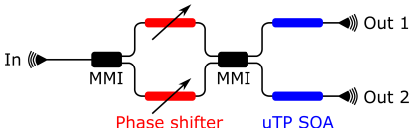
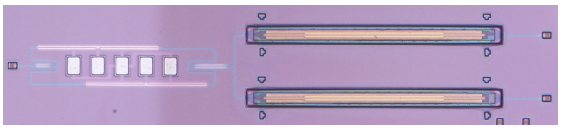
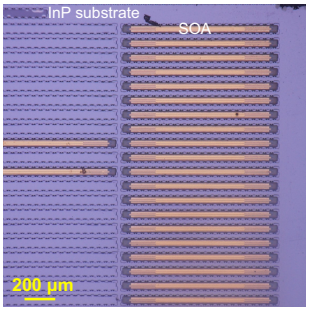
single-stage carrier-injection based 1×2 MZI, with a μTP III-V SOA present at both its outputs (Fig. 4).



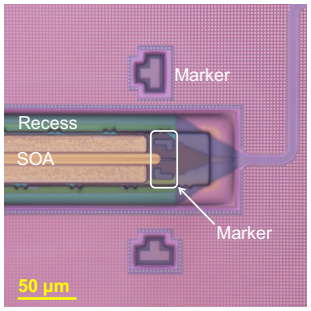
(a) Schematic overview.



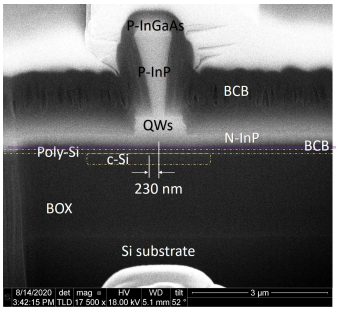
(b) Silicon photonics chip before metallization step.



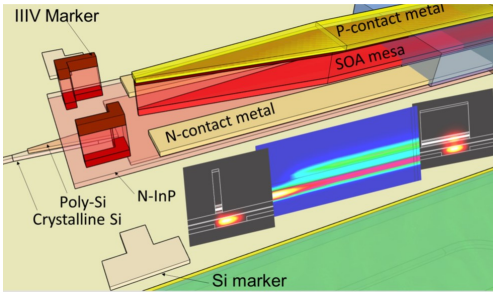
(c) Source wafer with pre-fabricated III-V SOA arrays.



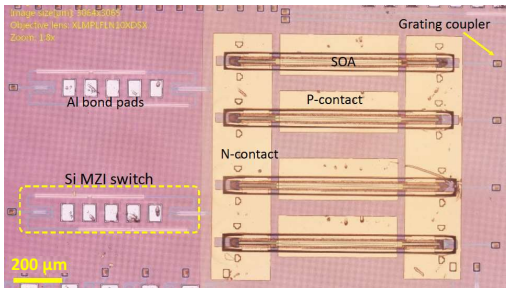
(d) Transfer-printed SOA in the recess of an advanced SiPh chip.



(e) Cross section of the III-V taper close to the taper tip.



(f) Schematic layout of the III-V/Si taper structure.



(g) SiPh chip after metallization step.

Fig. 4. Lossless high-speed III-V-on-Si MZI based switch. (g) is reproduced with permission from J. Zhang *et al.*, in *2022 IEEE 72nd Electronic Components and Technology Conference (ECTC)* (CA, USA, 2022), pp. 441-445. Copyright 2023 IEEE.

Fabrication of these lossless, high-speed switches starts from the design and fabrication of a SiPh chip. At the amplifier region of the SiPh chip, a waveguide is constructed using a combination of the standard 220 nm thick crystalline-Si (c-Si) waveguide layer and the 160 nm thick poly-Si layer available on top of the c-Si layer. Markers are defined at both sides of the amplifier region to aid the alignment of the coupon to the silicon waveguide during micro-transfer printing. Furthermore, tapers are present at both sides of the amplifier region to efficiently couple light from the SiPh chip to the active amplifier region and vice versa. These tapers consist of two sections. First, the light is coupled from the standard 220 nm thick c-Si waveguide to the 380 nm thick poly-on-crystalline-Si waveguide. Secondly, the taper couples the light from the 380 nm thick Si waveguide to the III-V active region while providing sufficient robustness to misalignment caused by the printing process. To allow for the printing of the SOA on top of the 380 nm thick Si waveguide, 80 μm × 1050 μm recesses were defined and opened up following the procedure discussed in section 3. The SOA coupons used in this demonstrator are 45 μm wide and 950 μm long, comprising a 500 μm straight waveguide section and a 225 μm long taper on both sides. Detailed information on the SOA design can be found in section 2.5.2 of ref. [31]. A

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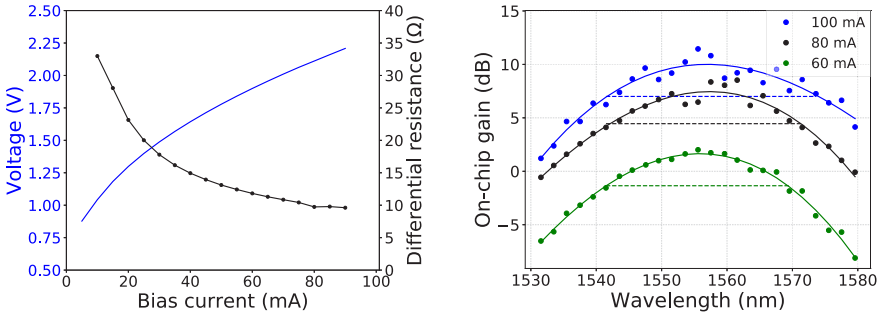
microscope image of the InP source chip containing these pre-fabricated III-V SOAs is shown in Fig. 4(c). To improve the adhesion of the SOA to the Si waveguide, a 75 nm thick DVS-BCB layer was spray-coated and soft-baked shortly at 150 °C. Subsequently, the SOAs were printed using an X-Celeprint μTP-100 tool adopting a single post PDMS-stamp of 40 μm × 1200 μm. Figure 4(d) shows a zoomed-in image of the SiPh chip after printing the SOA in the recess. This image clearly shows two sets of alignment markers that are used to achieve accurate printing, one pair on the SiPh chip and one pair on the SOA. A cross-section was made on the final chip using focused ion beam (FIB), resulting in the SEM image depicted in Fig. 4(e) (close to the III-V taper tip). The cross-section shows a poly-on-c-Si waveguide, implemented on the SiPh chip, which is covered by a thin layer of BCB on top of which the printed C-band III-V SOA coupon resides. Figure 4(f) depicts the proposed III-V/Si taper structure, while the inset images show the fundamental TE mode propagating through this taper structure. Furthermore, the FIB cross section (Fig. 4(e)) shows that for the demonstrated device, there is a 230 nm lateral misalignment.

A vertical setup consisting of a temperature-controlled stage, two fiber probes, a set of DC probes and a RF probe was used to characterize the resulting device. A Santec-510 tunable laser was used to inject continuous wave (CW) light into the chip while an HP power meter was used to measure the output coupled optical power. Furthermore, two Keithley 2401 power sources were used, one to bias the Si MZI switch and the other to bias the III-V amplifier in front of the monitored output. This setup was used to characterize the optical gain of the transfer printed SOAs at 20 ° C.

As shown in Fig. 5(a), the micro-transfer-printed SOA exhibits a differential resistance of 10 Ω at 100 mA. To find the gain that is introduced by the amplifier, the MZI switch loss should be subtracted from the on-chip transmission measurement. The MZI switch is biased at 0.9 V to achieve maximum transmission with an insertion loss of 1.4 dB around 1550 nm [30]. First, the wavelength of the tunable laser was set to 1560 nm and the bias current applied to the integrated SOA was swept up to 100 mA. The on-chip gain increases with increasing bias current and saturates at around 10 dB. This on-chip gain is derived from the measured gain by calibrating out the losses from the setup, grating couplers and the Si MZI switch. Subsequently, the gain spectrum of the device was obtained by measuring the on-chip gain over the wavelength range from 1530 nm to 1580 nm, while keeping the on-chip input power at −20 dBm. As shown in Fig. 5(b), the 3 dB optical gain bandwidth is around 25 nm at 60 mA and increases to over 30 nm at 100 mA.



(a) (b)

Fig. 5. Micro-transfer printed InP SOA: (a) I-V curve and differential resistance. (b) On-chip gain spectra for different bias currents (Reproduced with permission from J. Zhang *et al.*, in *2022 IEEE 72nd Electronic Components and Technology Conference (ECTC)* (CA, USA, 2022), pp. 441-445. Copyright 2023 IEEE.).

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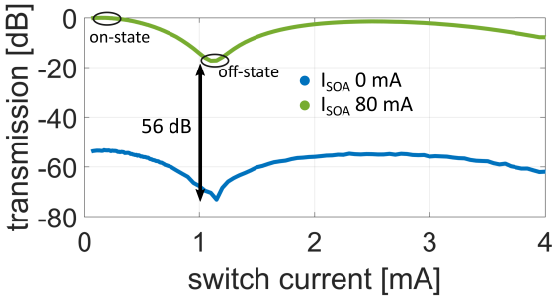
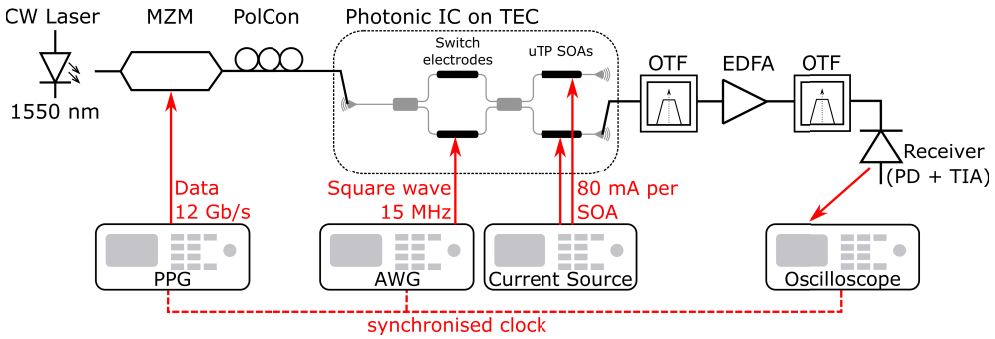
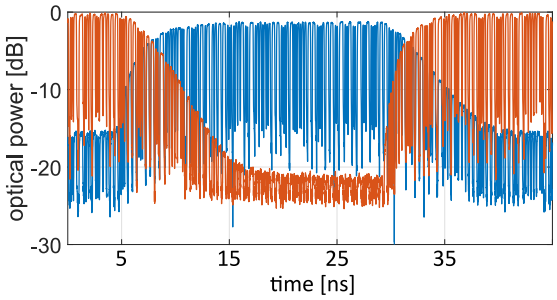


Fig. 6. Optical transmission versus the Si MZI switch bias current for different SOA currents of 0 mA and 80 mA. 56 dB cross-talk reduction is achieved when the SOA is deactivated. Reproduced with permission from J. Zhang *et al.*, in *2022 IEEE 72nd Electronic Components and Technology Conference (ECTC)* (CA, USA, 2022), pp. 441-445. Copyright 2023 IEEE.



(a)



(b)

Fig. 7. (a) Measurement setup for the characterization of the Si MZI switch with co-integrated SOAs. (b) Optical transient response of the system when routing a 12 Gb/s data stream through switching the MZI but not the booster SOAs.

To characterize the switching behavior of the resulting integrated circuit, the current applied to one of the switching arms was swept from 0 to 4 mA while the SOA was biased at different currents. The wavelength of the laser source was fixed at 1550 nm and the output power was adjusted to have 0 dBm optical power launched into the Si MZI switch. Figure 6 shows the recorded transmission at one output port. The spectra were calibrated to the maximum transmission when the SOA is biased at 80 mA. The maximum and minimum transmission, corresponding to switch currents of 0.2 and 1.1 mA, are defined to be the on-state and off-state, respectively. As the power splitting ratios of the 2 multi-mode interferometer (MMI) splitter/combiner, which is

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connected to the amplifiers is slightly unbalanced and an additional loss (maximally −1.4 dB) will be inherently introduced to one of the arms when the phase shifter is biased, a fraction of the light still leaks into the branch which is in the off-state, resulting in a −20 dB optical cross-talk. However, this cross-talk can be heavily reduced by lowering the SOA bias current of the unused output port. This is due to the reduction of the optical gain and even absorption at low bias levels of the integrated amplifier. 56 dB reduction in crosstalk is achieved when the unused SOA is deactivated by setting its bias to 0 mA. Subsequently, high-speed operation was tested by routing a 12 Gb/s data stream (carrier at 1550 nm) through the MZI switch and driving the switch with a 15 MHz square wave electrical signal. As shown in Fig. 7(a), the high-speed data stream was generated with an external modulator driven by a pulse-pattern generator (PPG) and is injected into the switch via the input grating coupler. During the characterization, the III-V amplifiers were biased at 80 mA. Figure 7(b) shows the detected optical signal at the two output ports of the integrated circuit using a high-speed optical receiver. It is worth noticing that the rise and fall transients of these carrier-injection based switches are unbalanced. Higher degrees of symmetry in switching times can be achieved with pre-emphasis based driving signals. Given the low loss of the Si MZI switch, the demonstrated III-V-on-Si integrated circuit can easily achieve loss-less operation. Furthermore, the crosstalk of the data in its off-state would be heavily reduced compared to Fig. 7(b) when the SOAs are switched off at the correct time slots.

5. SiPh transmitter with integrated III-V/Si widely tunable laser

Optical lane rate requirements are increasing rapidly, thereby pushing transmission schemes from intensity modulation / direct detection (IM/DD) to coherent. Most of the essential building blocks - modulation, detection, and optical 90° hybrid - can be easily implemented in advanced SiPh platforms. However, a laser is missing at the input of the modulator and as a local oscillator (LO) at the coherent receiver side. These key building blocks can be added using μTP of pre-fabricated SOAs on the advanced SiPh platform, as discussed in the previous sections. Figure 8 illustrates how a III-V-on-Si coherent transceiver looks like. It has one optical output (the modulator output) and one optical input (the signal port of a coherent receiver). Additionally, it includes a µTP III-V SOA that provides gain and is used to construct a laser where the lasing cavity is defined in the SiPh circuit on which the SOA is printed. This laser is fed both to the coherent modulator and the LO port of the coherent receiver through a power splitter.

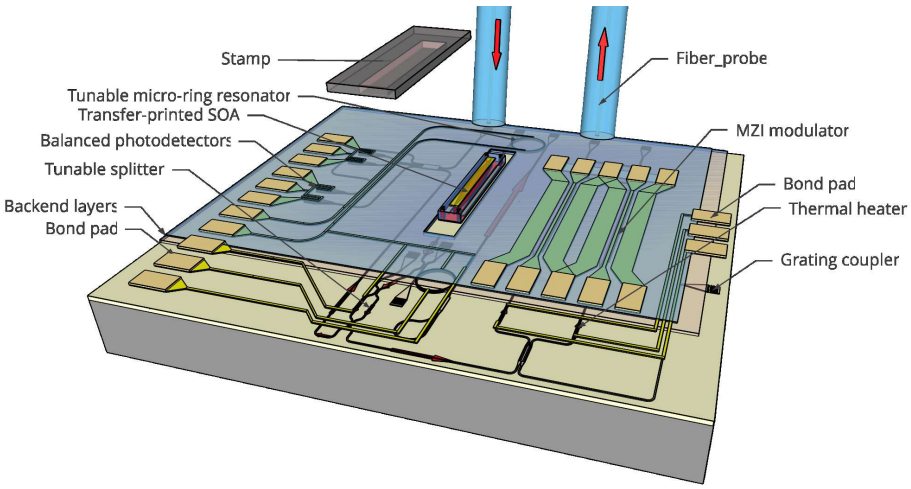

Fig. 8. Integrated coherent transceiver with micro-transfer-printed III-V/Si widely tunable laser.

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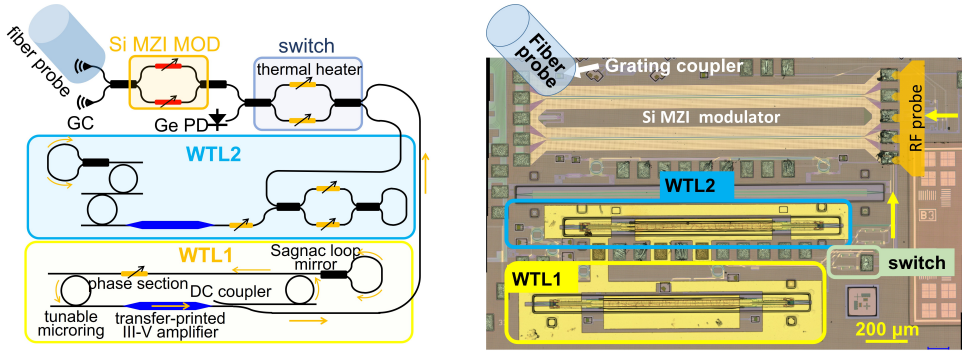
The circuit shown in Fig. 9(a) was designed as a first step towards such a coherent transceiver. It includes two widely tunable lasers (WTLs) with one as backup, a Mach-Zehnder interferometric modulator (MZM), and a tunable switch to send part of the unmodulated laser light to a monitor PD [32]. The main laser source, WTL1, has a 3.4 mm long ring cavity incorporating a pair of add-drop micro-ring resonators with slightly different bend radii (25 and 27 µm). The lasing wavelength of this laser can be tuned over 40 nm in the C-band using integrated microheaters to thermally control the resonance wavelength of both rings, and consequently the Vernier profile of the combination of the two micro-rings. A phase section is included in the ring cavity to adjust the roundtrip phase condition of the laser. Adding a Sagnac loop mirror, which can be implemented by interconnecting the two outputs of a MMI based 3 dB splitter, to one of the unused micro-ring ports will introduce explicit coupling from clockwise to counter-clockwise propagating modes, resulting in unidirectional propagation in the cavity [33]. A directional coupler with an expected cross-coupling ratio of 30% is used to couple out the generated laser light. WLT2 is a backup laser source. It has a linear cavity, formed by connecting the microrings, the gain section between a Sagnac loop mirror, and a MZI-based tunable reflector. The microrings and the Sagnac loop mirror used in this laser are exactly the same as those in WL1. The output ports of the two lasers are respectively connected to the two input ports of a MZI-based switch. By tuning the integrated micro-heater(s), we can select the laser source and maximize the optical power injected into the following Si MZM. In this demonstration, WLT1 is used as the light source while WTL2 was not in operation. Finally, a printing site is implemented, on top of which the prefabricated III-V SOA, with 1.15 mm long active region, can be printed. At the printing site, the crystalline Si (c-Si) waveguide is tapered out to a 220 nm thick, 3 µm wide waveguide, and overlaid with a 160 nm thick poly-Si slab. A combination of the alignment tolerant tapers, defined in the c-Si/poly-Si and in the III-V coupons, as shown in Fig. 4(f), will ensure over 90% coupling between the SiPh laser cavity and the III-V gain medium. Following the fabrication of the SiPh integrated circuit at imec, the processing steps described in Fig. 3 were performed. A recess was defined and etched back down to the c-Si/Poly-Si waveguide layer. For the discussed transmitter, we opened up a 80 µm by 1335 µm recess on top of the printing site, by using a combination of reactive ion etching (RIE) and a short BHF dip, resulting in a final recess depth of 3.6 µm. Subsequently, a thin DVS-BCB layer (< 50 nm) was spray coated on the target SiPh chip at EV Group, before µTP the prefabricated III-V SOA coupons using an X-Celeprint µTP-100 lab-scale printer. Finally, a single metal layer was deposited and patterned to connect the device to the target SiPh chip and enable biasing of the SOA. Figure 9(b) shows the resulting III-V-on-Si integration PIC.



(a) Schematic of the optical transmitter with integrated widely tunable lasers.

(b) Resulting III-V-on-Si integrated circuits.

Fig. 9. Integrated transmitter with widely tunable laser.

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Prior to the evaluation of the high-speed performance of the integrated transmitter, the WTL1 was characterized as a standalone device. Both the assessment of the laser performance as well as the characterization of the high-speed transmitter were done using a temperature-controlled stage set to 20 ° C. Figure 10 presents the results of these measurements. First, Fig. 10(a) shows the LIV curves where the measured output optical power was calculated back to the power available in the waveguide at the laser output port. To avoid any damage to the transfer-printed lasers, a maximum bias current of 130 mA was used in the following measurements. The LIV curves were obtained after setting the WTL1 to single-mode operation at a wavelength of 1553 nm. The differential resistance and the waveguide-coupled power are found to be around 6.5 Ω and approximately 2 mW (or equivalently 3 dBm), respectively, at 130 mA SOA bias current. To improve the output power, an III-V-on-Si booster can be co-integrated with the WTL [34,35]. Additionally, Fig. 10(a) shows that for this 1553nm wavelength setting the lasing threshold is just below 100 mA. Dips in the LI curve, e.g. around 115 and 125 mA, are due to the occurrence of mode hopping. As aforementioned, the WTL1 can be tuned quasi-continuously over a 40 nm wide wavelength range around 1550 nm by adopting the Vernier effect between the two microrings with slightly different radii. Thermal tuning is done by simultaneously optimizing the microheaters present at each ring and the phase section. Figure 10(b) shows the tuning capabilities of the WTL1 when only one of the microrings is tuned together with the phase section. The resulting tuning is discrete with the tuning step corresponding to the free spectral range (FSR) of the untuned ring, which is nearly 4 nm for the fabricated device. In this way, discrete tuning over more than 40 nm was demonstrated. To tune the WTL1 continuously and achieve full wavelength tuning coverage, both microrings need to be adjusted together with the phase section, as shown in Fig. 10(c).

Next, the high-speed characterization of the integrated transmitter depicted in Fig. 9, will be discussed while varying the operation wavelength of the integrated laser over its tuning range. The setup used for these high-speed link experiments is described in Fig. 11. The integrated transmitter was placed on a temperature-controlled stage set to 20 °C, and includes the aforementioned WTL1 set to the desired wavelength, a tunable splitter to configure the portion of the laser output to be modulated, and a traveling wave MZM with on-chip terminations. The MZM consists of two arms, each containing a 1.5 mm long Si carrier-depletion phase modulator, and allows for single-drive as well as push-pull operation. It also includes a thermal phase shifter in each of the arms to set the MZM operation point. For the results discussed in the remainder of this section, the MZM was operated in single-drive mode. An arbitrary waveform generator (Keysight M8196A, 92 GSa/s) was used to generate a data signal and a clock signal. The data signal was first amplified (+14 dB) and combined with a DC bias (V_{PN}) using a bias tee, before feeding it to the MZM. While no RF signal was injected into the second arm of the MZM, the phase modulator still required biasing to the same DC level V_{PN}. To get the correct signals at the RF pads of the MZM, a 40 GHz GSGSG RF probe was used where one of the RF arms was connected to the RF signal plus bias while the other arm was directly connected to a DC power supply. Furthermore, V_{MZI} was tuned to set the MZM to its correct working point using a thermal phase shifter. The modulated light was coupled out via a grating coupler and sent to a 10/90 splitter, where 10 % of the light that is coupled out of the integrated transmitter chip is monitored by a power meter and 90 % is injected into an Erbium-doped fiber amplifier (EDFA) set to 10 dBm output power. The amplified modulated signal is then passed through a tunable optical bandpass filter (OTF), and launched into an optical receiver, after tapping off 1 % of the light to analyze the optical spectrum. The optical receiver is a combination of a high-speed photodetector (Discovery DSC10H) and a broadband RF amplifier (+22 dB), and the optical input at the receiver is around 3.7 dBm. The output signal is analyzed using a sampling scope (Keysight 86100C) by also feeding it with the clock signal generated by the AWG.

Starting from this setup, we measured both the effect of varying data rate (with the wavelength set to 1551.4 nm) and the effect of varying lasing wavelength (with the data rate fixed at 40 Gbps).

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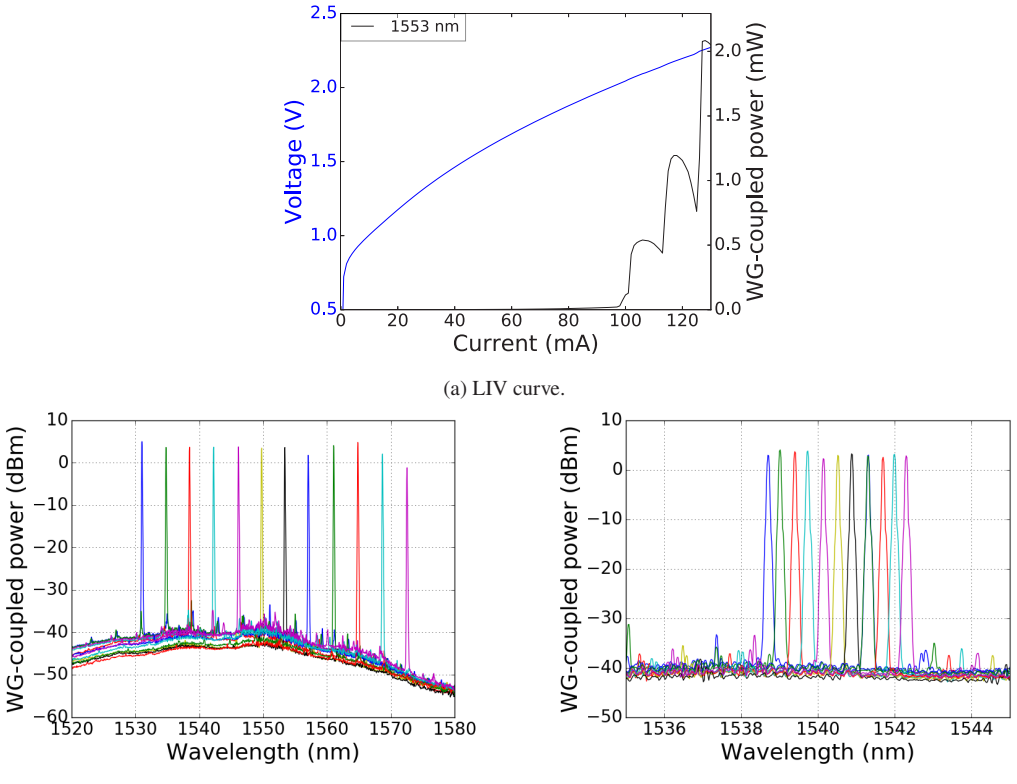

(a) LIV curve.

(b) Coarse wavelength tuning.

(c) Fine wavelength tuning.

Fig. 10. Widely tunable laser performance at 20°C. Reproduced with permission from J. Zhang *et al.*, in *2022 Optical Fiber Communications Conference and Exhibition (OFC)* (CA, USA, 2022), Tu2D.2. Optica Publishing Group, 2022.

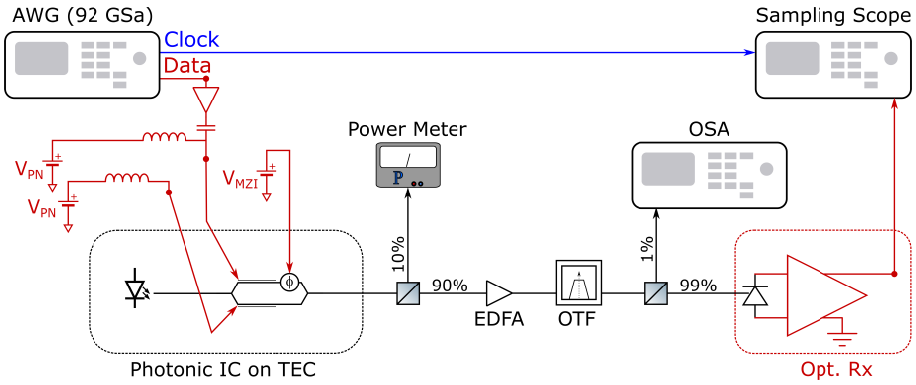

Fig. 11. Measurement setup for high-speed NRZ transmission.

In all scenarios, a 2^9-1 long pseudo random binary sequence non-return-to-zero (NRZ) signal with Gaussian-shaped pulses was transmitted over the link and the SNR of the eye diagram was monitored. Finally, the bit error rate (BER) was calculated based on these measured SNR values. Figure 12 shows the effect of varying the bit rate on the link BER. It is important to note that in this paper no equalization was used, hence, the BER-values are a combined effect of the BER of

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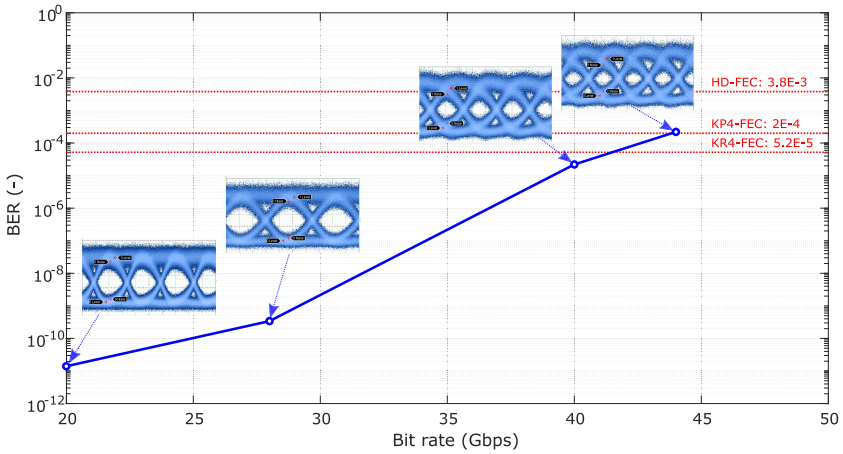

Fig. 12. Bit error rate as a function of the bit rate for NRZ signals at 1551.4nm.

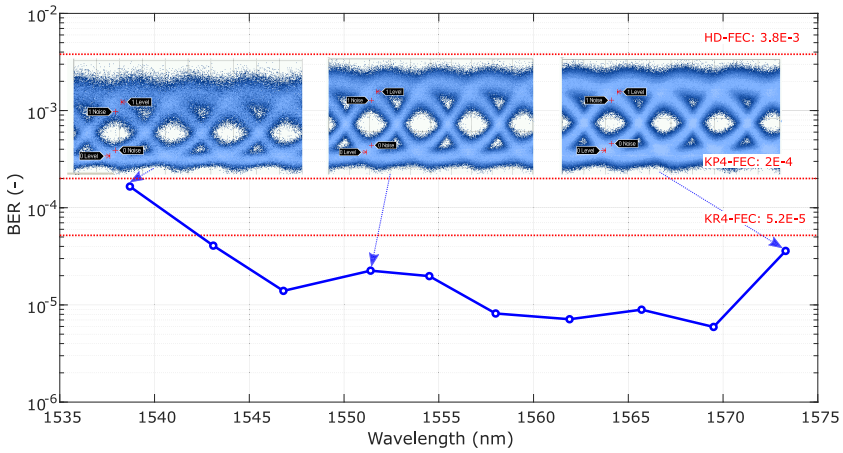

Fig. 13. Bit error rate as a function of the wavelength for 40 Gbps NRZ signals.

the optical link and the imperfections of the electrical back-to-back link (AWG, RF amplifiers, etc.). This electrical back-to-back link can be defined as the purely electrical connection from the AWG output to the sampling scope input when the cable connected to RF input of the modulator is instead directly fed into the sampling scope. At 40 Gbps, the electrical back-to-back was characterized and it was found to result in a BER of approximately 1.8×10^{-9}. This sets a lower limit to the BER that can be achieved for the optical link at 40 Gbps. It is shown in Fig. 12 that the NRZ eye remains open and that the BER increases from 1.4×10^{-11} to 2.2×10^{-4} when increasing the bit rate from 20 to 44 Gbps NRZ. Finally, we measured how the link performance changes over the tuning range of the WTL1 given a 40 Gbps NRZ data stream. As mentioned before, a lower boundary of this performance is a BER of 1.8×10^{-9} due to the absence of equalization of the electrical back-to-back link. The resulting BER is presented in Fig. 13 and it indicates that the integrated transmitter is able to operate below KP4 forward error correction (FEC) over 35 nm for 40 Gbps NRZ streams. It should be noted that the degraded performance at low and/or high wavelengths can partially be caused by the limited wavelength operation window of the EDFA.

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6. Conclusion

Silicon photonics is a key enabling technology that relies on CMOS compatible processing to implement compact, high complexity photonic integrated circuits at a low cost with a high yield. State of the art SiPh platforms include a wide variety of high-performance readily available components. However, these platforms still lack crucial functionalities, such as optical amplification and isolation, that can not be implemented natively on SOI. Heterogeneous integration through flip-chip and multi-die-to-wafer bonding techniques have been proposed but suffer from respectively low throughput and the need for substantial modifications to the well-established SiPh back-end process flow. In this paper, we discuss micro-transfer printing as a heterogeneous integration approach that benefits from minimal disruption to the process flow, high throughput, improved yield through testing prefabricated devices, etc. Furthermore, this paper explains how µTP can be realized in the advanced SiPh platforms where the back-end first needs to be removed locally to access the waveguide layer to achieve tight integration between the Si waveguide and the printed devices. While the micro-transfer printing approach is very promising, there is still a lot of work ongoing to expand the selection of printable devices and materials, to improve the integrated device performance and yield, and to scale up the technology to 200 and 300 mm wafers. In the second part of the paper, two devices adopting µTP of prefabricated III-V SOAs on imec's advanced SiPh platform iSiPP50G were discussed. First, lossless high-speed C-band switches were demonstrated. Here the switching is done using an MZI with carrier-injection pin-diode based phase shifters readily available on the SiPh platform. Prefabricated SOAs were micro-transfer printed in predefined recesses at the switch outputs to achieve lossless operation and improve the extinction ratio of the switch states. Secondly, a SiPh transmitter with an integrated III-V/Si widely tunable laser was demonstrated. The on-chip widely tunable laser is based on a ring cavity architecture, with a µTP III-V SOA providing the required gain, and realizes a quasi-continuous tuning range of more than 40 nm. Together with the co-integrated doped-Si based MZM, 40 Gbps NRZ communication has been demonstrated over a tuning range of nearly 35 nm.

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Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

References

1. S. Y. Siew, B. Li, F. Gao, *et al.*, "Review of silicon photonics technology and platform development," J. Lightwave Technol. **39**(13), 4374–4389 (2021).
2. D. Colucci, M. Baryshnikova, Y. Shi, *et al.*, "Unique design approach to realize an O-band laser monolithically integrated on 300 mm Si substrate by nano-ridge engineering," Opt. Express **30**(8), 13510–13521 (2022).
3. B. Shi, Y. Han, Q. Li, *et al.*, "1.55-μm Lasers Epitaxially Grown on Silicon," IEEE J. Sel. Top. Quantum Electron. **25**(6), 1–11 (2019).
4. J.-S. Park, M. Tang, S. Chen, *et al.*, "Heteroepitaxial growth of III-V semiconductors on silicon," Crystals **10**(12), 1163 (2020).
5. B. Kunert, R. Alcotte, Y. Mols, *et al.*, "Application of an sb surfactant in ingaas nano-ridge engineering on 300 mm silicon substrates," Cryst. Growth Des. **21**(3), 1657–1665 (2021).
6. V. Cao, J.-S. Park, M. Tang, *et al.*, "Recent progress of quantum dot lasers monolithically integrated on Si platform," Front. Phys. **10**, 839953 (2022).
7. T. Zhou, M. Tang, G. Xiang, *et al.*, "Continuous-wave quantum dot photonic crystal lasers grown on on-axis si (001)," Nat. Commun. **11**(1), 1 (2020).
8. Y. Shi, B. Kunert, Y. D. Koninck, *et al.*, "Novel adiabatic coupler for III-V nano-ridge laser grown on a Si photonics platform," Opt. Express **27**(26), 37781–37794 (2019).
9. C. Mitchell, R. Schachler, K. Li, *et al.*, "Tooling and procedures for hybrid integration of lasers by flip-chip technology," (2020).
10. T. Matsumoto, T. Kurahashi, R. Konoike, *et al.*, "Hybrid-integration of soa on silicon photonics platform based on flip-chip bonding," J. Lightwave Technol. **37**(2), 307–313 (2019).

Optics EXPRESS

11. X. Luo, Y. Cao, J. Song, *et al.*, "High-throughput multiple dies-to-wafer bonding technology and III/V-on-Si hybrid lasers for heterogeneous integration of optoelectronic integrated circuits," Front. Mater. **2**, 28 (2015).
12. M. Cooke, "Silicon photonics and III-V integration," Semiconductor TODAY **11**, 80 (2016).
13. B. Szelag, K. Hassan, L. Adelmini, *et al.*, "Hybrid III–V/silicon technology for laser integration on a 200-mm fully CMOS-compatible silicon photonics platform," IEEE J. Sel. Top. Quantum Electron. **25**(5), 1–10 (2019).
14. B. Corbett, R. Loi, J. O'Callaghan, *et al.*, "Chapter three - transfer printing for silicon photonics," in *Silicon Photonics*, vol. 99 of *Semiconductors and Semimetals* (Elsevier, 2018), pp. 43–70.
15. Y. Sun and J. A. Rogers, "Fabricating semiconductor nano/microwires and transfer printing ordered arrays of them onto plastic substrates," Nano Lett. **4**(10), 1953–1959 (2004).
16. D. Gomez, K. Ghosal, M. A. Meitl, *et al.*, "Process capability and elastomer stamp lifetime in micro transfer printing," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, (2016), pp. 680–687.
17. B. H. Dean, D. L. Aronstein, S. J. Smith, *et al.*, "Micro transfer printing for micro assembly of heterogeneous integrated compound semiconductor components," in *CS MANTECH Conference*, (May 9-12, 2022).
18. J. Zhang, G. Muliuk, J. Juvert, *et al.*, "III-V-on-Si photonic integrated circuits realized using micro-transfer-printing," APL Photonics **4**(11), 110803 (2019).
19. B. Corbett, R. Loi, W. Zhou, *et al.*, "Transfer print techniques for heterogeneous integration of photonic components," Prog. Quantum Electron. **52**, 1–17 (2017).
20. J. O'Callaghan, R. Loi, E. Mura, *et al.*, "Comparison of ingaas and inalas sacrificial layers for release of inp-based devices," Opt. Mater. Express **7**(12), 4408 (2017).
21. D. Minemura, R. Kou, Y. Sutoh, *et al.*, "Compact magneto-optical isolator by μ-transfer printing of magneto-optical single-crystal film on silicon waveguides," Opt. Express **31**(17), 27821–27829 (2023).
22. T. Vanackere, T. Vandekerckhove, L. Bogaert, *et al.*, "Heterogeneous integration of a high-speed lithium niobate modulator on silicon nitride using micro-transfer printing," APL Photonics **8**(8), 086102 (2023).
23. I. Ansari, K. De Geest, J. De Witte, *et al.*, "PZT micro-transfer printing for photonic MEMS," in *2023 IEEE Photonics Conference (IPC)*, (Orlando, Florida, USA, 2023). Accepted.
24. R. Loi, P. Ramaswamy, A. Farrell, *et al.*, "Micro transfer printing of electronic integrated circuits on silicon photonics substrates," in *2022 European Conference on Integrated Optics (ECIO)*, (2022).
25. Europractice. https://europractice-ic.com/technologies/photonics/imec/.
26. E. Soltanian, G. Muliuk, S. Uvin, *et al.*, "Micro-transfer-printed narrow-linewidth III-V-on-Si double laser structure with a combined 110 nm tuning range," Opt. Express **30**(22), 39329–39339 (2022).
27. C. Op de Beeck, F. M. Mayor, S. Cuyvers, *et al.*, "III/V-on-lithium niobate amplifiers and lasers," Optica **8**(10), 1288–1289 (2021).
28. S. Cuyvers, B. Haq, G. Roelkens, *et al.*, "Mode-locked comb lasers for chip-scale spectroscopy," Compound Semiconductor **27**(7), 60–64 (2021).
29. J. Zhang, C. J. Krückel, B. Haq, *et al.*, "Lossless high-speed silicon photonic MZI switch with a micro-transfer-printed III-V amplifier," in *2022 IEEE 72nd Electronic Components and Technology Conference (ECTC)*, (2022), pp. 441–445.
30. C. J. Krückel, H. Becker, Y. Ban, *et al.*, "Towards maximum energy efficiency of carrier-injection-based silicon photonics," J. Lightwave Technol. **39**(9), 2931–2940 (2021).
31. Bahawal Haq, "III-V-on-Si SOAs and DFB/DBR lasers realised using micro-transfer printing," Ph.D. thesis, Ghent University (2021).
32. J. Zhang, E. Soltanian, B. Haq, *et al.*, "Integrated optical transmitter with micro-transfer-printed widely tunable III-V-on-Si laser," in *2022 Optical Fiber Communications Conference and Exhibition (OFC)*, (2022).
33. J. Zhang, Y. Li, S. Dhoore, *et al.*, "Unidirectional, widely-tunable and narrow-linewidth heterogeneously integrated III-V-on-silicon laser," Opt. Express **25**(6), 7092–7100 (2017).
34. G. Roelkens, J. Zhang, L. Bogaert, *et al.*, "Micro-Transfer Printing for Heterogeneous Si Photonic Integrated Circuits," IEEE J. Sel. Top. Quantum Electron. **29**(3: Photon. Elec. Co-Inte. and Ad), 1–14 (2023).
35. E. Soltanian, M. Billet, A. Hermans, *et al.*, "Micro-Transfer-Printed III-V-on-Si Semiconductor Optical Amplifiers with High Saturation Power," in *Annual Symposium of the IEEE Photonics Society Benelux Chapter*, vol. 26 (Eindhoven, Netherlands, 2022), pp. 201–204.