Comparison of Photonic to Plasmonic Mode Converters for Plasmonic Multiple-Input Devices

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***Abstract*—Implementing a compact optical integrated circuit by utilizing subwavelength plasmonic devices requires the design of compact and efficient photonic to plasmonic mode converters. Especially for plasmonic multiple-input devices such as logic gates that require multiple converters, the footprint can be largely penalized by the photonic waveguides, which should be considered in the design. In this work, we simulate and benchmark five photonic to plasmonic mode converter topologies for the application of multiple-input plasmonic devices. Our design includes both directional and end coupling schemes of plasmonic waveguide and Si photonic waveguides of wire and slot configurations. We optimize the performance of the converters considering the pitch mismatch between the photonic and plasmonic waveguides, the total footprint, and mode conversion efficiency.**

***Index Terms*—Coupling efficiency, mode conversion, plasmonics, waveguide.**

I. Introduction

PLASMONICS provides a means to overcome the diffraction limit of light, opening up possibilities for subwavelength optics and thereby demonstrating significant potential in the realm of compact optical integrated circuits. Recent advancements in plasmonics have led to the development of a diverse array of plasmonic devices that can generate, guide, manipulate, and detect surface plasmon polariton (SPP) signal in a sub-wavelength scale. Researchers have designed and demonstrated active and passive plasmonic components, such as plasmonic modulators [1], [2], logic gates [3], plasmonic detectors [4], [5], plasmonic interconnects [6], [7], and couplers [8], exploiting their unique features for nanophotonic computing.

A complete plasmonic computing system can be viewed in Fig. 1(a), where plasmonic phase modulators, driven by CMOS circuits, encode input data and feed a plasmonic logic gate. The design and operation of such a logic gate is presented in [9]. A plasmon detector converts the logic gate output to an electrical signal, which is received and processed by the CMOS circuit. At the beginning of the system, a plasmon source is needed to excite SPP. There are various SPP excitation methods, such as prism coupling [10], grating coupling using periodic corrugated structures [11], electronic excitation using tunneling electrons [12], etc. These methods have limited practical applications due to the requirement of bulky devices, challenging device integration, strict alignment requirements, or low excitation efficiencies. A photonic to plasmonic mode converter is an on-chip SPP excitation method that can generate coherent, efficient, and unidirectional SPP signal, and hence is applicable for plasmonic computing [13], [14].

Various photonic to plasmonic waveguide (WG) mode converters were previously investigated based on directional coupling [13], [15], [16] and mode size matching using tapered WGs [17], [18], [19]. Research on photonic to plasmonic mode converters mostly considered metal-insulator-metal (MIM) WG for mode coupling since MIM WG allows nm-scale mode confinement [20], [21], ensuring high-density device integration, which is the main appeal of plasmonics. For instance, a Si-MIM-Si directionally coupled structure consisting of a 400 nm-wide Si WG and a 100 nm-wide MIM WG was fabricated, and 60% of the input power was received at the output [13]. Moreover, a taper-funnel coupler between a 300 nm-wide Si WG and a 200 nm-wide MIM WG was demonstrated, and a coupling efficiency of 33% was achieved experimentally [18]. Ono et al. demonstrated 3D mode conversion from a Si wire WG of 400 $nm \times 200$ nm core size to a plasmonic slot WG of 50 $nm \times 20$ nm core size with a coupling loss of 1.7 dB [14].

All these works studied the coupling of isolated photonic and MIM WGs and primarily focused on coupling efficiency. For plasmonic devices like the logic gates [9], [22] that have multiple inputs and thus require multiple mode converters, the converter design should include considerations such as the WG pitch, the total footprint of the mode converter and the device along with the coupling efficiency. For example, the logic gate of Fig. 1(a) has ten input MIM WGs, which may require ten photonic WGs for SPP excitation. However, as shown in Fig. 1(b), the pitch of the photonic WG is significantly larger than that of the MIM WG. Due to the mismatch between the pitch of conventional Si WG and plasmonic MIM WG, coupling a single MIM WG to a Si WG will significantly increase the total footprint. Additionally, the photonic and plasmonic layers of Fig. 1(b) should be close enough to ensure strong mode coupling. However, for the proper functionality of plasmonic WGs/devices, these two layers should be spaced apart to prevent power coupling back to the photonic mode. These contradictory requirements should be balanced in a proper way, and they

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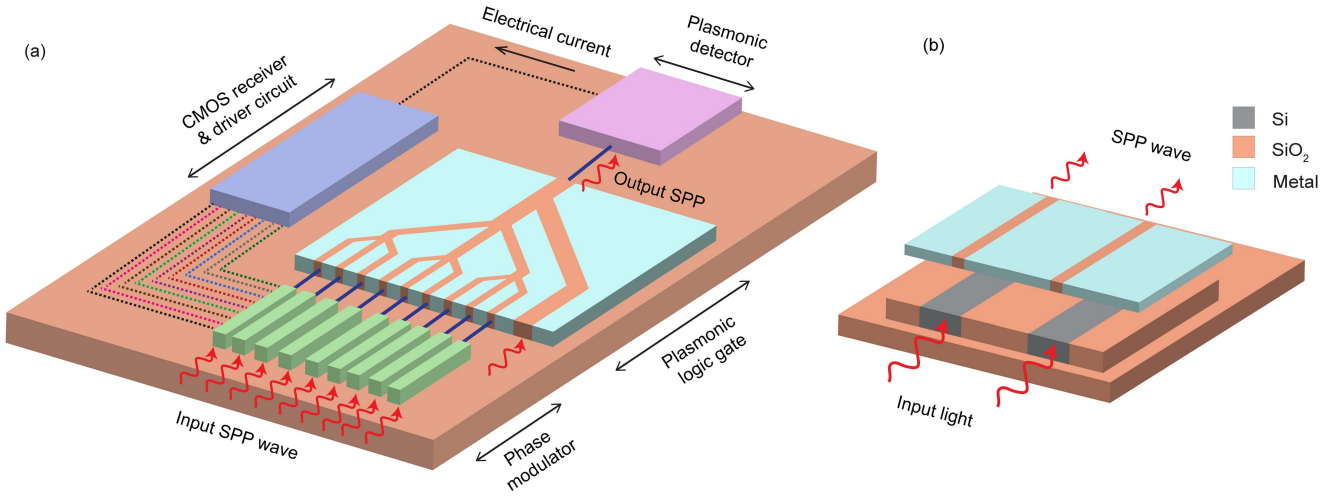

Fig. 1. (a) A plasmonic computing system consisting of phase modulators, a 9-input logic gate, a plasmon detector, CMOS receiver circuit, and driving circuit of the modulators. The phase modulator, plasmon detector, and CMOS circuits are represented as black boxes. The optical and electrical connections are shown as solid and dotted lines, respectively. (b) Si photonic to plasmonic mode coupling: only two photonic WGs are shown for simplicity. The system of (a) requires ten photonic WGs to excite plasmon for the ten input WGs of the logic gate.

should hence be included in the mode conversion design trade-off exploration.

In this work, considering all the aspects discussed above, we design and benchmark the potential performance of possible photonic to plasmonic mode converters for the application of plasmonic multiple-input devices such as interferometric logic gates. We consider single-mode Si photonic WGs and through rigorous numerical simulations, optimize their performance for mode coupling to plasmonic MIM WGs that act as the inputs of the logic gate.

II. Plasmonic Interferometric Multi-Functional Logic Gate

To design the mode converter for multiple-input plasmonic devices, we take a multi-functional plasmonic logic gate as an example. The nanoscale cascadable plasmonic logic gate was previously designed [9], and its application to implement arithmetic primitives like multipliers was demonstrated [23]. The logic gate can have 3, 9, or 27 inputs. The gate relies on the interference of the incoming SPP signals, resulting in multiple output levels that represent the strength of the majority of the input data. For example, the 9-input logic gate of Fig. 1(a) has ten possible output levels. Multiple output levels enable the gate to perform non-Boolean computing, such as majority voting in addition to Boolean logic like AND and OR operations.

The multi-functional logic gate is based on the plasmonic MIM WG that allows nm-scale mode confinement, resulting in an input pitch (center-to-center distance between adjacent WGs) of around a few hundred nanometers. For instance, the slot width of the input MIM WG of the logic gate of Fig. 1(a) is only 60 nm, and the input pitch is 310 nm. The pitch is determined considering the trade-off between crosstalk and footprint/ achievable device packing density [9]. The choice of material for the MIM WG also influences the pitch since mode confinement varies with different materials.

Dielectric/photonic logic gates have long lengths (several hundred microns to several millimeters) [24], [25] and large footprints, limiting their application in high-density integrated circuits. Photonic crystal-based logic gates offer smaller sizes, typically in the range of a few tens of microns [26], [27]. However, the design of photonic crystal-based structures relies on lattice orientation, limiting the adaptability of device structures for multiple functions. In contrast, plasmonic logic gates are compact (a 3-input logic gate is only 1.6 μm long, for example) and performs multiple functions.

III. Results and Discussion

This section discusses the coupling schemes of Si photonic waveguide (WG) and $Al - SiO_2 - Al$ plasmonic MIM WG. We consider CMOS compatible material Al for the MIM WG since the integration of plasmonics with Silicon photonics and electronics requires full technological compatibility with the mainstream CMOS front-end fabrication. The coupled structure is embedded in SiO_2. A cross-section of $60\ nm \times 100$ nm is considered for the MIM slot throughout the paper, which represents the cross-section of the input WG of the logic gate. The effective index of the single-mode MIM WG is $n_{eff,MIM} = 1.79 + 0.036i$. The calculated subwavelength mode volume of the WG is $0.0017\ \mu m^3$ or $0.02(\lambda_0/2n)^3$, where n is the index of the propagating medium, SiO_2 and free-space wavelength, $\lambda_0 = 1.31\ \mu m$. Five different mode coupling or conversion schemes are numerically investigated. Each scheme is optimized, and the transmission in the coupled MIM WG, which acts as the input of the plasmonic logic gate, is calculated.

A. Vertical Directional Coupling of Photonic and Plasmonic WGs

1) Mode Conversion Scheme 1: Plasmon mode can be excited in the MIM WG from a closely placed underlying Si WG, which forms a directional coupler. In scheme 1, out-of-plane

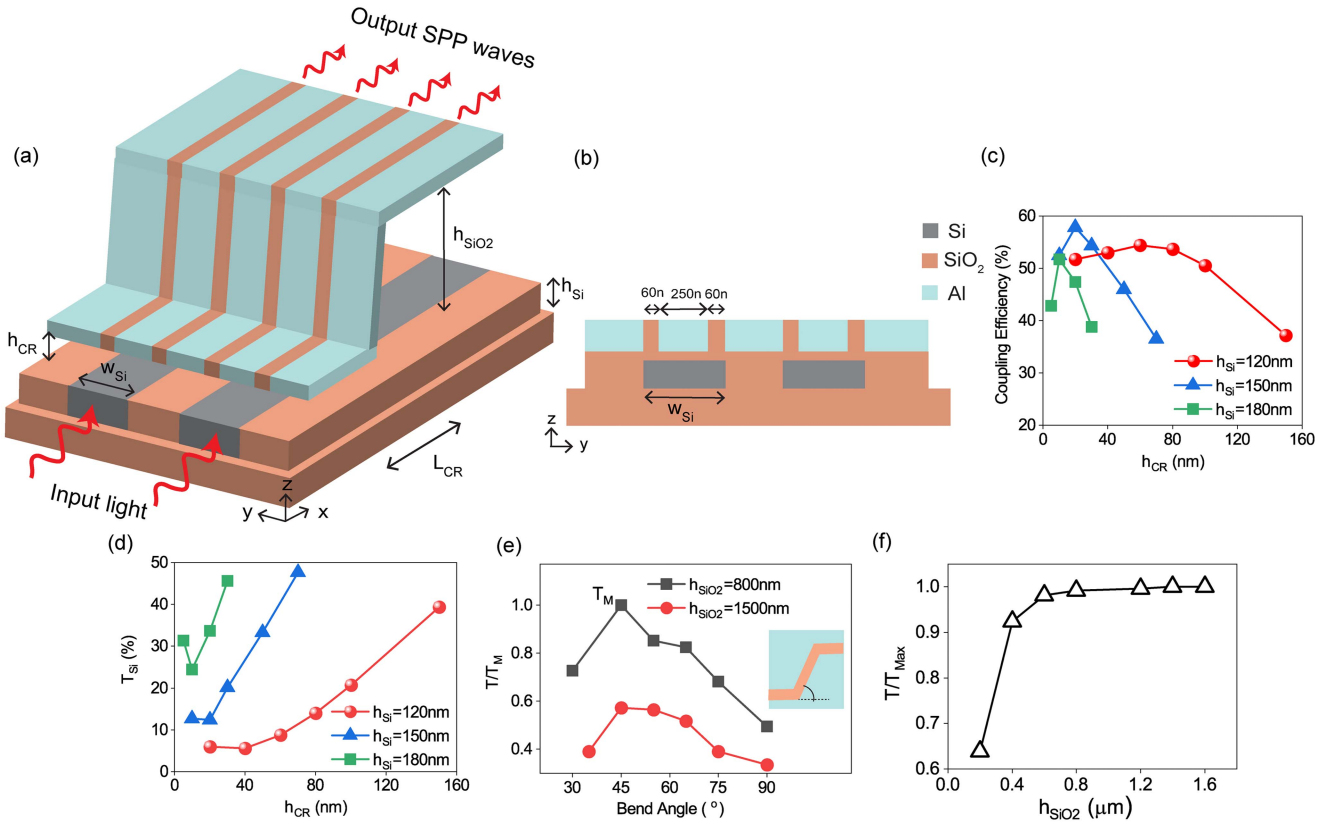

Fig. 2. (a) Representation of mode conversion scheme 1. For simplicity, the SiO_2 layer between the photonic and plasmonic WGs has not been shown. (b) Cross-section of the photonic and plasmonic WGs at the coupling region showing $w_{Si} = 370$nm. (c) Power coupling efficiency and (d) power transmission in Si wire WG for varying distance between Si and MIM WGs. (e) Optimization study of the MIM out-of-plane bend. Inset shows the out-of-plane bend angle. (f) Normalized power transmission at the output of a 3-input logic gate with varying h_{SiO2}.

bends are employed to vertically separate the photonic and plasmonic layers after plasmon excitation, which addresses the conflicting requirement outlined in the introduction. Fig. 2(a) represents scheme 1. In this scheme, plasmonic devices like the plasmonic logic gate can be implemented in the upper layer, while the photonic WG continues in the bottom layer.

For coupling, a single-mode Si wire WG is considered. As the conventional Si wire WG's core width ($\sim 400\ nm$) is nearly an order of magnitude larger than the MIM slot width ($60\ nm$), coupling a single MIM WG to a Si WG will require four (ten) Si WGs to excite plasmons for a 3-input (9-input) gate, substantially increasing the device footprint. To take advantage of the high integration density of plasmonic devices, two MIM WGs are coupled to a single Si WG. For example, Fig. 2(a) shows the coupling of four MIM WGs using two neighboring Si WGs, which can be utilized to excite plasmon in the four input WGs of a 3-input logic gate. Therefore, in this way, only two (five) Si WGs are needed to excite plasmon for a 3-input (9-input) logic gate. The MIM WG's width and pitch are the same as those of the input WG of the logic gate. Consequently, the Si wire WG's core width (w_{Si}) is ≥ 370 nm (Fig. 2(b)). Si WG supports multiple modes for $w_{Si} > 370$ nm at $\lambda_0 = 1.31\ \mu m$; hence, $w_{Si} = 370$ nm is considered in the design.

With $w_{Si} = 370$ nm, three different Si WG heights, $h_{Si} = 120$ nm, 150 nm, and 180 nm are considered. The corresponding Si WGs have an effective index, $n_{eff,Wire} = 1.96$, 2.17, and 2.33, respectively. The Si WG supports multiple TE modes for $h_{Si} > 180$ nm and is not considered. Power exchanges between the Si and MIM WGs in a beating pattern due to the interaction of even and odd supermodes of the coupled superstructure. The coupling region length (L_{CR}) represents the length over which maximum power ($T_{\text{Max},MIM}$) is transferred to the MIM WGs. The two MIM WGs carry equal power. Fig. 2(c) and 2(d) show the total power coupled to the two MIM WGs ($2\,T_{\text{Max},MIM}$ = coupling efficiency) and the power remaining in the Si WG (T_{Si}), respectively. The details of $T_{\text{Max},MIM}$ calculations are explained later in the method section.

Fig. 2(c) shows that when the separation (h_{CR}) between the WGS is small, the coupling efficiency is low due to the unequal excitation of the supermodes [16]. There is an optimal h_{CR} that results in the highest coupling efficiency. A larger h_{CR} degrades the coupling efficiency due to the weak coupling. Fig. 2(c) also shows that although $n_{eff,Wire}$ is closest to $n_{eff,MIM}$ for $h_{Si} = 120$ nm resulting in phase matching condition, its coupling efficiency is not maximum among the three values of the h_{Si}. For $h_{Si} = 120$ nm, the coupling efficiency is maximum at a larger h_{CR}, resulting in increased coupling length and higher propagation loss. Further reduction of h_{Si} reduces the coupling efficiency more and is, therefore, not taken into account.

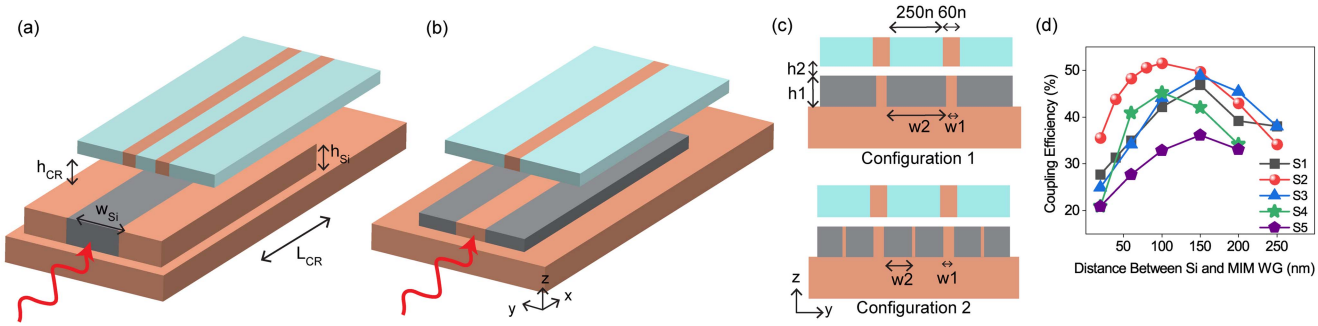

Fig. 3. (a) Representation of mode conversion scheme 2. (b) Vertical directional coupling of Si slot WG and MIM WG. (c) Cross-section view of the two different configurations of the Si slot WG used in our design. (d) Optimization of coupling efficiency for the five different samples of Si slot WG coupled to a MIM WG.

The coupling efficiency is maximum for $h_{Si} = 150$ nm and $h_{CR} = 20$ nm, where 58% of the input power is coupled to the two MIM WGs, and 12.5% remains in the Si WG for a coupling region length, $L_{CR} = 800$ nm. Maximum power coupling to the MIM WGs is expected for the operation of the plasmonic devices. However, if the Si WG is used for exciting SPP for the next computation stage, sufficient power should also flow through the Si WG. For this reason, although $h_{Si} = 150$ nm results in the maximum power coupling to the MIM WGs, considering the amount of power remaining in the Si WG, $w_{Si} = 370$ nm, $h_{Si} = 180$ nm, $h_{CR} = 20$ nm, and correspondingly $L_{CR} = 1\ \mu m$ are the optimized parameters. In this configuration, 47% of the input power is coupled to the two MIM WGs, and 34% remains in the Si WG. The same WG setting is also simulated without the plasmonic loss. In the lossless case, 60% of the input power is coupled to the MIM WGs, and 38% remains in the Si WG.

Scheme 1 uses an out-of-plane bend to separate the photonic and plasmonic layers. Next, we optimize the MIM out-of-plane bend configuration. We simulate an MIM out-of-plane bend with different bend angles and find the power transmission 200 nm after the bend edge. Fig. 2(e) shows the normalized T values for bent WGs when $h_{SiO_2} = 800$ nm and 1500 nm. For both cases, the bend angle of 45^o results in maximum power transmission. Moreover, with the increase of h_{SiO2}, T decreases due to the loss associated with increased plasmon path length. However, a large h_{SiO_2} helps to avoid power coupling back to the photonic mode. For example, we have simulated a 3-input plasmonic logic gate for varying h_{SiO2}, as shown in Fig. 2(f). Simulation results show that when $h_{SiO2} > 1500$ nm, there is a negligible change in the power transmission at the logic gate output. As h_{SiO2} decreases, power transmission decreases due to power coupling back to the bottom Si WG. Moreover, when $h_{SiO2} = 800$ nm, power transmission reduces by $\sim 1\%$ of the maximum transmission. Further reduction significantly increases the power coupling to the Si WG, reducing the power at the output of the logic gate. As a result, we have selected $h_{SiO2} = 800$ nm as the optimum value.

We simulate the complete mode conversion scheme 1 with the optimized values: $w_{Si} = 370$ nm, $h_{Si} = 180$ nm, $h_{CR} = 20$ nm, $L_{CR} = 1\ \mu m$, and $h_{SiO_2} = 800$ nm. The resulting total transmission in the two MIM WGs is 14% (7% in each MIM WG), and transmission in the Si WG is 40%. Here, total loss includes the loss associated with coupling and the propagation decay/plasmonic loss. If plasmonic losses were absent, total power transmission in the two MIM WGs would increase to 30%. Power transmission in the two MIM WGs drops from 47% (in the coupling region) to 14% (after the out-of-plane bend). Therefore, the out-of-plane MIM bend results in more than 5 dB loss. This significant loss strongly motivates us to study other schemes that do not have out-of-plane bends.

2) Mode Conversion Scheme 2: With the previous scheme, only 14% of the input optical power is transmitted to the two output MIM WGs. The remaining power is dissipated due to plasmonic and bending losses or is propagated in the underlying Si WG. To improve the transmitted plasmonic power, we look at the option where the Si WG is terminated after coupling to plasmonic mode, as shown in Fig. 3(a). Outside the directional coupler, the Si WG is absent under the MIM slot, and the mode is guided only by the MIM WG. We have considered this scheme as an application case when there is only one computation stage. The analysis is the same as in Fig. 2(c)–(d). The optimized parameters are $w_{Si} = 370$ nm, $h_{Si} = 150$ nm, $h_{CR} = 20$ nm, and $L_{CR} = 800$ nm, which result in 58% total transmission in the two MIM WGs. We also simulated the same WG setting without the plasmonic loss. In the lossless case, 73% of the input power is coupled to the MIM WGs, and 14% remains in the Si WG. Therefore, coupling efficiency drops from 73% to 58% due to the plasmonic loss, which is reasonable as the plasmonic realization significantly enhances the compactness of the overall design.

3) Mode Conversion Scheme 3: To match the effective index of Si WG with the MIM WG, Si slot WG is employed, as shown in Fig. 3(b). Unlike the Si wire WG, the Si slot WG can support and guide mode for a narrow slot width. Therefore, a single MIM WG can be coupled to a single Si slot WG without paying any penalty in terms of footprint. Two different Si slot WG configurations (Fig. 3(c)) are designed to match the input WG pitch $(310\ nm)$ of the plasmonic logic gate. For Config. 1, the Si region of the neighboring two WGs is shared, while for Config. 2, a SiO_2 spacer separates the two neighboring WGs. The SiO_2 spacer helps to change Si width $(w2)$, which in turn changes the effective index of the Si WG. Using the two WG configurations, the slot width $(w1)$, Si width $(w2)$, and WG

TABLE I
PARAMETERS OF THE SI SLOT WG SAMPLES WITH $n_{eff,Slot} \approx 1.79$

Sample	Slot width, w1 nm	Si width, w2 nm	WG height, h1 nm	Effective index, $n_{eff,Slot}$
S1	20	290	80	1.77
S2	20	140	200	1.78
S3	40	270	100	1.8
S4	40	130	300	1.77
S5	60	250	100	1.7

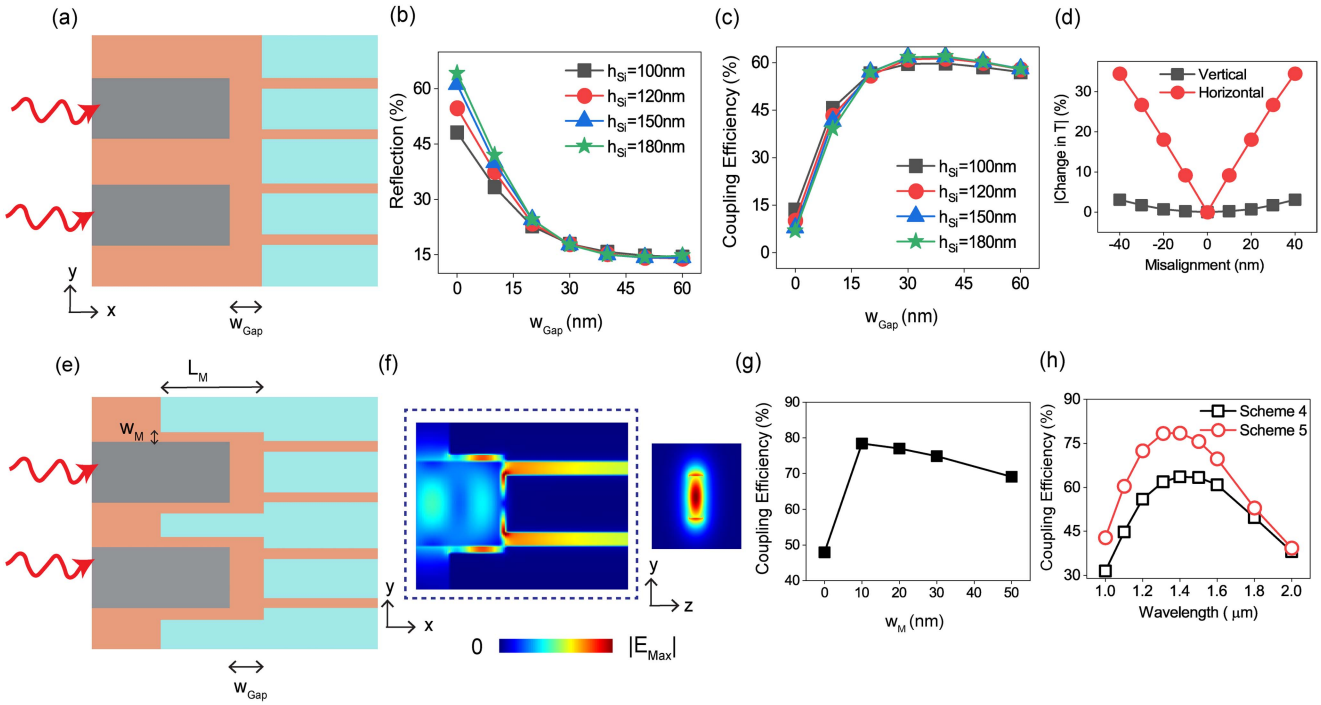

Fig. 4. (a) End coupling of Si wire and plasmonic MIM WG. Effect of w_{Gap} on (b) reflection and (c) coupling efficiency. (d) Fabrication tolerance study of scheme 4. (e) End coupling of Si wire and plasmonic MIM WG with overlapping metal near interface. (f) Electric field profile for scheme 5 and mode profile of Si wire WG showing sidelobes. (g) Optimization of coupling efficiency for scheme 5. (h) Wavelength dependence of coupling efficiencies of schemes 4 and 5.

height $(h1)$ are varied, and five different samples are designed that have an effective index, $n_{eff,Slot} \approx n_{eff,MIM} \approx 1.79$, fulfilling the phase matching condition of the directional coupler. The parameters of the five samples are listed in Table I.

Here, samples S1, S3, and S5 represent the WG Config. 1 as the Si region of the neighboring two WGs is shared. The rest of the samples represent WG Config. 2. For the five samples, the coupling efficiency in the coupled MIM WG is optimized by varying the distance $(h2)$ between the two WGs. Fig. 3(d) illustrates the optimization study, where coupling efficiency $= T_{\text{Max},MIM}$, the maximum power coupled to the MIM WG. From the graph, S2 is the optimized configuration with WG parameters of slot width, $w1 = 20$ nm, Si width, $w2 = 140$ nm, and WG height, $h1 = 200$ nm. The calculated mode volume of the Si slot WG is $0.0168\ \mu m^3$, which is $10X$ the mode volume of the MIM WG. When the WG is placed at a distance, $h2 = 100$ nm from the MIM WG, 52% of the input power is coupled to the MIM WG, and 8% power remains in the Si WG at a coupling region length of $1.8\ \mu m$. Although the Si slot WG fulfills the phase matching condition of directional coupling, the coupling efficiency is not better than the phase mismatched Si wire WG case of scheme 2. This can be attributed to the added propagation loss in the plasmonic WG associated with the increased coupling length of $1.8\ \mu m$ for the Si slot WG case. However, when the plasmonic loss is hypothetically not present, the coupling efficiency improves compared to scheme 2, and 83% of the input power is coupled to the MIM WG while 5% remains in the Si WG.

B. End Coupling of Photonic and Plasmonic WGs

1) Mode Conversion Scheme 4: The two WGs can also be end-coupled for mode conversion. Fig. 4(a) shows the end coupling scheme of Si wire WG and MIM WGs. As discussed in scheme 1, the chosen width of the Si WG is $w_{Si} = 370$ nm, and two MIM WGs are coupled to a single Si WG. When the Si and MIM WGs are coupled back-to-back, a large amount of power gets reflected, resulting in inefficient coupling of the WGs. Introducing a gap between the photonic and plasmonic WG reduces this reflection. Fig. 4(b) and 4(c) show that as the

gap width (w_{Gap}) is increased from 0 nm to 40 nm, reflection reduces by 76.6%, resulting in a $9X$ improvement of coupling efficiency in the MIM WGs when $h_{Si} = 180$ nm. A further increase of w_{Gap} reduces the efficiency due to power loss in the gap. Fig. 4(c) also shows that the coupling efficiency is not significantly affected as h_{Si} is varied. From the figure, the optimized parameters are $w_{Si} = 370$ nm, $h_{Si} = 180$ nm, $w_{Gap} = 40$ nm, and the resulting coupling efficiency (= total transmission in the two MIM WGs) is 62%. The coupling efficiency improves to 70% when the plasmonic loss is not present.

The fabrication tolerance of scheme 4 has been studied by evaluating the alignment tolerance of the Si and plasmonic WGs. Fig. 4(d) presents the effect of misalignment between Si and plasmonic waveguides on coupling efficiency. In this study, the center of the Si WG is intentionally misaligned in both lateral (y) and vertical (z) directions compared to the plasmonic WGs. The results indicate that the coupling scheme demonstrates significant tolerance to vertical misalignment, showing only a 3% change for a misalignment of 40 nm. In contrast, the scheme is highly intolerant of lateral misalignment, leading to a 34% change in coupling efficiency for a 40 nm lateral misalignment. However, the lateral misalignment (overlay accuracy) for the state-of-the-art 193 nm immersion lithography is 3 nm (mean + 3 sigma) [28]. Slightly older technologies can achieve $<$ 10 nm (mean + 3 sigma). Therefore, even with older technologies, we can expect a change in coupling efficiency of less than 10% due to lateral misalignment of the waveguides.

2) Mode Conversion Scheme 5: The mode coupling in the end-coupled MIM WGs can be further improved by introducing metal in Si WG's cladding close to the coupling interface. The coupling arrangement is shown in Fig. 4(e), with the electric field and cross-sectional mode profiles shown in Fig. 4(f). The mode profile shows that the eigenmode of the Si wire WG has two side lobes outside the Si core. The side lobes interact with the surrounding metal placed in the vicinity of the Si WG and coupled to the MIM WG mode.

The gap between the Si core and metal (w_M) is critical for improving the coupling efficiency, as shown in Fig. 4(g). With no gap, metal touches the Si core, making the Si WG lossy, which reduces the coupling efficiency to 48% from 62% in scheme 4. Introducing a gap between the Si and metal efficiently introduces the Si WG's side lobes into the MIM WGs and reduces the absorption loss in the mode conversion. With a 10 nm gap. the coupling efficiency is maximum, resulting in 78% power transmission in the two MIM WGs. If the gap is further increased, the coupling loss increases as the side lobes are scattered, reducing the coupling efficiency. Although the overlapping metal helps to improve mode coupling, it should not be too long. Our simulations show that if $L_M > 300$ nm, coupling efficiency starts to degrade due to an increased loss in the Si WG. The coupled WG configuration is simulated for zero plasmonic loss, and the resultant coupling efficiency is 93%.

We have performed a wavelength sweep for schemes 4 and 5, as shown in Fig. 4(h). For both schemes, the coupling efficiency changes less than 10% if the wavelength varies from 1.2 μm to 1.6 μm. Further change in wavelength significantly impacts the coupling efficiency.

Fig. 5(a) summarizes the performance of the five mode conversion schemes. The total footprint is calculated by considering an integrated system comprising photonic to plasmonic mode converters, plasmonic phase modulators [29], a 3-input plasmonic logic gate, and a plasmonic detector [5]. The length of the phase modulator and plasmonic detector are 10 μm and 1 μm, respectively, which are taken from the literature [5], [29]. We can see that the total footprint is not largely affected by the conversion schemes, whereas scheme 5 results in a maximum coupling efficiency of 78%. If plasmonic losses were hypothetically eliminated, the transmission would improve to 93%, which shows this coupling scheme is quite efficient.

Although scheme 5 outperforms all other schemes, its application might be limited in systems with many components and multiple stages as both the photonic and plasmonic WGs/devices are in the same layer, which can result in congestion and blockage issues. The coupling schemes discussed in this work have different usage situations, and a single scheme cannot be selected as the best choice for all applications. For instance, scheme 1 is applicable for a system with multiple computational stages and the continuing Si WG at the bottom can be used for exciting SPP for the next computation stages. On the other hand, scheme 5 is the best choice when the system has only one computation stage.

IV. Method

The WGs are simulated using the state-of-the-art 3D finite difference time domain (FDTD) method [30]. Perfectly matched layers are used at the computational domain boundaries. The FDTD domain is widened enough to ensure that the field is negligible at the boundaries. The FDTD grid size is $5nm \times 5nm \times 5$nm and time step is $0.011fs$. The source used in the simulation is monochromatic with wavelength $\lambda_0 = 1.31$ μm. The wavelength dependence of the optical properties of Al is included in the simulation from the experimental data of Mcpeak et al. [31]. The refractive indices of the materials used in simulations are $n_{Al} = 1.094 + 11.82i$, $n_{Si} = 3.5$, and $n_{SiO2} = 1.45$ at 1.31 μm wavelength. Mode volume representing the spatial confinement of mode is calculated using the following relation [32]:

$$V_m = \frac{\int_V \epsilon(\mathbf{r})|\mathbf{E}(\mathbf{r})|^2 \, d^3\mathbf{r}}{(\epsilon(\mathbf{r})|\mathbf{E}(\mathbf{r})|^2)_{\max}} \tag{1}$$

Here, $\epsilon(\mathbf{r})$ and $\mathbf{E}(\mathbf{r})$ are the 3D index and electric field data, respectively. The volume integration is performed over a 1 $\mu m \times$ 1 $\mu m \times$ 1 μm region of the MIM and Si slot WG. Moreover, transmission in the MIM WG is measured using an eigenmode expansion monitor, which calculates the fraction of power transmitted to the mode supported by the MIM WG. Additionally, reflection is measured by calculating transmission just after the source and subtracting the value from 100%.

For the directional coupler, coupling efficiency is measured by calculating the maximum power transmitted in the MIM WG $(T_{\text{Max},MIM})$. The superstructure consisting of overlapping plasmonic and photonic WGs supports two supermodes of even and odd symmetry. Along the direction of propagation, power

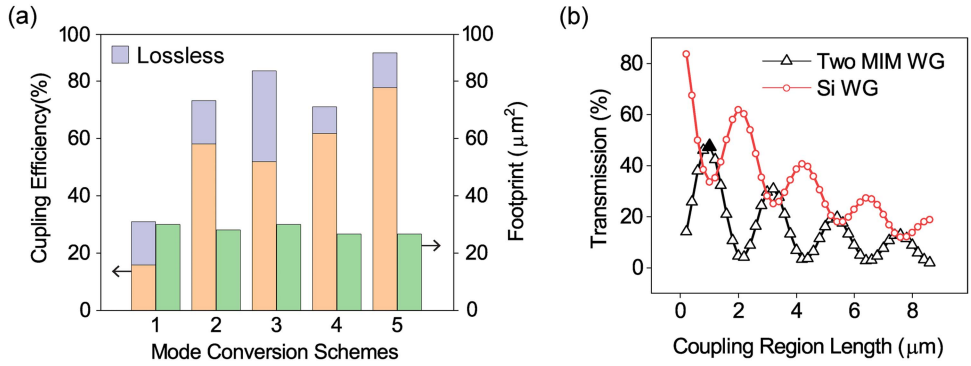

Fig. 5. (a) Comparison of the coupling efficiency and system footprint of the five mode conversion schemes. (b) Power transmission in a coupled Si wire WG and two MIM WGs showing the beating pattern. The solid symbol corresponds to the $2T_{\mathrm{Max},MIM}$ data point, which represents the coupling efficiency.

transfers from the Si WG to the plasmonic WG gradually due to the interference of these supermodes. The power exchange between the two WGs takes place every coupling length, L_{CR}. The output power of the MIM WG shows attenuated oscillations with an increasing interaction length. Fig. 5(b) shows the total power transmission in two MIM WGs coupled to a Si wire WG of $w_{Si} = 370$ nm, $h_{Si} = 180$ nm when the WG separation is 20 nm. From Fig. 5(b), calculated $2T_{\mathrm{Max},MIM}$ is 47%, and the coupling region length, L_{CR} is 1 μm. In the case of Si wire WG, coupling efficiency $= 2T_{\mathrm{Max},MIM}$ since two MIM WGs are coupled to a single Si WG, while coupling efficiency $= T_{\mathrm{Max},MIM}$ for Si slot WG.

Vertical directional coupling of Si WG and plasmonic WGs can be implemented/fabricated using the method described in [4]. Interested readers can refer to the reference. Implementation of plasmonic out-of-plane bend was also demonstrated earlier in literature [33] for long bends. For the relatively short out-of-plane bend MIM structure discussed in our work, wet etching can be employed to achieve the optimized 45^o bend angle.

V. Conclusion

In conclusion, we have performed a detailed numerical analysis of Si photonic to plasmonic MIM waveguide (WG) mode converters for multiple-input plasmonic devices, taking a plasmonic logic gate as an example. We have designed and compared five methods of mode conversion from Si wire and Si slot WGs, considering the input pitch of the plasmonic logic gate. For Si wire WGs, two MIM WGs are coupled to a single Si WG to address the size mismatch between photonic and MIM WGs. Both the directional and end coupling methods are included in our design. The coupling efficiency of each converter is optimized by varying the WG parameters, such as WG width and height, distance between the WGs, and length of the coupling region. Our analysis shows that directional coupling for both wire and Si slot WG results in $> 50\%$ coupling efficiency. However, continuing the photonic layer underneath the plasmonic layer results in the lowest power transmission in the MIM WG due to > 5 dB loss in the out-of-plane plasmonic bend used to separate the two layers. Additionally, we have found that for end coupling, introducing a metal overlap region close to the coupling interface significantly improves the mode converter's performance. The resulting coupling efficiency is 78%, which is the maximum among all of the mode conversion schemes.

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