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# Compressively strained epitaxial Ge layers for quantum computing applications

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ABSTRACT

The epitaxial growth of a strained Ge layer, which is a promising candidate for the channel material of a hole spin qubit, has been demonstrated on 300 mm Si wafers using commercially available $Si_{0.3}Ge_{0.7}$ strain relaxed buffer (SRB) layers. The assessment of the layer and the interface qualities for a buried strained Ge layer embedded in $Si_{0.3}Ge_{0.7}$ layers is reported. The XRD reciprocal space mapping confirmed that the reduction of the growth temperature enables the 2-dimensional growth of the Ge layer fully strained with respect to the $Si_{0.3}Ge_{0.7}$. Nevertheless, dislocations at the top and/or bottom interface of the Ge layer were observed by means of electron channeling contrast imaging, suggesting the importance of the careful dislocation assessment. The interface abruptness does not depend on the selection of the precursor gases, but it is strongly influenced by the growth temperature which affects the coverage of the surface H-passivation. The mobility of $2.7 \times 10^5$ $cm^2/Vs$ is promising, while the low percolation density of $3 \times 10^{10}$ $/cm^2$ measured with a Hall-bar device at 7 K illustrates the high quality of the heterostructure thanks to the high $Si_{0.3}Ge_{0.7}$ SRB quality.

## 1. Introduction

In the past decade, there has been a growing interest for Ge hole spin qubits in view of quantum information applications – interest that is driven by a combination of appealing material properties: high charge mobility, low hyperfine interaction, all-electrical spin control due to a large spin-orbit interaction, and its compatibility with existing CMOS technology [1–11]. Holes with p-like orbitals have indeed a strong spin-orbit coupling allowing spin control by an electric field, which is much easier in terms of device operation. Ge is a promising candidate as a channel material, because in Ge, holes have a stronger spin-orbit interaction and a smaller effective mass compared to Si. Since the latter implies larger quantum dots (easier confinement and observation of quantum confinement), this allows easier qubit control with a relaxed pitch. For quantum devices to be realized in Ge, and similar to the better studied case of Si, low defectivity, low disorder, low charge noise, and, in general, near-perfect isolation of the qubits from the solid-state environment are crucial [5,12].

The strained Ge layer is typically embedded in the relaxed $Si_{1-x}Ge_x$ layers to realize the valence band offset and the higher hole mobility due to compressive strain [13]. The fabrication of qubits with low charge noise characteristics sets a need for Ge channels with an extremely high material quality. Especially, the presence of threading dislocations is a concern [5,12]. The large lattice mismatch between the Si substrate and the $Si_{1-x}Ge_x$ strain relaxed buffer (SRB) layer with a Ge content around 70–80% of Ge is a driving force to introduce a high number of misfit and threading dislocations in the SRB. These defects can lead to strain non homogeneity in the overgrown strained Ge, even after prior chemical-mechanical polishing (CMP) of the $Si_{1-x}Ge_x$ thick buffer [14]. In addition, threading dislocations crossing the active layers of the quantum device, can glide and form misfit dislocation segments at the interface between the buried channel and the strained relaxed $Si_{1-x}Ge_x$ layers underneath and above [15,16]. Typical threading dislocation densities (TDDs) in reverse step-graded $Si_{1-x}Ge_x$ SRBs with 70–80% Ge grown on Si substrate are in the range of $10^6$–$10^7$ $/cm^2$ [3,7]. For recently, the second research group reported even lower TDDs, as low as

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$6 \times 10^5$ /cm$^2$, for reverse graded SRB with a top layer of $Si_{0.17}Ge_{0.83}$ and directly grown on a bulk Ge substrate [5]. The lower TDD is explained by the reduced lattice mismatch between the SRB and the Ge substrate. Because of the heavy mass, the maximum size of Ge substrates is however limited in production which limits the compatibility of Ge wafers with state-of-the-art CMOS processing which is today running on 300 mm wafers. Because of the higher compatibility with existing CMOS technology, the usage of a TDD optimized commercial SRB on a Si substrate is, therefore, today's best option to suppress the TDD in the active layer stack of the device. A TDD value as low as that for the case of using Ge wafers was reported for the forward graded buffer layer grown on the Si substrate [17,18]. In addition to the requirement on low TDD, the top interface of the Ge layer which is used as the channel is essential in terms of the carrier behavior [19].

In previous publications, we reported about Ge-rich epitaxial $Si_{1-x}Ge_x$ growth for Ge gate all around (GAA) field effect transistors [20,21]. The use of higher order precursor gases, disilane ($Si_2H_6$) and digermane ($Ge_2H_6$) for Si and Ge, respectively, allows to cover a wide range of Ge concentrations with a relatively high growth rate at a temperature which can be as low as 350 °C. The Ge growth at low temperatures also allows the deposition of strained Ge without the risk for 3-dimensional island growth (Stranski-Krastanov growth), which has been reported to be challenging when using conventional $GeH_4$ as Ge precursor [22]. However, spin qubit devices require the elimination of the nuclear spin. This sets a need to deposit $^{73}$Ge-depleted Ge and $Si_{1-x}Ge_x$ layers. In Chemical Vapor Deposition (CVD), this is currently only possible by using so-called $^{73}$Ge depleted $GeH_4$ as precursor gas. To our knowledge, none of the gas-suppliers is currently able to provide $^{73}$Ge depleted $Ge_2H_6$. In Ref. [23], the capability to deposit smooth 2-dimensional strained Ge on $Si_{0.25}Ge_{0.85}$ SRBs, without 3D islanding using $GeH_4$ has been demonstrated. However, at that moment in time, SRBs were less well developed. They contained a higher TDD and some within-wafer non-uniformity of the TDD and the distribution of the misfit dislocations. Also, the efficiency of pre-epi surface clean of Ge-rich $Si_{1-x}Ge_x$ layers was not at today's standard. Such a clean is required as the SRB receives a chemical mechanical polishing step to reduce the surface roughness before the stack with the strained Ge layer is grown. Those limitations resulted in uncontrolled interface contamination between the SRB and the 2nd epi layer and non-optimal interface characteristics between the strained Ge and the surrounding $Si_{0.15}Ge_{0.85}$. In case of a larger lattice mismatch (lower Ge content in the SRB), unwanted strain relaxation of the Ge-layer has been reported [23].

The assessment of the layer and interface qualities for a buried strained Ge layer embedded in $Si_{1-x}Ge_x$ layers, using conventional $GeH_4$, on 300 mm commercial SRBs is therefore still important. First studies can be done using natural $GeH_4$ followed by further demonstration using $^{73}$Ge free $GeH_4$. The change from natural to $^{73}$Ge free $GeH_4$ is expected not to affect the growth behavior as long as the dilution of the precursor gases is the same. The present paper reports on the development of strained Ge layers embedded in $Si_{0.3}Ge_{0.7}$ and epitaxially grown on top of commercially available $Si_{0.3}Ge_{0.7}$ SRBs using conventional precursor gases and an industry compatible CVD tool for 300 mm Si wafers.

## 2. Experimental

The compressively strained Ge layers embedded in $Si_{0.3}Ge_{0.7}$ layers were prepared in a 300 mm ASM Intrepid™ CVD reactor. The stacks were grown with natural-$SiH_4$ and natural-$GeH_4$ on commercially available SRB wafers [14,18], which contain $Si_{0.3}Ge_{0.7}$ in the top layer, and which are fabricated on conventional 300 mm Si wafers. The SRB wafers received a short dip in diluted HF combined with a $H_2$ bake at 800 °C at 20 Torr, which is sufficiently high to remove traces of oxide and low enough to minimize surface roughening [20]. The prepared stacks are summarized in Table I. The stack consists of top (24 nm) and bottom (100 nm) $Si_{0.3}Ge_{0.7}$ layers, and a strained Ge layer (14 nm) embedded in between these $Si_{0.3}Ge_{0.7}$ layers. A total of two samples were prepared by growing the same stack at different temperatures. The full stack of sample-H has been grown at a constant nominal growth temperature above 500 °C. For another sample, Sample-M, the Ge and the top $Si_{0.3}Ge_{0.7}$ layers were grown at a slightly lower nominal growth temperature which is a few 10 °C lower than 500 °C. The nominal growth temperature as chosen for the sample-M, is sufficiently low to maintain a strong H passivation during the growth. The presence/absence of H passivation is known to strongly affect surface diffusion during the growth [24]. 3D island growth for Ge grown on SRBs using a nominal growth temperature of 500 °C was reported in Ref. [25]. In addition, the H-passivation enables steeper interfaces as predicted in Ref. [26] and demonstrated in this manuscript. For the samples M and H, the same thicknesses of the individual layers were targeted (24 nm top $Si_{0.3}Ge_{0.7}$, 14 nm Ge, and 100 nm bottom $Si_{0.3}Ge_{0.7}$). Before growing these tri-layer stacks, single $Si_{1-x}Ge_x$ layers were grown on thick Ge buffer layers as virtual substrates, to confirm and adjust the growth rate and Ge concentration.

**Table 1**
The nominal structures of prepared samples.

| | Bottom $Si_{0.3}Ge_{0.7}$ layer | Strained Ge layer | Top $Si_{0.3}Ge_{0.7}$ layer |
|---|---|---|---|
| Sample-M | 100 nm (at >500 °C) | 14 nm (at <500 °C) | 24 nm (at <500 °C) |
| Sample-H | 100 nm (at >500 °C) | 14 nm (at >500 °C) | 24 nm (at >500 °C) |

The layers were characterized by X-ray reflectivity (XRR) for thickness extraction, X-ray diffraction reciprocal space mapping (XRD-RSM) for strain assessment, and High-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) combined with Energy dispersive X-ray spectroscopy (EDS) at 200 kV to study the interfacial abruptness. The material properties were compared to those of previous layers grown with higher order precursors [20]. The TDD was measured using electron channeling contrast imaging (ECCI) with the applied beam energy of 20 kV. Hall bar devices have been fabricated to measure key electrical properties at low temperatures. The electrical characterization was performed in a cryo-system with an electronic temperature of 7 K, a perpendicular magnetic field of 1 T, and a Source-Drain bias of 1 mV. A 2-dimensional hole gas (DHG) is formed in the Ge quantum well by applying a gate voltage going from 0 to −0.8 V. The Pd/Ti/$Al_2O_3$ stack was used as the gate stack [3]. Charge carrier density and mobility in this 2DHG are extracted from the longitudinal and transversal voltage measurements.

## 3. Results and discussions

$Si_{0.3}Ge_{0.7}$/Ge/$Si_{0.3}Ge_{0.7}$ stacks were grown on $Si_{0.3}Ge_{0.7}$ SRBs at different substrate temperatures. The distinct RSM peak corresponding to the strained Ge layer in addition to signals originating from both $Si_{0.3}Ge_{0.7}$ layers overlapping with that of the SRB was confirmed by XRD RSM taken around the $Si_{0.3}Ge_{0.7}$ 224 reciprocal lattice point. The strained Ge RSM peak vertically aligned with the $Si_{0.3}Ge_{0.7}$ RSM peak indicates that the 14 nm-thick Ge layer is fully strained with respect to the $Si_{0.3}Ge_{0.7}$ layers in the case of the sample-M (Fig. 1a). The thickness fringe was also visible between the peaks. The estimated compressive strain in the Ge layer is 1.41%. In the case of the sample-H for which both the nominally strained Ge and the $Si_{0.3}Ge_{0.7}$ top-layer were grown at a higher temperature, the Ge RSM peak was slightly tilted. The tilt and broadening of the RSM peaks as observed for the Ge layer grown at higher growth temperature indicate the presence of initial strain relaxation (Fig. 1b).

However, the ECCI inspection revealed that misfit dislocations were introduced during the growth of the sample-M where the RSM indicated that the layers were coherently grown on the SRB (Fig. 2). The line-shape contrast seen in Fig. 2 is the misfit dislocation that ended with the threading dislocation toward the sample surface. The inspection was performed with the applied beam energy of 20 kV, which enables the

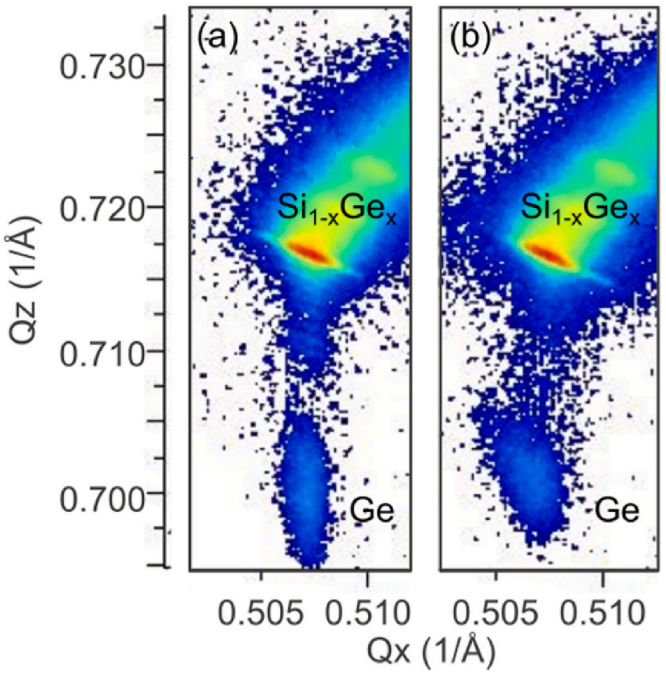


**Fig. 1.** RSM around 224 reciprocal lattice points of step-graded $Si_{0.3}Ge_{0.7}$ SRB, $Si_{0.3}Ge_{0.7}$ and strained Ge for (a) Sample-M and (b) Sample-H for which the Ge and the top $Si_{0.3}Ge_{0.7}$ layers were grown at a higher substrate temperature compared to (a).

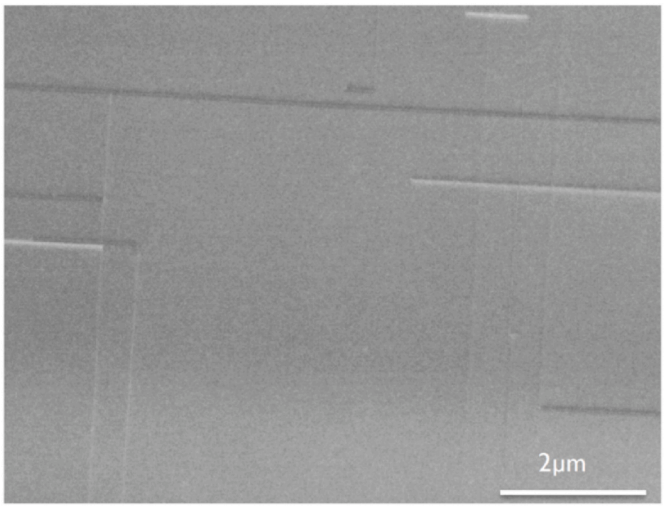


**Fig. 2.** Top-view ECCI image for the sample-M. The inspection was performed with the applied beam energy of 20 kV which goes as deep as around 90 nm from the surface. The selected diffraction vector $g = 220$.

detection of the threading dislocations and misfit dislocations up to a depth of around 90 nm [27]. The detected misfit dislocations are therefore located at the interface of the strained Ge layer, although it is hard to distinguish whether it is the top interface, the bottom interface of the layer, or at both interfaces. The estimated TDD from the ECCI inspection is $7 \times 10^6$ /cm$^2$, where 69 threading dislocations were observed in the investigated area of 982.42 μm$^2$. This TDD is higher than that in the SRB wafer ($<1 \times 10^6$ /cm$^2$ [18]). This also indicates that additional dislocations have been introduced during the growth. The theoretical critical thickness for layer relaxation calculated using the theory proposed by People and Bean [28] for strained Ge grown on strain relaxed $Si_{0.3}Ge_{0.7}$ lies below 10 nm. With a Ge thickness of 14 nm, there is a driving force for the introduction of new misfit dislocations. The 14 nm-thick strained Ge layer and the top $Si_{0.3}Ge_{0.7}$ layer were grown at lower than 500 °C for the sample-M, while the around 15 nm-thick Ge quantum wells for quantum applications grown at 500 °C have been reported [4,7]. This result suggests that the careful assessment of dislocations is essential, even though the average lattice constant indicates that the layer is fully strained according to the RSM result.

The HAADF-STEM inspection was carried out for the sample-H and the sample-M (Fig. 3). Because the HAADF-STEM contrast is approximately proportional to the square of the atomic number and to the thickness of the TEM lamella [29], the brighter contrast layers can be assigned to the Ge layer embedded in $Si_{0.3}Ge_{0.7}$ layers grown on the $Si_{0.3}Ge_{0.7}$ SRB. The same contrast for both top and bottom $Si_{0.3}Ge_{0.7}$ layers indicates that the top and bottom $Si_{0.3}Ge_{0.7}$ layers have nearly the same Ge contents. There is a contrast at the interface between the bottom $Si_{0.3}Ge_{0.7}$ and the $Si_{0.3}Ge_{0.7}$ SRB which is probably due to the CMP process and/or the strain non homogeneity in the SRB. A Ge enrichment (<10%) at the interface was observed by energy dispersive X-ray spectroscopy (not shown), however, it's confined near the interface. The inspection for sample-H revealed that 3-dimensional island growth of the Ge layer caused elastic relaxation observed with the tilt of the Ge peak seen in the RSM (Fig. 1b). The 3-dimensional island growth occurs when the growth temperature is too high, probably because during Ge growth, the surface is not H passivated [26]. This results in a more pronounced Ge surface diffusion during the Ge growth. The surface orientation of the 3-dimensional Ge island affected the top $Si_{0.3}Ge_{0.7}$ growth rate in addition to the surface diffusion during the $Si_{0.3}Ge_{0.7}$ growth. On the other hand, smooth and uniform $Si_{0.3}Ge_{0.7}$/Ge top and bottom interfaces and a smooth and uniform $Si_{0.3}Ge_{0.7}$ surface are seen for sample-M where the Ge layer and top $Si_{0.3}Ge_{0.7}$ layer were grown at a slightly lower substrate temperature (Fig. 3b). At lower growth temperatures, the H-passivated surface was maintained, and the surface diffusion was suppressed. In addition, no interface defects were observed at the upper and lower interfaces of the strained Ge layer in this inspection region.

For this sample, the interface quality was further confirmed by clear XRR fringes, observed from the center to the edge of the 300 mm wafer (Fig. 4a), which allows the extraction of the layer thicknesses of the $Si_{0.3}Ge_{0.7}$ top layer and the strained Ge layer (Fig. 4b). The bottom $Si_{0.3}Ge_{0.7}$ was excluded because it is identical to the $Si_{0.3}Ge_{0.7}$ SRB. The within wafer thickness variations of the strained Ge layer and the top $Si_{0.3}Ge_{0.7}$ layer were ±1.0 nm and ±2.0 nm, respectively. The corrected standard deviation of the total thickness of the top $Si_{0.3}Ge_{0.7}$ + strained Ge layers over the wafer as extracted from XRR spectra is 1.0 nm, which corresponds to a nonuniformity (relative standard deviation) of 2.7%. The difference in the average Ge contents at the center of the wafer and at a radius of ~100 mm from the wafer center is ~1% for both the bottom and the top $Si_{0.3}Ge_{0.7}$ layers and this for both sample-M and sample-H. These Ge concentrations were estimated by EDS performed with the cross-sectional TEM inspections.

The impact of the growth conditions on the interface abruptness was investigated using the horizontally integrated HAADF-STEM contrast. As mentioned above, the HAADF-STEM contrast is approximately proportional to the square of the atomic number. Namely, the contrast depth profile was used to extract the Ge depth profile. The upper interface of the strained Ge layer was slightly broader than its lower interface due to more pronounced Ge segregation from the strained Ge layer into the top $Si_{0.3}Ge_{0.7}$ (Fig. 5a). This difference can be explained by the strong Si–H bond on the bottom $Si_{0.3}Ge_{0.7}$ surface. The Si–H bond is stronger compared to the Ge–H bond and the presence of the hydrogen passivation suppresses the Ge segregation [26]. The integrated contrast was fitted with the Sigmoid function as shown in Fig. 5b. The Sigmoid function is expressed as follows,

$$f(x) = \frac{C}{1 + e^{\frac{\pm(x_0 - x)}{\tau}}} + b \cdots \quad (1)$$

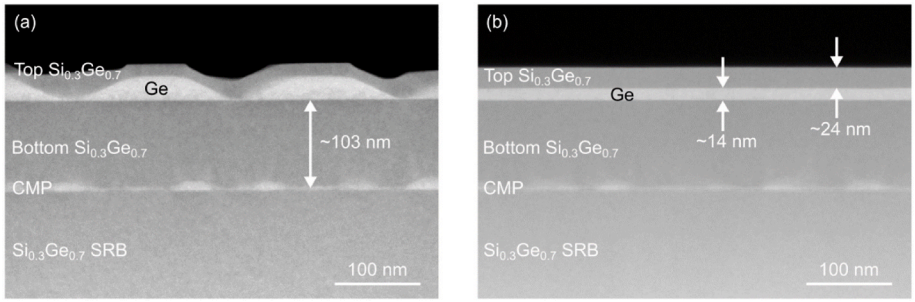


**Fig. 3.** Cross-sectional HAADF-STEM image of (a)Sample-H and (b)Sample-M.

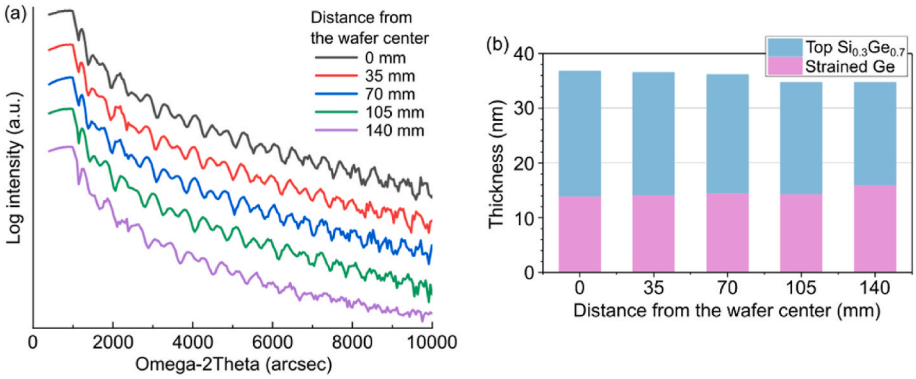


**Fig. 4.** (a) XRR spectra and (b) extracted thicknesses of the top $Si_{0.3}Ge_{0.7}$ and the strained Ge layers as a function of the distance from the wafer center for the sample-M.

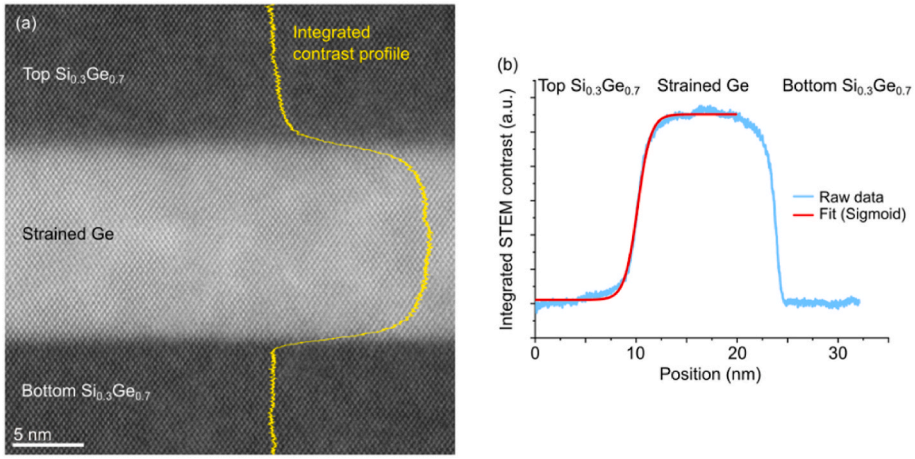


**Fig. 5.** (a) Cross-sectional HAADF-STEM image of the sample-M with the horizontally integrated contrast profile (yellow curve) and (b) the fitting result on the integrated contrast profile using the Sigmoid function.

where $C$ and $b$ are the constants and $Z_0$ denotes the position of the interface. The value of $4 \times \tau$ is used as the interface thickness [30,31]. From the Sigmoid function fitting, the interface thickness for the top interface of the strained Ge layer in sample-M was estimated to be 2.6 nm which is thicker than the interface thickness of 1.7 nm extracted for the bottom interface of the strained Ge layer. This thicker interface layer at the top interface is considered to be due to the higher amount of Ge in the underlying layer, namely the Ge segregation from pure-Ge in the case of the top interface. In addition, the estimated interface thickness is much higher than the values, e.g. ~0.8 nm as reported for the stack consisting of $Si/Si_{0.7}Ge_{0.3}$ [31]. This result indicates that further efforts are needed to suppress the Ge segregation in order to reduce the interface thickness if the strained Ge channel is considered as quantum qubit stack with the higher amount of Ge and the less pronounced surface H-passivation.

The top interface thicknesses were also estimated for other samples to compare the impact of the growth temperature and the choice of precursor gases on interface properties (Fig. 6a). One is the sample-H grown at a higher temperature, another one is a strained Ge gate-all-around stack [20] grown at 350 °C which is lower than the growth temperature used for sample-M but using $Si_2H_6$ and $Ge_2H_6$ as precursor gases. Note that the TEM specimens were prepared by focused ion beam (FIB) technique, always with the target lamella thickness of ~80 nm. The effect of the lamella thickness on the extracted interface thickness is supposed to be negligible. The growth rates of the top SiGe layers in

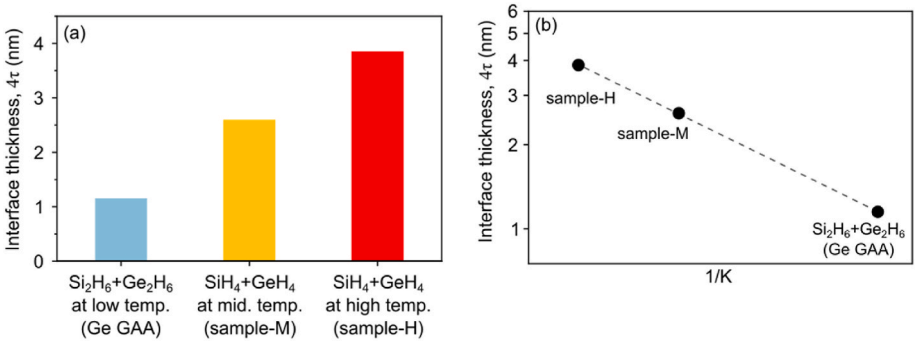


**Fig. 6.** (a) Interface thickness, 4τ, at the top $Si_{0.3}Ge_{0.7}$/Ge interface for the stacks grown with either $Si_2H_6$+$Ge_2H_6$ or $SiH_4$+$GeH_4$ and different substrate temperatures. The samples for yellow and red bars correspond to the sample-M and the sample-H, respectively. (b) Arrhenius plot of the extracted 4τ values for those samples.

three samples compared in this study increased with the increasing growth temperature. The Ge segregation is suppressed when the growth rate is high at the same growth temperature [32], the observed tendency, however, showed the suppression of the Ge segregation in the case of the growth at lower growth temperature. Therefore, the degraded interface abruptness by Ge segregation during the growth of the $Si_{0.3}Ge_{0.7}$ cap layer is strongly affected by the growth temperature which affects the coverage of the surface H-passivation. For the process conditions studied in this work, there is no indication that the choice of precursor gases affects the interface thickness, as shown by the straight line in the Arrhenius plot (Fig. 6b). The need for $^{73}$Ge-depleted gas leads to the conclusion of the analysis results: it is crucial to grow the stack at the lowest possible temperature within the range feasible when using $GeH_4$ as precursor gas.

The Hall mobility was measured for the sample-M at 7 K as shown in Fig. 7. The good repeatability of the measurement for 3 devices from the center of the same wafer exhibits the reliability of the measurements. The measurement displays a high peak mobility of $2.7 \times 10^5$ cm$^2$/Vs and a low percolation density of $3 \times 10^{10}$ /cm$^2$. The measured peak mobility is compared with the values reported in literature (Fig. 8). It should be noted that a higher mobility can be obtained by increasing the thickness of the top $Si_{1-x}Ge_x$ layer, because it reduces the impact of the scattering effect at the interface of the gate oxide and the top $Si_{1-x}Ge_x$ surface. On the other hand, thicker top $Si_{1-x}Ge_x$ layer may not be desirable on the control and upscaling prospective, because the thick top $Si_{1-x}Ge_x$ layer could increase the crosstalk effect [33]. The peak mobility as measured on the sample-M having thin top $Si_{0.3}Ge_{0.7}$ is promisingly high. This confirms the high quality of the heterostructure, in terms of material disorder and interface roughness thanks to the commercial SRB wafer. There is still room for improvement in the mobility as there are additionally introduced dislocations as measured by ECCI (although the RSM result indicated that the Ge layer is fully strained with respect to the $Si_{0.3}Ge_{0.7}$ bottom layer in terms of the average lattice constant of the strained Ge layer).

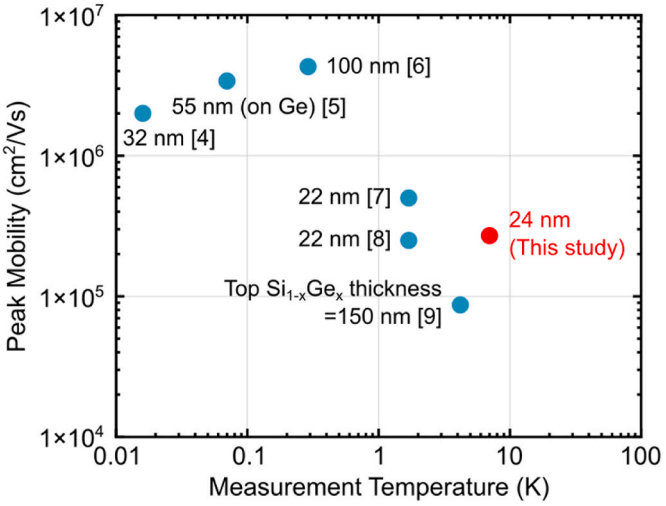


**Fig. 8.** The measured peak mobility plotted with reported values [4–9] as a function of the measurement temperature. The thickness of the top $Si_{1-x}Ge_x$ layer is mentioned for each plot.

## 4. Conclusions

Two-dimensional epitaxial growth of strained Ge layers embedded in $Si_{0.3}Ge_{0.7}$ layers grown on SRB layers fabricated on 300 mm Si wafers has been demonstrated. The stack was grown with a combination of $SiH_4$ and $GeH_4$ which is compatible with purified Si and depleted Ge precursor gases enabling elimination of nuclear spin dephasing. The reduction of the growth temperature allows the growth of fully strained Ge with respect to the SRB as confirmed by XRD-2DRSM measurements. However, the careful dislocation assessment by ECCI suggested the introduction of additional dislocations. The interface abruptness

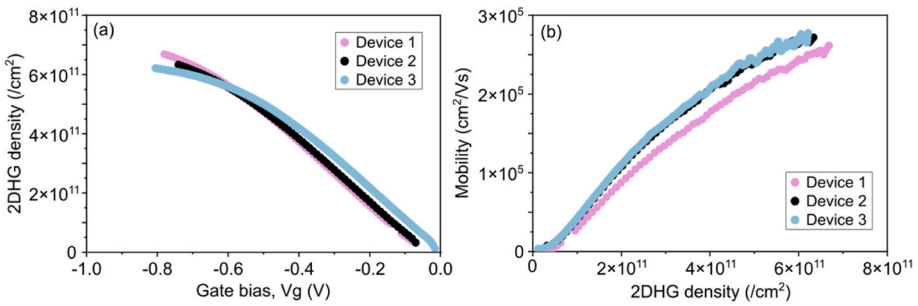


**Fig. 7.** (a) 2DHG density and (b) Hall mobility measured at 7 K on three different Hall-bar devices fabricated on the sample-M.

assessed by the HAADF-STEM contrast was found to be independent of the selection of the precursor gases, but it is strongly affected by the growth temperature which affects the coverage of the surface H-passivation. The mobility of $2.7 \times 10^5$ $cm^2/Vs$ and a low percolation density of $3 \times 10^{10}$ $/cm^2$ were measured using a Hall-bar device at 7 K. This promising peak mobility, despite (1) the use of the thin top $Si_{1-x}Ge_x$ layer and (2) the presence of dislocations measured by ECCI, indicates a high quality heterostructure thanks to the high $Si_{0.3}Ge_{0.7}$ SRB quality.

## CRediT authorship contribution statement

**Yosuke Shimura:** Writing – original draft, Investigation, Formal analysis, Data curation, Conceptualization. **Clement Godfrin:** Writing – review & editing, Investigation, Formal analysis, Data curation. **Andriy Hikavyy:** Writing – review & editing, Validation, Data curation. **Roy Li:** Writing – review & editing, Validation, Conceptualization. **Juan Aguilera:** Writing – review & editing, Investigation. **Georgios Katsaros:** Writing – review & editing, Investigation. **Paola Favia:** Writing – review & editing, Formal analysis. **Han Han:** Writing – review & editing, Formal analysis. **Danny Wan:** Writing – review & editing, Project administration, Funding acquisition, Conceptualization. **Kristiaan De Greve:** Writing – review & editing, Project administration, Funding acquisition, Conceptualization. **Roger Loo:** Writing – review & editing, Validation, Supervision, Project administration, Conceptualization.

## Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Data availability

No data was used for the research described in the article.

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