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Early defect detection for EUV self-aligned litho-etch litho-etch patterning with EPE

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ABSTRACT

We demonstrate the use of EPE (Edge Placement Error) as an early defect detection metric in an EUV self-aligned litho-etch-litho-etch (eSALELE) patterning process. Pitch 21nm test structures were investigated on an eSALELE flow consisting of 4 EUV exposures, 2 of which are lines-spaces while the other 2 exposures are for block patterns that defines the tip-to-tip. An HMI eP5 SEM with large field-of-view (8x8µm FOV) was used to measure critical dimension (CD) on wafer at each critical processing step while the overlay between multiple exposures were measured optically on uDBO marks using a YieldStar (YS). On top of CD metrology, patterning defects were measured at the final patterning transfer into dielectric material using an eP5 SEM and built-in defect inspection capability. Line-break defects are reported. Although each metric like CD, LWR or OVL is expected to contribute to the defect performance of the final pattern transfer, using only one information or another is not fully descriptive. Combining these information into an EPE metric on this complicated patterning process showed better correlation to the defect rates at dielectric transfer.

Keywords: eSALELE, EPE, defect, eP5

1. INTRODUCTION

Self-aligned patterning processes play an important role in enabling device scaling in advanced technology nodes. Even with the advent of extreme ultraviolet (EUV), multi-patterning is still needed to realize smaller dimensions and aggressive pitches. Densest metal layers for 5-nm node and beyond are patterned with multi-patterning schemes like self-aligned double/quadruple patterning (SA(D/Q)P) and self-aligned litho-etch-litho-etch (SALELE) [4][5]. SALELE has advantages over the traditional SA(D/Q)P due to the following: in SALELE, there are no metal widths or metal spacing limitations compared to SA(D/Q)P; LE1 metal lines are directly printed and LE2 metal lines are patterned directly and aligned to LE1 with the aid of spacers; SALELE also does not have design limitation in terms of internal routing tracks number whereas SAQP always enables designs with odd number; SAQP has a main challenge in terms of pitch walk which translates into critical dimension (CD) control problem; block mask schemes are also limited in SA(D/Q)P, while in SALELE block size is allowed to extend to the middle of the next metal track.

Advanced technology nodes with advanced devices and complicated patterning schemes come with tighter edge placement error (EPE) specifications [2]. Even with the aforementioned advantages of SALELE over SA(D/Q)P, final patterns require good process control to meet EPE requirements. The EPE budget contains contributions from systematic, global and local effects as expressed in Equation 1 [1]. Accurate estimation and measurement of EPE budgets are extremely important to enable holistic approach in EPE control from design phase, lithography, deposition and etch until final pattern transfer.

$$EPE_{max} = \frac{HR_{OPC}}{2} + \frac{3\sigma PBA}{2} + \frac{6\sigma LWR}{\sqrt{2}} + \sqrt{(\frac{3\sigma CDU}{2})^2 + (3\sigma OVL)^2} \quad (1)$$

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HR_{OPC}	=	Half-Range of the CD error due to optical proximity (OPC) residuals
PBA	=	Proximity Bias Average (field average CD by feature caused by scanner tool-tool variation)
OVL	=	Overlay error
CDU	=	CD Uniformity (reticle error, scanner error and error from etch and deposition processes)
LWR	=	Line Width Roughness originating from resist and photon stochastics + local mask errors

2. EXPERIMENTAL DESIGN AND METHODS

2.1 Description of the process flow

In this work, an EUV-based Self-Aligned Litho-Etch Litho-Etch (eSALELE) was chosen to achieve a 21nm line/space pitch grating [3]. The patterning flow is decomposed into 4 EUV exposures. There are 2 LE masks (LE1 and LE2), in which the second LE patterning is self-aligned to the first LE gratings using a conformal spacer deposition. The blocks are defined by 2 block masks (BL1 and BL2), which are self-aligned block schemes. The BL1mask defines blocks in the LE1 trenches selectively to the LE2 trenches, and vice versa for the BL2 mask.

2.1.1 LE1 process

The LE1 trenches are defined by transferring the printed patterns into an a-Si layer (see Figure 1). The pitch of these trenches is 42 nm, and the final target is to reach ~13nm a-Si lines. The litho lines are trimmed using a cyclic process of oxidation and oxide removal. Next, a conformal oxide spacer is deposited on the a-Si lines and subsequently etched, as shown in Figure 1c. At this stage, both populations of trenches are already defined: the a-Si lines are the mandrels and will form the LE2 trenches after a-Si removal later in the flow. The gaps in between the spacers are defining the LE1 trenches.

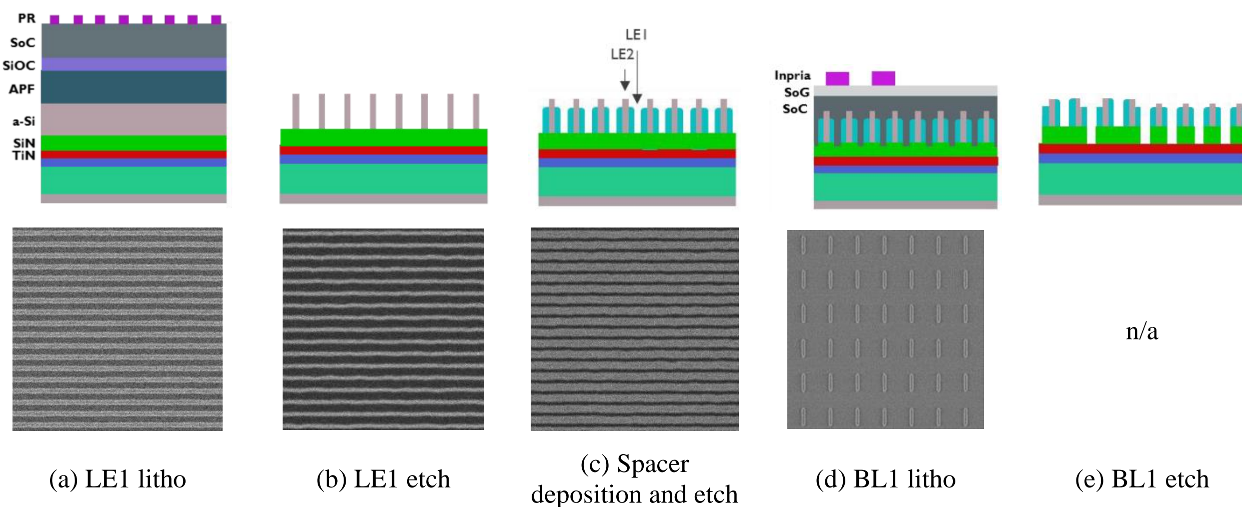

Figure 1: (top) A schematic representation of the LE1 and BL1 patterning steps of the eSALELE process flow. (bottom) Cropped top-down eP5 SEM images after (a) LE1 exposure, (b) the pattern transfer into a-Si, (c) spacer deposition and spacer etch, (d) BL1 exposure, and (e) BL1 pattern transfer into the SiN storage layer.

2.1.2 BL1 process

For the block BL1 patterning, a negative tone metal-containing resist is chosen to define the blocks for the LE1 trenches (Figure 1). The block patterns are consequently transferred into a spin-on carbon layer, after which both the blocks and the LE1 trenches are etched into the SiN storage layer. As the LE2 trenches are still protected with the a-Si mandrels, the BL1 layer is selectively blocking LE1 trenches without interfering with the LE2 trenches. From the top-down SEM images in Figure 2, the original block size can be observed due to the recess of the spacer material and the a-Si mandrels during the SiN etch.

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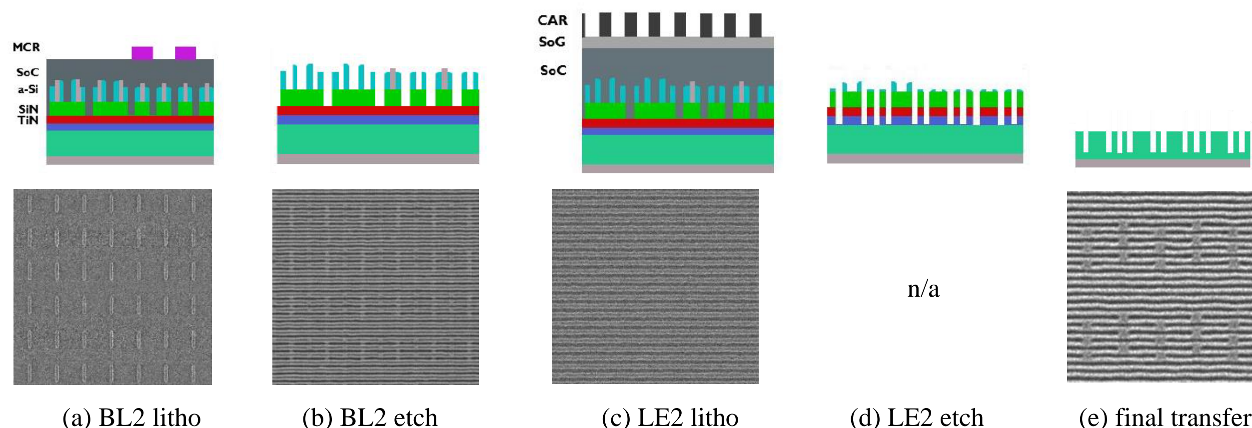

(a) BL2 litho (b) BL2 etch (c) LE2 litho (d) LE2 etch (e) final transfer

Figure 2: (top) A schematic representation of the BL2 and LE2 patterning steps of the eSALELE process flow. (bottom) Cropped top-down SEM images after (a) BL2 exposure, (b) the BL2 pattern transfer into a-Si, (c) LE2 exposure, (d) the pattern transfer into TiN and (e) the pattern transfer into the dielectric material.

2.1.3 BL2 process

The second block layer is defined using a negative tone metal-containing resist, as shown in Figure 2a. Next, the a-Si mandrels, which define the LE2 trenches, are removed everywhere except where the second blocks are defined (Figure 2b). As there is no a-Si in the LE1 trenches, this blocking scheme is selectively blocking LE2 trenches, without affecting LE1 trenches.

2.1.4 LE2 process

In the last patterning step, the LE2 trenches are defined. The relaxed LE2 lithography step targets 23 nm lines and trenches at 42 nm pitch, as shown in Figure 2c. These patterns are transferred in a regular tri-layer stack (spin-on-glass/ spin-on-carbon) and through self-alignment of the spacers, the LE2 trenches of ~12 nm are also transferred down into the SiN storage layer. After stripping the LE2 mask layers, all patterns can be transferred down in TiN (Figure 2d). For a better visualization with top down SEM, all the patterns are transferred into the underlying dielectric layer, followed by a wet removal of the TiN hard mask. As such, the SEM images in Figure 2e shows the final pattern transferred into dielectric using an eSALELE patterning scheme, with self-aligned blocks and self-aligned LE2.

2.2 eBeam Metrology

Along the patterning flow, an HMI's eP5 SEM with large field-of-view (8x8µm FOV) was used to collect images on wafer at each critical processing steps. The critical dimension (CD) of features (*e.g.* Space CD, Block width and height) and block placement were extracted from the images using built-in metrology software. With the large FOV, we characterize not only the average CD and its variation across wafer but also the line width/edge roughness (LWR/LER) for the lines-spaces patterns and the local CD uniformity (LCDU) for the blocks. Hence, CD, LWR/LER and LCDU transfers were investigated from after-litho through etch processes until the final pattern transfer. In this method, contours are extracted and used to calculate CD and roughness. As the SEM images are always affected by metrology noise, power spectral density analysis was used to remove this effect. In this paper we refer to them as unbiased line edge roughness (LER) and unbiased line width roughness (LWR). In addition to the CD metrology, patterning defects were measured at the final dielectric transfer also using an HMI defect inspection module. This defect inspection and classification module reports the number of defects and location within the large FOV image. Two defect types were extracted namely line-breaks and line-bridges, following an automatic defect classification. In this paper, we only focus on line-break defects as this is the major failure mechanism. A sample image with line break defect is shown in Figure 3.

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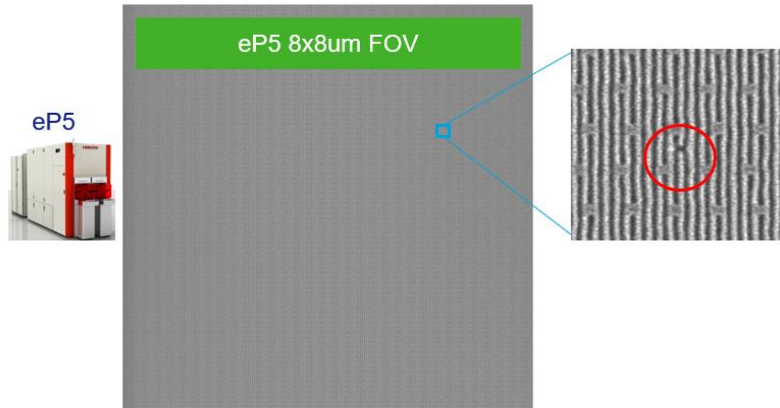


Figure 3: An HMI eP5 8x8µm FOV SEM image at final pattern transfer (zoomed in showing a line break defect)

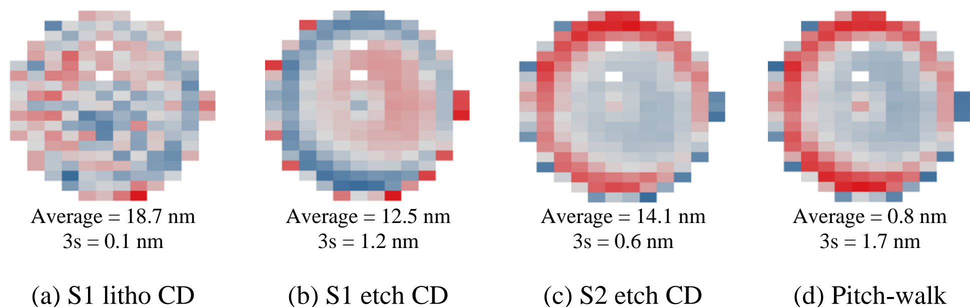
2.3 Overlay metrology

Overlay between multiple exposures were measured optically on uDBO marks using a YieldStar (YS).

3. ANALYSIS AND RESULTS

3.1 CD transfer through process

In the SALELE process, there are two populations of metal trenches as discussed in 2.1; one that is defined from the litho mandrel (LE2) and the other which is the space between the spacers (LE1). For convention throughout the rest of this section, LE2 will be labeled S1, while LE1 is S2. The process parameters that define S1 and S2 are different which means that the root cause of defects in S1 and S2 are also different. Figure 4 shows CD and LER after-litho and after etch. At after-litho, S1 LER (Figure 4e) is 1.9 nm and no visible fingerprint across the wafer is observed. CDU of 0.17nm (Figure 4a) is also small. The S1 CD is trimmed ~6nm from litho to etch (Figure 4b). In this etch trim process, CDU has increased due to etch non-uniformity. The LER after etch (Figure 4f) has also increased and varies across the wafer with clear radial signature. This signature is similar to the average CD fingerprint. The S2 CDU (Figure 4c) is similar to that of S1 since it shares the same etch trim process fingerprint, but opposite in sign. The S2 LER (Figure 4g) is lower compared to that of S1, this is because the S2 edges are defined by the spacer deposition process. Also noticeable that the LER fingerprint across the wafer is smaller, however the radial signature is still present. There is a pitch-walk (Figure 4d) of 0.8nm and varies across the wafer.



(a) S1 litho CD (b) S1 etch CD (c) S2 etch CD (d) Pitch-walk

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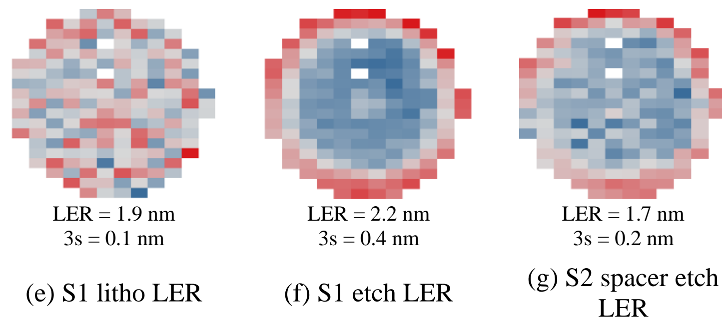

Figure 4: (a) S1 (mandrel) litho CD, (b) S1 (mandrel) after-etch CD, (c) S2 after spacer etch, (d) pith-walk, (e) S1litho LER, (f) S1 after-etch LER, (g) S2 after spacer etch LER

The wafer fingerprints after final pattern transfer into dielectric material for both S1 and S2 (shown in Figure 5a-b) look different compared to what is previously shown in Figure 4b-d. Noticeably, the S1 and S2 have different fingerprints, as well as two line populations, L1 and L2 (Figure 5c-d). The CD and LER (Figure 5d-e) do not share the same signatures. As discussed in 2.1, during the BL1 process S2 is etched into the SiN storage layer while S1 is protected. On the other hand, during the last process step (LE2 process), S1 is etched and transferred down into the SiN storage layer. After this, both S1 and S2 are transferred into the dielectric material. The differences in the processing of the two trench populations lead to the different signatures at the final pattern transfer.

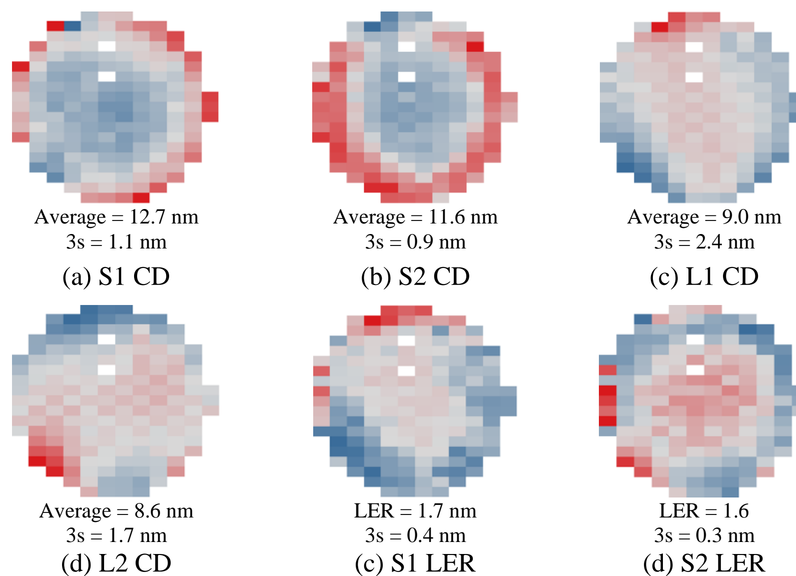

Figure 5: Final pattern transfer into the dielectric material: (a) S1 CD, (b) S2 CD, (c) L1 CD, (d) L2 CD, (e) S1 LER, (f) S2 LER

3.2 Overlay metrology

Overlay between multiple exposures were measured optically on uDBO marks using a YieldStar (YS). Most of mean+3σ values of overlay are less than 3nm, however for LE2 → LE1, larger variation is measured which is over 3nm. This large overlay contributes to the defects observed after the final transfer. LE2 → LE1 y-overlay is relevant overlay parameter for the line-break defects.

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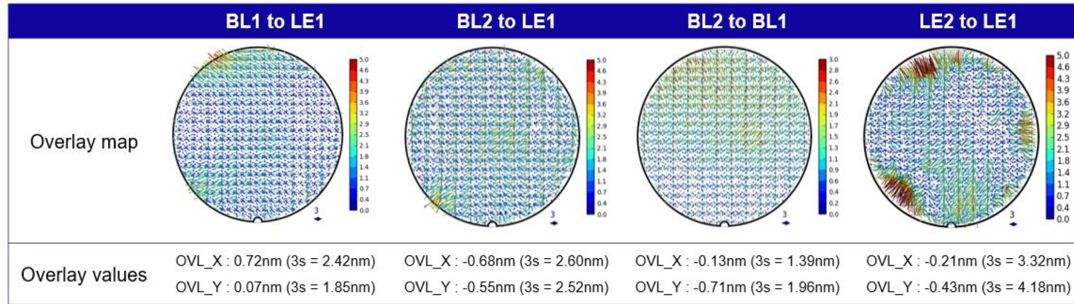
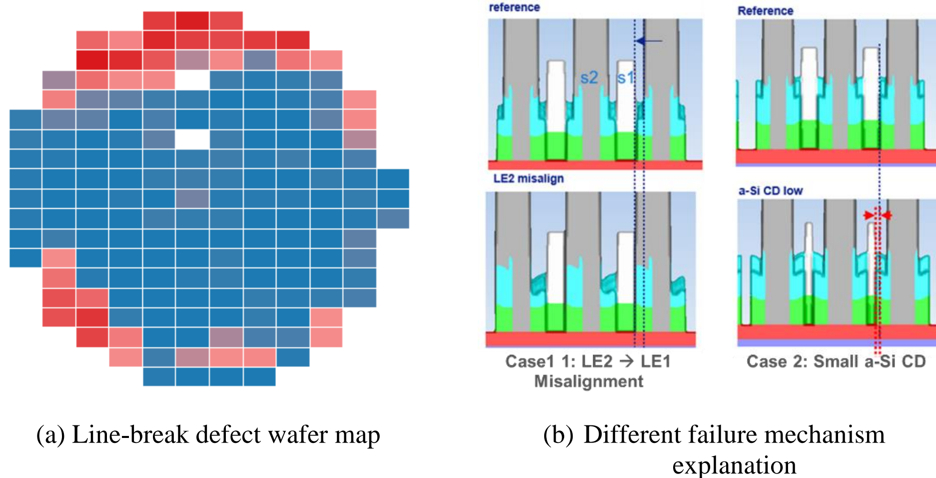


Figure 6: Measured overlay for different intra-layer exposures.

3.3 Defect characterization

As discussed in 2.2, patterning defects were measured. For this work, we only focus on line-break as this is the main defect mechanism observed on the wafer. Figure 7a shows the line-break defect wafer map. Most of the defects are located close to the wafer edge with concentration on either the wafer top or around the 7 o'clock. The defect wafer fingerprint have similar signatures to the following: LE2 → LE1 overlay (Figure 6), L1 and L2 CD after the final pattern transfer (Figure 5c-d), pitch-walk and the S1 and S2 CDs (Figure 4b-d). Whenever LE2 → LE1 y-overlay is large, or dielectric line CD is small, or the pitch-walk is high, or the LER is high, the number of defect increases.



(a) Line-break defect wafer map

(b) Different failure mechanism explanation

Figure 7: (a) Line-break defect wafer map at the final pattern transfer into the dielectric, (b) schematic of the line-break in the two main failure mechanisms

3.3.1 Failure mechanism

In Figure 7b, the two main failure mechanisms are shown schematically. One of the contributors of the line-break is the mis-alignment of LE2 → LE1 (Figure 7b Case1). During the LE2 etch, the oxide spacer should remain as much as possible because, it works as a hard mask for the final line patterning. But when LE2 pattern is misaligned in the y-direction against LE1 pattern, the oxide spacer is exposed more than normal. During the SiN etch, oxide spacer is consumed due to the low selectivity between SiN and oxide spacer. As a result, when there's a large LE2 → LE1 overlay, one of the line CDs becomes smaller, hence will result into a CD imbalance of the lines L1 and L2. As a consequence, the chance of a line-break failure is increased in the lines with smaller CD. This is indeed confirmed with the wafer data that on the locations with high LE2 → LE1 overlay, more line-break occurs and there is CD imbalance between L1 and L2. The second contributor to the line-break is the smaller a-Si CD which results in the pitch-walk and further result into the smaller line CD at the final pattern transfer (Figure 7b Case2). This effect is mainly driven by the a-Si etch process. If a-Si CD is small, more spacer is exposed during the LE2 etch and will cause spacer loss in the same manner as the previous case. Compared

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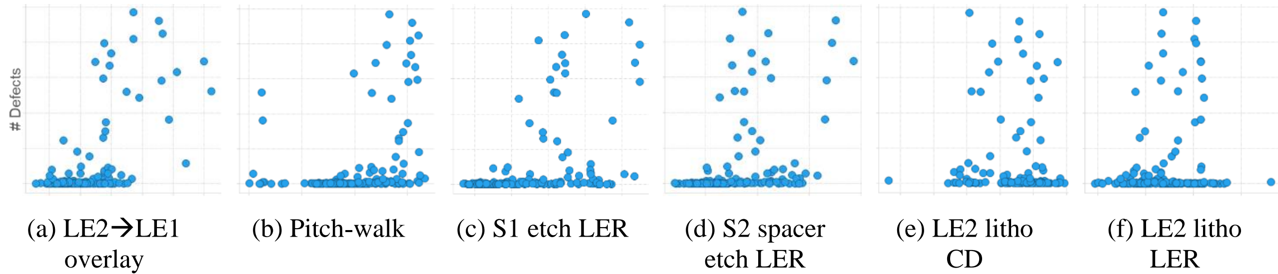
to case1 where there is CD imbalance, this mechanism leads to the smaller CDs of the lines L1 and L2. This effect is confirmed on the actual SEM images. The Figure 8a-f shows the correlation of defects to the individual metrics: LE2 → LE1 overlay, pitch-walk, CD and LER (in different process steps). We see that there is some correlation of the individual metrics to defects, however this correlation is a bit weak. Not one metric is enough to describe the defect trend.

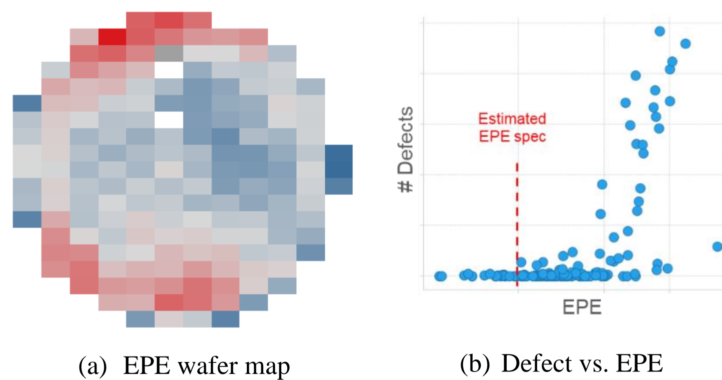


(a) LE2→LE1 overlay (b) Pitch-walk (c) S1 etch LER (d) S2 spacer etch LER (e) LE2 litho CD (f) LE2 litho LER

Figure 8: Correlation plots of individual wafer metrics to line-break defects at the final pattern transfer.

3.4 EPE characterization

The EPE metric combines systematic, global and local parameters into a single one as shown in Equation 1. Since using the individual metric is not enough to describe the defect trend, we use the EPE approach. We adapt the EPE equation to suit the SALELE use-case. Global and local parameters are used while the OPC and PBA are ignored. The Figure 9 shows the EPE wafer and the defect versus the EPE. The EPE wafer map qualitatively looks very similar to the defect wafer map shown in Figure 7a, and the level of correlation in Figure 9b has improved significantly compared to using only individual metric (as shown in Figure 8). This shows that in this complex SALELE process, EPE is a better metric compared to the overlay or CD alone to predict the performance of the final pattern transfer into the dielectric material. In this case, EPE was generated with the measured data after the LE2 litho exposure. At this step, EPE can be used to trigger early indication of patterning defects which could shorten the feedback loop, wafer rework and/or early wafer disposition.



(a) EPE wafer map (b) Defect vs. EPE

Figure 9: (a) EPE wafer map, (b) Correlation of defect and EPE.

In Figure 10a the EPE budget breakdown is reported. The local component dominates the budget at 54%, while the global part is 34% with overlay being the dominant contributor there. There is 11% systematic error due to targeting. The EPE_{max} is 13 nm which is much bigger than the estimated EPE specification from the device design. This also supports why we see patterning defects across the wafer. This process is in the early research and development phase hence significant process improvement is to be done. We reported in Figure 10b a simulated EPE budget breakdown if we correct for the systematic targeting error, better resist for LE2 exposure and correcting the global components via the Imaging Optimizer (IMO) dose and the Overlay Optimizer (OVO) scanner knobs. The EPE_{max} has reduced significantly to 6.9 nm, around the estimated EPE specification, then the local contribution becomes much more dominant at 74%; this means tighter requirement and optimization on the LER both at litho and etch transfers.

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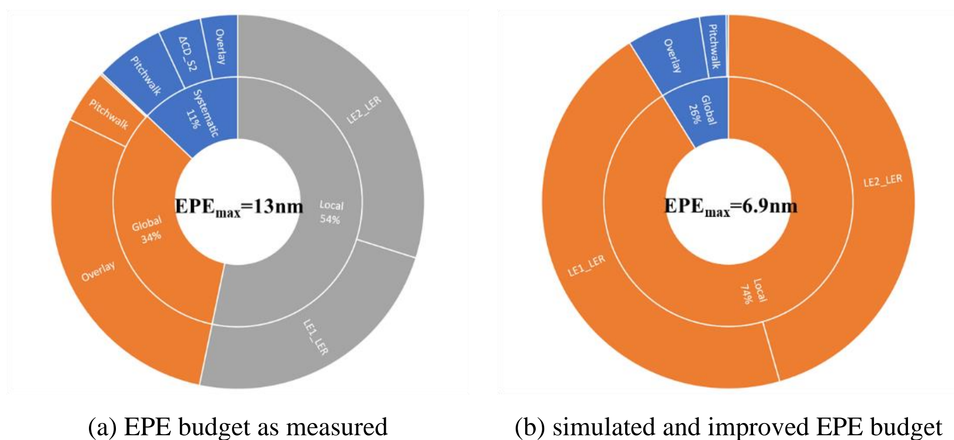

(a) EPE budget as measured (b) simulated and improved EPE budget

Figure 10: EPE budget breakdown (a) as measured, (b) simulated improvement.

4. CONCLUSION

We studied and characterized an eSALELE process on pitch 21nm test structures. The CD and LER were measured at each critical process step with HMI's eP5 large FOV SEM, and overlay with YS on uDBO marks. The line-break defects were also measured with HMI's eP5 after the final pattern transfer. The two cases of line-break failure mechanisms is described. They are mainly driven by mis-alignment and pitch-walk. We correlated individual metric (CD, LER, overlay) to the line-break defect performance, however, using only one or another shows a weak correlation. We have demonstrated that EPE is a better metric than just CD, LER or overlay independently. The EPE metric can be used to trigger early indication of patterning defects which potentially shortens the feedback loop, wafer rework and/or early wafer disposition. The EPE budget breakdown shows that the local effects dominating the EPE budget, followed by overlay. We also demonstrate that the EPE can be improved using the scanner dose and overlay knobs. Tight LER specification after-litho and after-etch is needed for this process to improve the defect performance.

5. ACKNOWLEDGEMENT

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