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ABSTRACT

Wafer bonding is a key technology for many advanced chip technologies. For 3D integration, advanced stacking schemes and high-density packaging put a stringent requirement on the bonding reliability. Bonding quality can be characterized by the absence of voids at the bonding interface, as the voids delimit the complexity of the subsequent processing and integration steps. Therefore, in-line and non-destructive inspection techniques for void detection are crucial for early-stage detection and full process integration. In this work, we perform a comprehensive study on bonding void detection for 3D integration. We fabricate bonded Si wafers with programmed bonding voids with size from 10 nm to 20 µm. We combine different inspection and review tools, including acoustic, optical, electron beam etc., for bonding void detection at different process steps of the fabrication with different top Si thicknesses.

Keywords: programmed bonding voids, scanning acoustic microscope, infrared microscope, high voltage scanning electron microscope, optical inspection, in-line inspection, non-destructive testing, 3D integration

1. INTRODUCTION

Three-dimensional (3D) integration stacks integrated circuits vertically to allow shorter interconnects with the advantages of higher bandwidth, lower power consumption, capability of heterogeneous integration, etc. 3D integration can occur at different levels of interconnect hierarchy, from package level to transistor level. Wafer bonding is a key process in several 3D integration schemes, such as die-to-wafer (D2W) stacking, wafer-to-wafer (W2W) stacking, backside power distribution network (BSPDN), and sequential CFET. In hybrid bonded die-to-wafer stacks, dies as thin as 50 µm can be temporarily bonded to a glass carrier to allow dicing or cleaning, and then permanently bonded to a Si wafer via hybrid metal/dielectric bonding.[1] In wafer-to-wafer stacking, two wafers with back-end-of-line (BEOL) layers are joined by hybrid bonding, followed by wafer thinning processes such as grinding, polishing and dry etching to target a final Si thickness of 5 µm.[2] In BSPDN and sequential CFET, the wafers are joined by dielectric-to-dielectric bonding followed by extreme wafer thinning, leaving only 500 nm or 10 nm - 50 nm of Si.[3,4] Bonding quality is important to these 3D integration schemes. Void free bonding is required to protect the stacks from stress during wafer thinning, and to ensure good electrical yield and multiple layers of stacking. However, these different 3D integration schemes use different materials at the bonding interfaces with different sizes and pitches of metal interconnections as well as target various final Si thicknesses. This requires us to combine multiple inspection techniques to detect bonding voids.

Bonding voids are one major source of bonding failure. They can be induced by trapped air, particles, uneven topography, high roughness, outgassing, etc.[5] The voids caused by trapped air and those surface discontinuity are directly formed after room temperature bonding, whereas the voids caused by outgassing are due to the thermal decomposition of organic contaminants during post-bond annealing.[6] The unbonded area becomes problematic for the processes after wafer bonding.[5] For example, delamination and wafer breakage can occur in the subsequent grinding process because of missing mechanical support and poor bonding strength. It can also cause non-uniform thinning that will later affect the TSV formation and multi-layer stacking.[7] The blisters formed above the bonding voids or the non-bonded dies can break or peel off, leaving contaminants in other tools.[8] Furthermore, the non-bonded metal interconnects will lead to electrical failures. Therefore, it is important to be able to detect bonding voids in an early-stage with in-line and non-destructive inspection techniques for the full process integration. With the increasingly higher interconnection densities and the development towards transistor level 3D integration, the critical bonding void size is becoming smaller, from micrometer

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down to nanometer range. Hence, it is also of significance to know the minimum void size that can be detected by different inspection techniques.

In this work, we perform a comprehensive study on bonding void detection for 3D integration. The objective is to find out the smallest detectable bonding void size after each critical process step of 3D integration. We fabricate bonded Si wafers with programmed bonding voids with size from 10 nm to 20 µm, with different top Si thicknesses from 775 µm to 50 nm corresponding to the different 3D integration schemes and process steps. We use and combine different inspection and review tools, including acoustic, optical, high-voltage electron beam etc., for bonding void detection at different top Si thicknesses. This study provides a guideline to the optimal detection method for different 3D integration schemes.

2. EXPERIMENT

2.1 Process flow and wafer description

To systematically replicate the bonding voids at bonding interface, we use the process flow of sequential CFET to fabricate the stacks as shown in Figure 1.[4] There are two sets of wafers involved in the bonding process, i.e., carrier wafers and donor wafers.

First, the carrier wafers were 300 mm p-type Si wafers with a thickness of 775 µm. 50 nm of SiO_2 was deposited on the Si substrate by plasma enhanced chemical vapor deposition (PECVD). Then 30 nm of SiCN was deposited as an etch stop layer by PECVD, followed by another 50 nm of SiO_2 by PECVD where the bonding voids would be formed. The wafers were then annealed. Electron-beam lithography (EBL) and dry etching were used to make the programmed voids with various lateral sizes. A control step was performed to characterize the programmed voids in the carrier wafers.

Second, the donor wafers were 300 mm silicon on insulator (SOI) wafers starting from 88 nm of Si channel and 145 nm of buried SiO_2. The wafers were annealed to oxidize the top Si channel and etched with HF to reach a final Si channel thickness of 54 nm. Then the wafers were annealed again to grow a thermal oxide of 10 nm for bonding and leave only 50 nm of Si channel. Edge trim was performed followed by cleaning. Next, the donor wafers were bonded to the carrier wafers by dielectric-to-dielectric bonding with a post-bond annealing. The programmed holes become programmed bonding voids at the bonding interface.

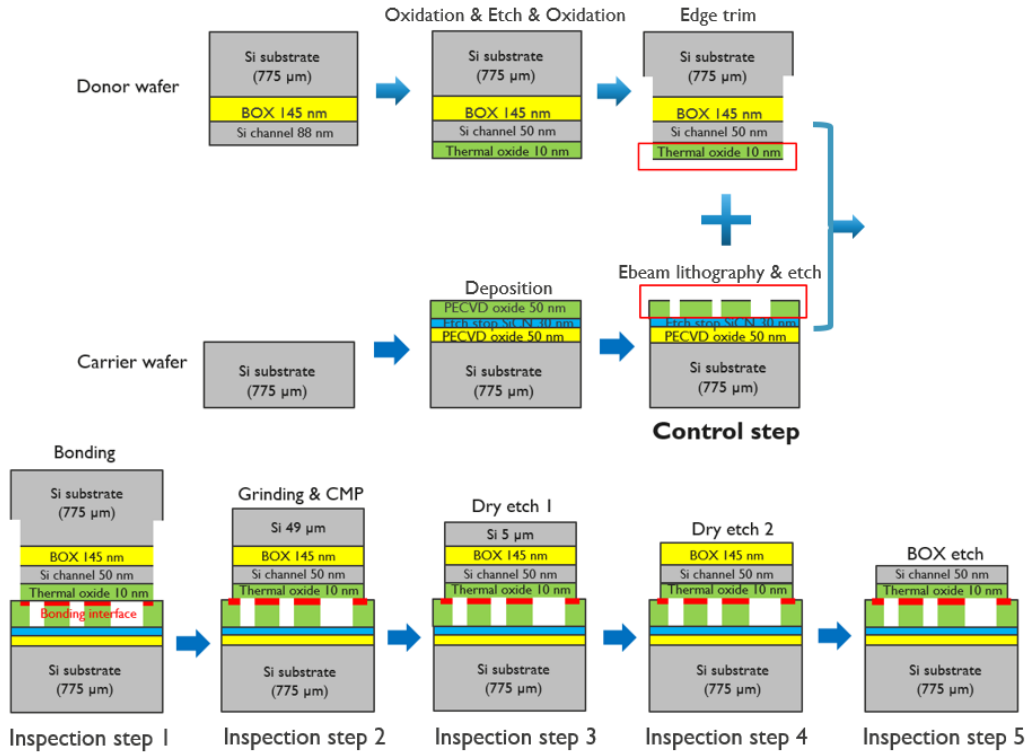


Figure 1 Schematic process flow of programming bonding voids in the test wafers.

Following that, we use different inspection and review techniques to detect the programmed bonding voids after each critical process. The void detection techniques performed on the stacks after post-bond annealing were named inspection step 1, after thinning to a top Si of 49 µm by grinding and chemical mechanical polishing (CMP) named inspection step 2, after dry etching to 5 µm of top Si named inspection step 3, after removing all Si substrate from the donor wafers by dry etching named inspection step 4, and after removing buried SiO_2 named inspection step 5. The above inspection steps are inserted after each critical process, which has different donor wafer thicknesses. An inspection for bonding voids is necessary for all 3D integration schemes at inspection step 1. Inspection step 2 is required for void detection for D2W targeting a die thickness of 50 µm, while inspection step 3 corresponds to void detection in W2W targeting a final top Si thickness of 5 µm. Inspection steps 4 and 5 are important for the void detection in sequential CFET.

In addition to different donor wafer thicknesses, we also introduce a wide range of void sizes from 10 nm to 20 µm as shown in Figure 2. The nanometer range voids are critical to transistor level 3D integration such as sequential CFET, while the micrometer range voids are critical to intermediate level 3D integration such as D2W and W2W. For each void size, there is a matrix of 10 × 10 voids with a constant pitch of 40 µm in both x and y directions. There is also an isolated void of the same size below the void matrix. A 100 µm long and 20 µm wide plus sign is added below each void matrix to help to locate the void matrix. A number indicating the void size in µm can be found below the plus signs.

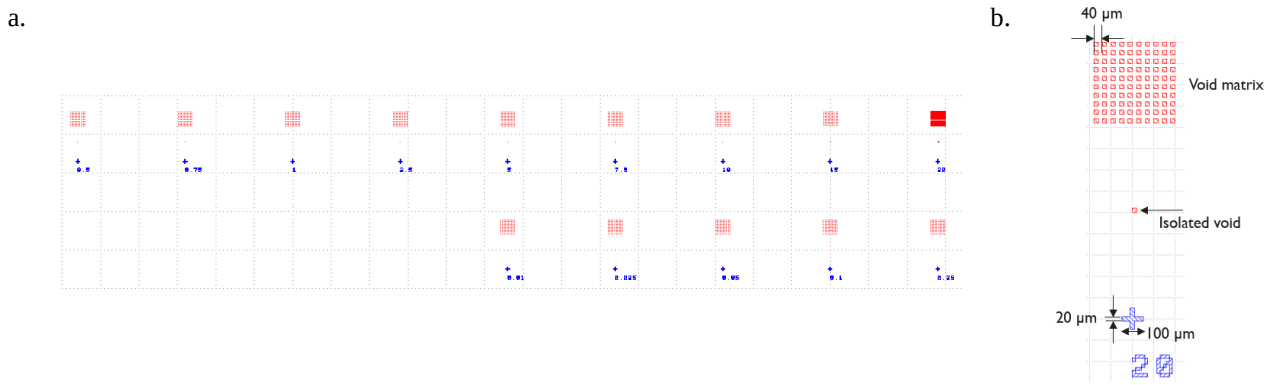


Figure 2 Design of the programmed voids. (a) Overview of the programmed voids. For each void size, there is a matrix of 10 × 10 voids with a constant pitch of 40 µm in both x and y direction. Below the void matrix, there is also an isolated void of the same size, a plus sign, and a number showing the void size in µm. (b) Magnification of the void matrix consisting of 20 µm voids.

2.2 In-line inspection and review techniques

At the control step, optical microscope in visible light wavelength, scanning electron microscope, and atomic force microscope were applied to check the size and depth of the programmed voids before bonding.

Various inline inspection and review techniques were employed to detect programmed bonding voids from inspection steps 1 to 5, including scanning acoustic microscope (SAM), infrared microscope, high voltage scanning electron microscope (HV-SEM), optical microscope in visible light wavelength, and optical interferometry. SAM and infrared microscope were used to detect bonding voids from inspection steps 1 to 3. HV-SEM, optical microscope, and optical interferometry were used to detect bonding voids at inspection steps 4 to 5.

3. RESULTS AND DISCUSSION

3.1 Control step

The programmed voids were etched into SiO_2 in the carrier wafer. The full wafer optical images were taken to identify the exposed dies and later can be used for comparison with the inspection steps after bonding. Figure 3 shows the cropped optical microscope image over the void patterns. Voids smaller than 2.5 µm cannot be observed with this optical image. To identify the smallest voids, scanning electron microscope was performed. Figure 4 shows the SEM images of the voids from 10 nm to 250 nm, confirming the patterning of the smallest void sizes in the design. All voids are designed to be squares, whereas after etching the voids smaller than 100 nm are rounded due to beam blur.[9] The voids in the range of 50 nm to 20 µm have a uniform depth of roughly 75 nm according to AFM (Figure 5). The voids of 10 nm and 25 nm are too small for the AFM cantilever to measure.

Figure 3 Cropped optical microscope image over the void patterns in one die.

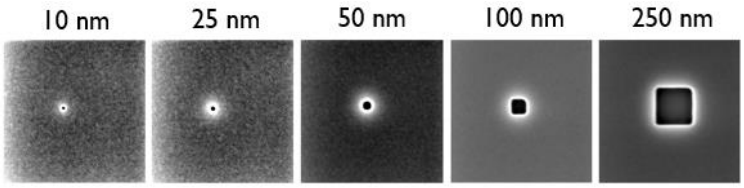


Figure 4 SEM images of the voids of 10 nm, 25 nm, 50 nm, 100 nm, and 250 nm. The field of view of the images is 1 µm.

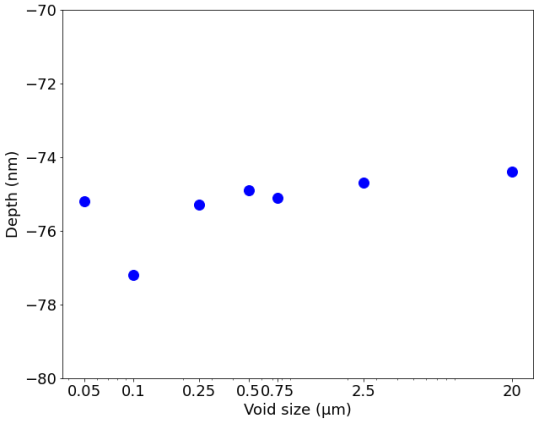


Figure 5 Void depth versus void size. The void depth was determined by AFM at the control step, i.e., prior to bonding.

3.2 Scanning acoustic microscope

The transducers in SAM have a nominal frequency of 175 MHz and a focal length of 8 mm in water. In order to achieve a good image quality, we place the transducers above the 775 µm Si side in all SAM measurements. Therefore, at inspection step 1 we scan the wafer from the donor wafer side, whereas at inspection steps 2 and 3 we flip the wafers for SAM measurement and inspect from the carrier wafer side. The full wafer SAM images in Figure 6a, c, and e were scanned at a resolution of 40 µm/px. The wafers are mostly well bonded except the wafer edge and the region where there are programmed bonding voids. The smallest detectable individual void sizes are 10 µm, 10 µm, and 15 µm, from inspection steps 1 to 3, respectively. The region of interest with programmed bonding voids were also scanned at 5 µm/px as shown in Figure 6b, d, and f. The grey values of the lines across individual voids and void matrices are plotted to reveal the void detection limit. The smallest detectable void sizes from inspection steps 1 to 3 are 7.5 µm, 7.5 µm, and 10 µm, respectively. The void detection becomes worse at inspection step 3. It is due to the fact that the at inspection step 3, the transducer collects both echoes from the bonding interface and the bottom of the stack, i.e., 5 µm Si/water interface. Therefore the echo from the well bonded region is also very strong and similar to that from the bonding void, making them difficult to be separated.

The voids in the void matrices with a pitch of 40 µm cannot be resolved individually by SAM at either 40 µm/px or 5 µm/px. Hence each void matrix becomes one large defect in the SAM image. It is easier to detect void matrix than individual voids in this case.

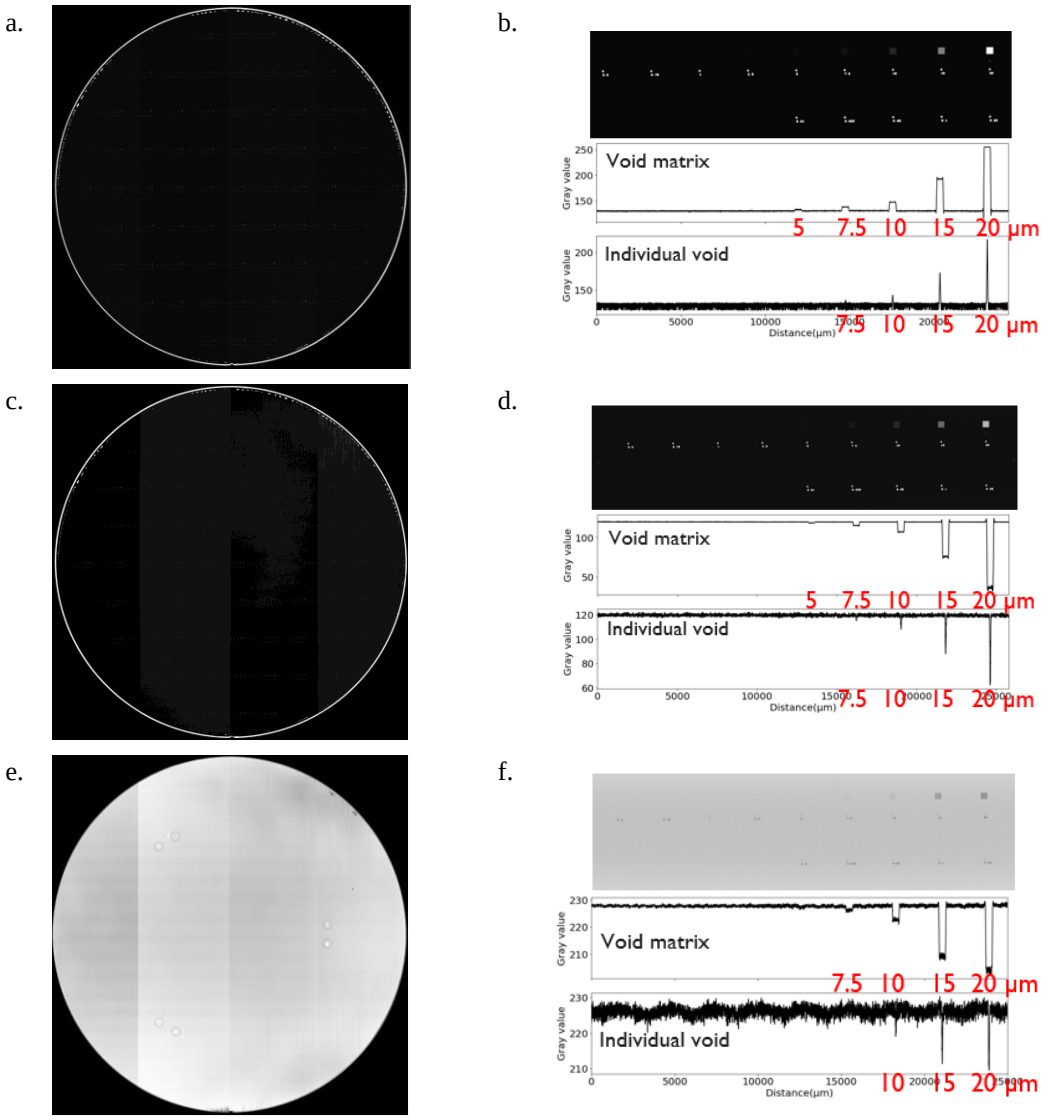


Figure 6 Full wafer SAM images at 40 µm/px, (a) inspection step 1, (c) inspection step 2, and (e) inspection step 3. Region of interest SAM images at 5 µm/px and the grey value across the void matrix and isolated voids, (b) inspection step 1, (d) inspection step 2, and (f) inspection step 3.

In summary, SAM (between 100-200 MHz range) can detect individual voids down to 7.5 µm and void matrix consisting of 5 µm below 775 µm of top Si. However, when the voids are too close to the top surface (<5 µm), the void detection capability is reduced.

3.3 Infrared microscope

Infrared microscopy can detect and resolve individual bonding voids down to 2.5 µm from inspection steps 1 to 3 as shown in Figure 7. Si has a bandgap of 1.12 eV at 300 K, and hence it is transparent to light with wavelength larger than 1100 nm, i.e., infrared light. SiO_2 and air have different refraction indices, and therefore we detect contrast between the well bonded area and bonding voids in the infrared microscope images. All measurements were performed in the transmission mode, with an infrared lamp illuminating from the carrier wafer side. The grey values of a cutline above the bonding voids versus distance are shown in Figure 7 below each microscope image to show the void detection limit. Infrared microscope images show the same void detection capability in all three stacks.

Apart from the programmed bonding voids, some random circular defects are also captured by infrared microscope as shown in Figure 7c. These round defects are roughly 2 µm to 10 µm in diameter and show similar contrast as the programmed voids. They are observed on the surface of 5 µm top Si at inspection step 3 by optical microscope and probably formed during dry etching.

In the case of dielectric-to-dielectric bonding, infrared microscope is an effective way to review the bonding voids. Regarding hybrid bonding in the D2W and W2W stacks, the bonding voids can occur in between metal interconnections like Cu pads, dielectric-metal interface, and bonding dielectric materials, which limits the functionality of infrared light as it is reflected by metals.

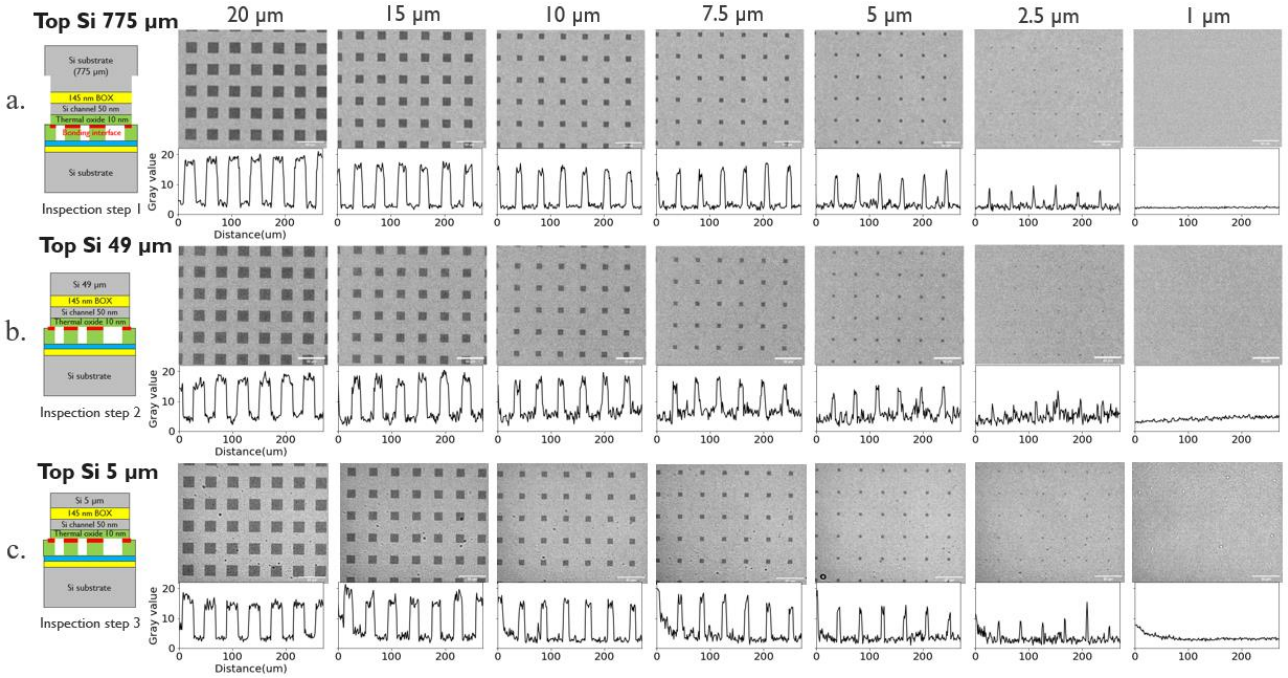


Figure 7 Infrared microscope images of the programmed voids from inspection steps 1 to 3. The grey values of a cutline above the bonding voids versus distance are shown in the figures below each microscope image.

3.4 Optical microscope

At inspection steps 4 and 5, the optical microscope in the visible light wavelengths can be used to detect bonding voids since the remaining Si thickness is no more than 50 nm at both inspection steps. Full wafer defect inspection was performed, and defect areas were reviewed. Both random defects and programmed bonding voids are detected in both steps and shown in the wafer maps in Figure 8a and b. Cropped defect maps showing the void patterns are indicated in Figure 8c and d together with the design patterns. Both individual voids and void matrices can be detected. The smallest detectable void size is 750 nm in both steps. Figure 8e and f show the microscope images of the 750 nm voids and the grey values of a cutline cross the 750 nm voids at inspection steps 4 and 5, respectively.

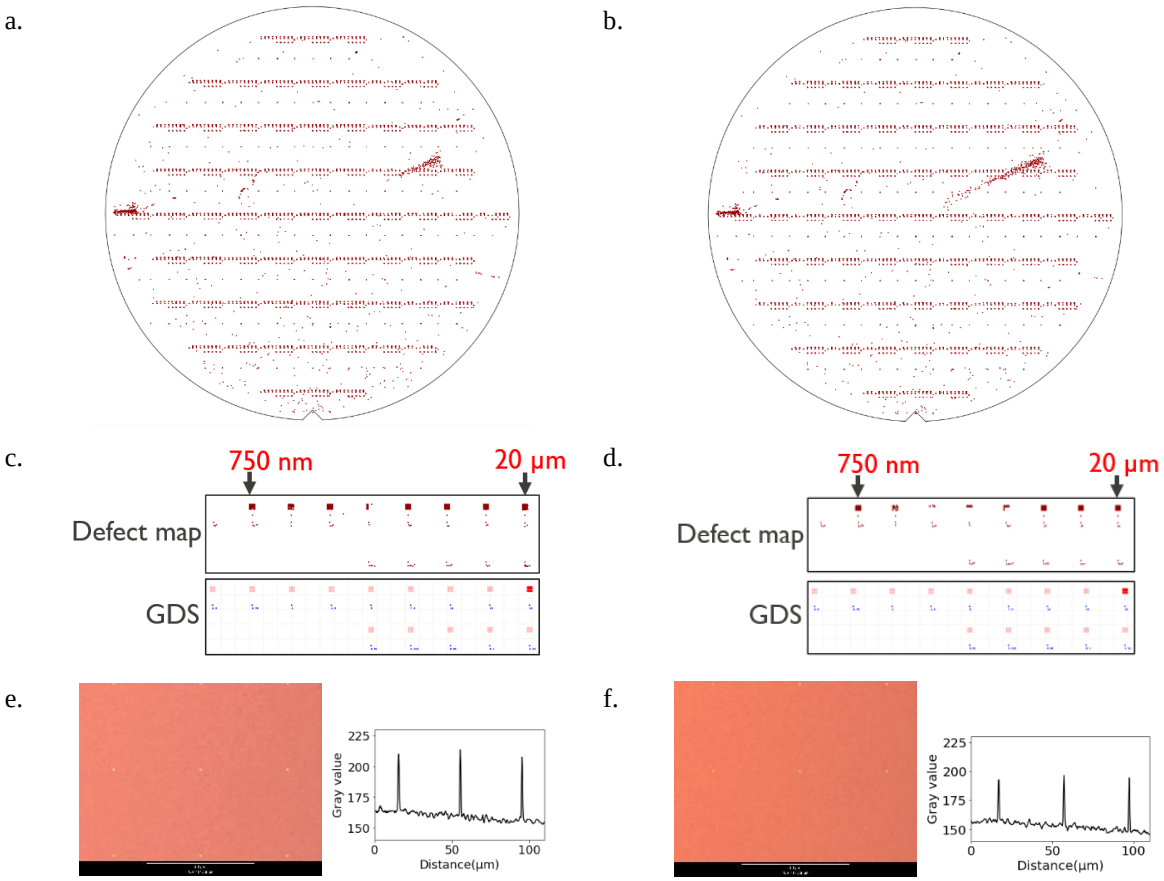
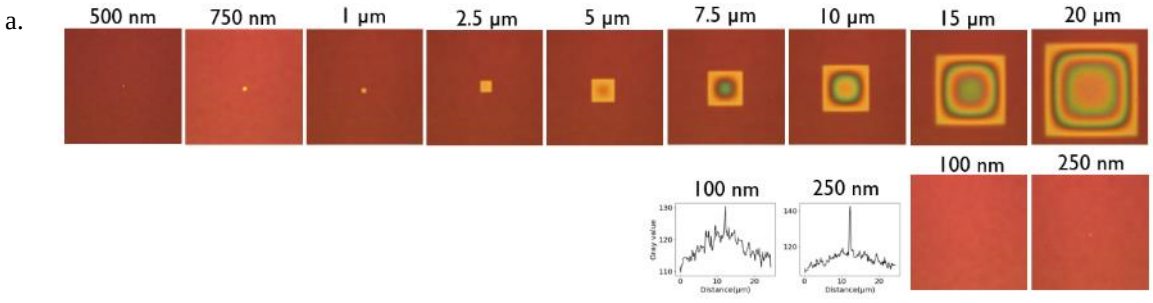


Figure 8 Defect wafer maps of the stacks at (a) inspection step 4 and (b) inspection step 5. Cropped defect maps of void patterns from (c) inspection step 4 and (d) inspection step 5 together with the designed patterns. Review images of the smallest voids (750 nm) detected in the inspection (e) inspection step 4 and (f) inspection step 5. The grey values of a cutline across the bonding voids versus distance are shown in the figures next to each microscope image.

The optical microscope also has a higher magnification camera. It cannot be used to scan the full wafer but can be used for the detailed review of a located programmed bonding voids. The smallest detectable void is 100 nm at both inspection steps 4 and 5 according to the figures of grey value as shown in Figure 9a and b. A series of colored fringes, so-called Newton's rings, due to the formation of blisters, are seen in the microscope images of voids ≥ 5 µm in both inspection steps.[10,11,12] AFM measurement in Figure 9c confirms the appearance of blisters for the voids ≥ 2.5 µm at inspection step 4 and for those ≥ 0.75 µm at inspection step 5, respectively. 3D AFM image of one 20 µm void at inspection step 4 is also shown.



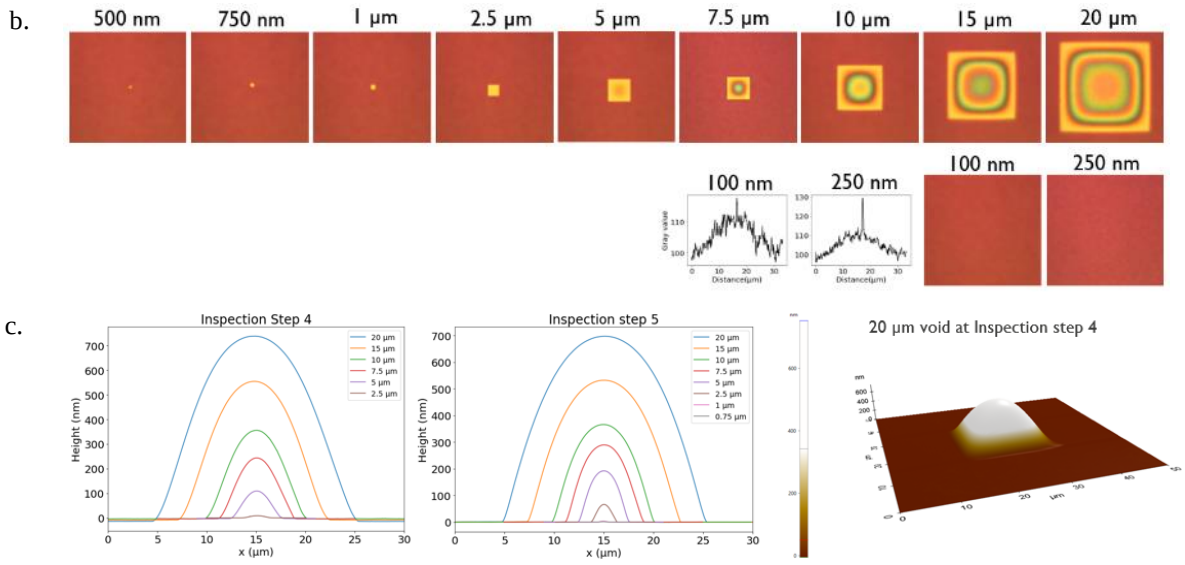


Figure 9 Optical microscope images with the review camera of detectable programmed bonding voids at (a) inspection step 4 and (b) inspection step 5. The grey values of a cutline over 100 nm and 250 nm voids are plotted. (c) AFM cross-section of the blisters at inspection steps 4 and 5. The maximum height versus void size is shown on the rightmost figure with an insert of the 3D AFM image of a 20 µm void at inspection step 4. The dashed lines are linear fit of the height versus void size.

3.5 Optical interferometry

Since there is topography above the programmed bonding voids at inspection steps 4 and 5, we can use optical interferometry method to detect them. Nanotopography can be derived from the measurement. Figure 10 shows that it can detect the void matrix consisting of 15 µm voids in both steps, but cannot detect individual voids. It can detect the plus signs of 100 µm by 20 µm and the numbers indicating void sizes. However, the height of the topography doesn't correspond to the AFM.

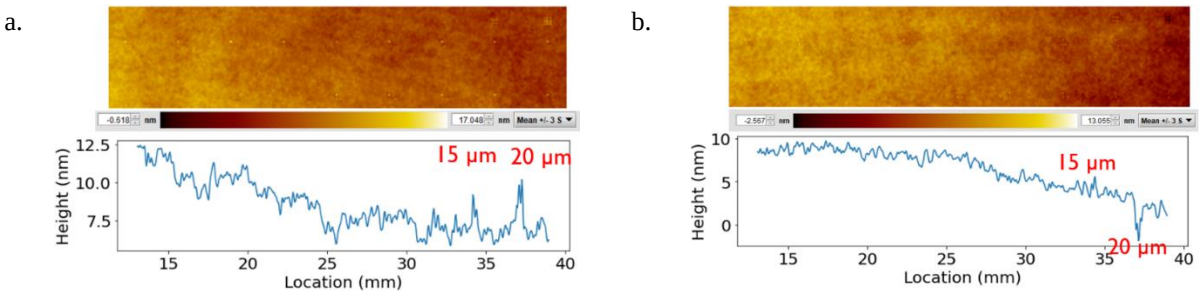


Figure 10 Nanotopography of the programmed voids derived from the interferometry measurements at (a) inspection step 4 and (b) inspection step 5.

3.6 High voltage scanning electron microscope

In a scanning electron microscope, higher acceleration voltage allows electrons to penetrate deeper into the stacks. At inspection step 4, there is roughly 145 nm of buried SiO_2, 50 nm of Si, and 10 nm of bonding oxide above the programmed bonding voids. At inspection step 5, the buried SiO_2 is removed, leaving only 50 nm of Si and 10 nm of bonding oxide. At these inspection steps, the top layers are thin enough for the electrons accelerated by different voltages to penetrate, and therefore HV-SEM could detect embedded bonding voids. As shown in Figure 11, the smallest detectable voids at inspection Steps 4 and 5 are 50 nm and 25 nm, respectively. Better void detection capability is found in the thinner top layer, i.e., inspection step 5. Special patterns are observed in the SEM images of voids from 2.5 µm to 20 µm at inspection step 5 as shown in Figure 11b. These are electron channeling patterns of single-crystalline Si [001].[13,14] These patterns are not apparent at inspection step 4 as the covering SiO_2 layer impedes any electron channeling.

In summary, the smallest detectable void size by HV-SEM is 25 nm below a stack of 50 nm of Si and 10 nm of SiO_2. The smallest detectable void size increases to 50 nm when there is an extra layer of 145 nm SiO_2 on top of the previous stack.

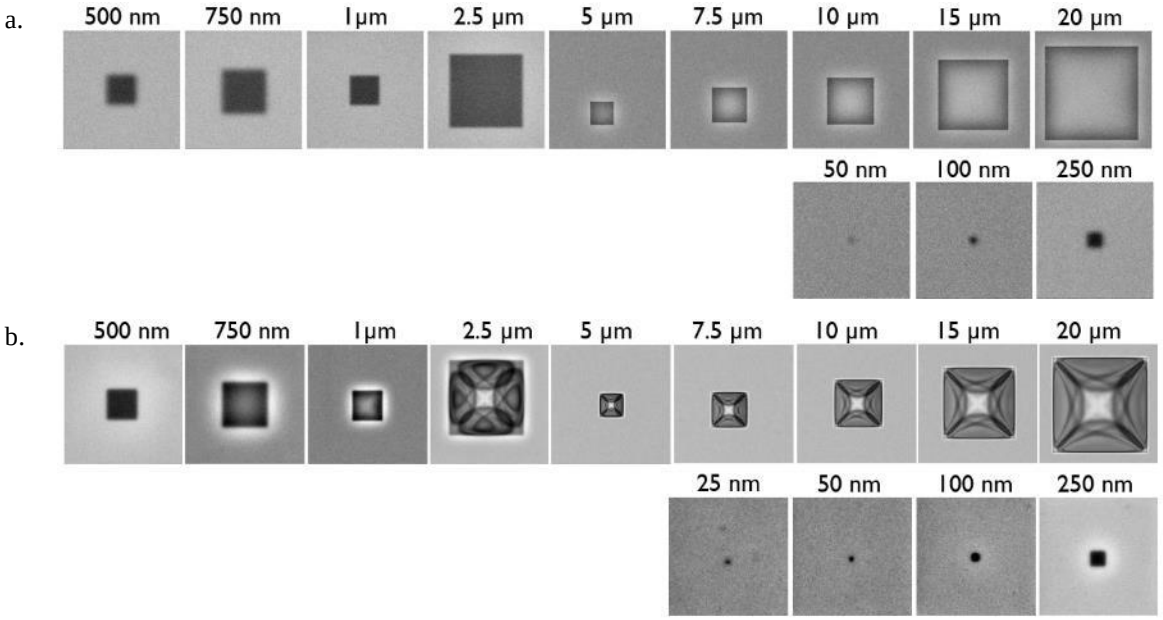


Figure 11 High voltage scanning electron microscope images of programmed voids of wafers at (a) inspection step 4 and (b) inspection step 5.

4. CONCLUSIONS

Wafers with programmed bonding voids from 10 nm to 20 µm have been fabricated. We have tested different inspection and review techniques to detect the buried voids after bonding and each thinning step as shown in Table 1. With a top Si of 775 µm (inspection step 1), 49 µm (inspection step 2), and 5 µm (inspection step 3), scanning acoustic microscope and infrared microscope can be used for the void detection. The smallest detectable individual voids for SAM equipped with 175 MHz transducers are 7.5 µm, 7.5 µm, and 10 µm from inspection steps 1 to 3, respectively. The infrared microscope can detect voids down to 2.5 µm in all 3 inspection steps. After removing Si substrate from the donor wafer, optical microscope with visible light wavelengths and high voltage scanning electron microscope can be applied for void detection. The optical microscope can detect down to 750 nm in both steps, while HV-SEM can detect a void down to 50 nm below a stack of 145 nm SiO_2/50 nm Si/10 nm SiO_2 (inspection step 4) and down to a void of 25 nm below a stack of 50 nm Si/10 nm SiO_2 (inspection step 5). Owing to the formation of blisters above bonding voids at inspection steps 4 and 5, optical interferometry can detect the void matrices consisting of down to 15 µm voids. The buried bonding voids of 10 nm have not been observed by any inspection and review techniques tested here. It remains a challenge to detect bonding voids as small as 10 nm, as well as sub-micron voids at double wafer thickness (before thinning). Among these techniques, SAM, optical microscope, and optical interferometry can be used for full wafer inspection with a high throughput, while infrared microscope and HV-SEM can be used for detailed defect review.

Table 1 Smallest detectable void size of different inspection techniques at all inspection steps.

Stack above bonding voids	Inspection step 1: Top Si 775 µm/ 145nm SiO_2/ 50 nm Si/ 10 nm SiO_2	Inspection step 2: Top Si 49 µm/ 145nm SiO_2/ 50 nm Si/ 10 nm SiO_2	Inspection step 3: Top Si 5 µm/ 145nm SiO_2/ 50 nm Si/ 10 nm SiO_2	Inspection step 4: 145nm SiO_2/ 50 nm Si/ 10 nm SiO_2	Inspection step 5: Top Si 50 nm/ 10 nm SiO_2
Scanning acoustic microscope	7.5 µm	7.5 µm	10 µm		
Infrared microscope	2.5 µm	2.5 µm	2.5 µm		
Optical microscope				0.75 µm	0.75 µm
Optical interferometry				15 µm matrix	15 µm matrix
High-voltage scanning electron microscope				50 nm	25 nm

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