Active area patterning for CFET – Nanosheet etch

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ABSTRACT

Nanosheet device architectures such as complementary FET (CFET) are candidates to replace FinFET, improving device performance while allowing a higher density of devices for a similar footprint. Two main challenges can be highlighted in the definition of the active area (AA) patterning for CFET. First the presence of stacked nanosheets generates the need for a higher aspect-ratio compared to FinFET. Secondly, the nanosheets layers, composed of silicon and silicon-germanium with varied thicknesses and concentrations, require new approaches in terms of process definition and control. The first results of an active area patterning for a full CFET device have been demonstrated at imec. Thicker nanosheet stacks are patterned opening the path to the creation of a complete CFET device.

Keywords: CFET, Nanosheet, Active Area

1. INTRODUCTION

In order to extend the Moore's law of transistor scaling novel device architectures are proposed, allowing the definition of smaller transistors, with a reduced footprint while still maintaining the performances of the devices. Scaling started with planar/horizontal designs and evolved to 3D definition of fins and Gate-All-Around structures[1]. New devices be using the vertical third direction to reduce the footprint[2]. Not only stacking can increase the device density but the new concept can also pave the way to a reduction of power consumption. CFET devices are the continuation of the evolution from FinFet, Nanosheet and Forksheet devices (Figure 1).

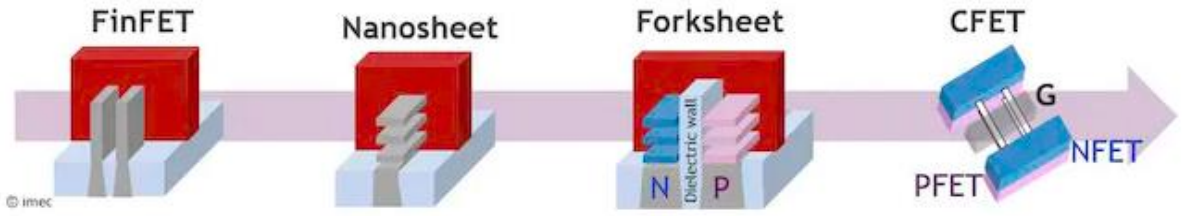

Figure 1 - Device evolution, from FinFET to CFET

If the 3D solution brings a great improvement potential, it also comes with new challenges, specifically in the integration of the structures in manufacturing. Two approaches have been studied [3], the monolithic approach[4] (or all in one wafer) and the sequential approach (2 wafer-approach). Each approach comes with its own challenges, the monolithic integration dealing with high aspect ratio and complex superlattice structures, the sequential approach requiring a high level of accuracy for the two wafers alignment.

The processes defined in this document focus on an application for the monolithic approach. In such an approach, both n-MOS and p-MOS devices (top and bottom) are stacked. Stacking the n-MOS and p-MOS devices results in the definition of high aspect ratio (HAR) patterning for the active area. Moreover, the HAR is combined with the requirements to pattern through a complex multi-material stack composed of silicon and silicon germanium (SiGe) layers with varied concentration. An example of a monolithic integration of a CFET device is represented in figure (Figure 2). The n-MOS and p-MOS channels are stacked on top of each other.

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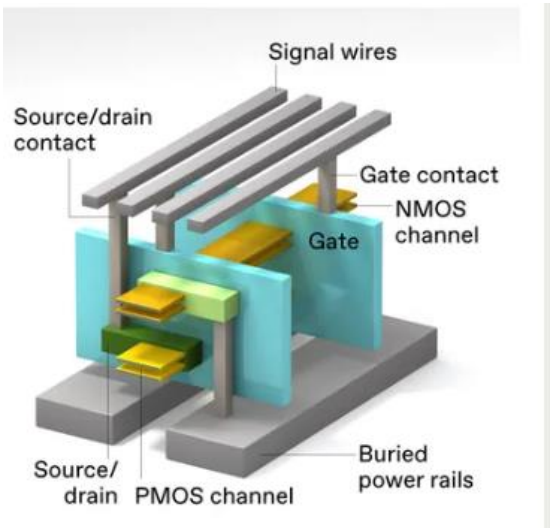

Figure 2 - CFET device structure with stack p-MOS and n-MOS channel with bottom contact using a buried power rail

In the approach used in this document SiGe layers, used as sacrificial layers will later be removed to be replaced by a dielectric layer to create top/bottom device isolation.

The active area patterning, also referred to as nanosheet (NSH) patterning is the first etching step of the front-end flow. The etching process comes after an epitaxial growth of the superlattice stack (NSH) and is followed by a shallow trench isolation (STI) formation. Downstream processes are STI fill, the Gate patterning and the source drain (SD) definition.

NSH patterning is critical to define a stable baseline for those following steps.

2. STACK AND PATTERNING

The stack is composed of multiple layers and can be decomposed between three main parts, the silicon fin, the NSH and the HM required for the patterning. The stack is represented in Figure 3.

The stack represented in Figure 3 shows a configuration on a Silicon-On-Insulator (SOI) wafer where silicon has been deposited on top of the BOx.

The definition of the silicon fin will follow a similar process for both bulk and SOI configurations. Minor adjustments will be performed to cope with the different configurations.

The oxide of the SOI will act as the stop layer creating the STI floor at the Box level. In a bulk Si wafer processing, without an etch stop layer, the process itself will define the STI floor.

The patterning is performed using EUV exposure. For development purposes, dense structures are used for process validation.

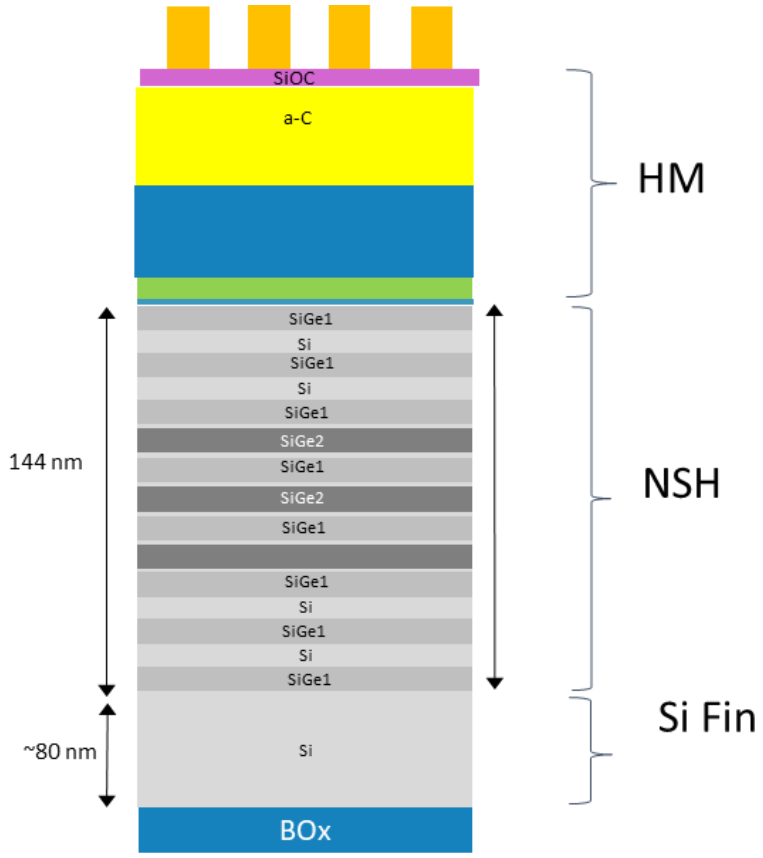

Figure 3 - 2x2 NSH stack, including Si FIN, NanoSHeets and Hard Mask

3. HARD MASK OPENING

The HMO has an essential role in the pattern CD control and in the profile of the pattern. Through the definition of the processes, we optimized the HMO to reduce the non-uniformity across the wafer to reduce the 3-σ range from 1.9 nm or 1.0 nm. Temperature skews were also performed, allowing to re-target the mean value of the CD.

4. NSH ETCH

4.1.1 Multistep process

The Nanosheet Etch (NSH) is a complex process designed to cope with a multilayer stack. The multilayer stack is composed of Silicon and Silicon Germanium with varied concentrations. The process is split into four blocks.

The first block acts as a passivation layer protecting the top of the HM. It prevents shouldering of the HM and thus limits the risk of tapering of the profile.

In the second block an approach of etch and passivation is used to pattern the Silicon and Silicon-Germanium layers while protecting the sidewall. The sidewall protection limits the risk of notching in the weakest silicon germanium layers. After processing of block 2 the superlattice is etched stopping into the silicon fin.

The third block, in a similar way to the first block, provides extra protection to the already etched silicon/silicon germanium layers by covering the sidewalls with a passivation layer. This passivation allows us to continue with processing block 4 without major impact on the superlattice.

The block 4, uses a more standard approach, similar to a STI etch. The process is time based and allows to reach the Box (for SOI wafers) or define the STI floor (for bulk silicon substrates).

The development discussed in this document focuses mainly on block 2 (superlattice etch) and block 4 (Si etch/STI).

4.1.2 Process optimization

The process in block 2 relies on balancing etch and passivation. Passivation is mostly used for the control of two elements, the suppression of a bulge and the profile control of the silicon fin. On a first version of the process (Rev. 1.0 - Figure 4 - left) a bulge is visible at the bottom of the nanosheet. A tapered profile is also visible in the silicon fin.

The first passivation optimizations allowed to suppress the bulge but increased the tapered profile. After several adjustments, a process has been set, allowing to obtain a straight profile from the top to the bottom of the NSH and to remove the presence of the bulge.

To obtain our process revision 2 (Figure 4 – right), a co-optimization was performed. It consists in limiting the block 2 process to the NSH etch to let the silicon fin etch happen through block 4. Block 4 offers a better selectivity towards oxide. By favorizing block 4 processing over block 2 we manage to achieve a reduced oxide HM consumption and to limit the risk recessing into the bottom oxide.

Such optimization, not only allow to provide a straight profile along the complete pattern, but also increase the process window, allowing to cope with incoming variation in the stack.

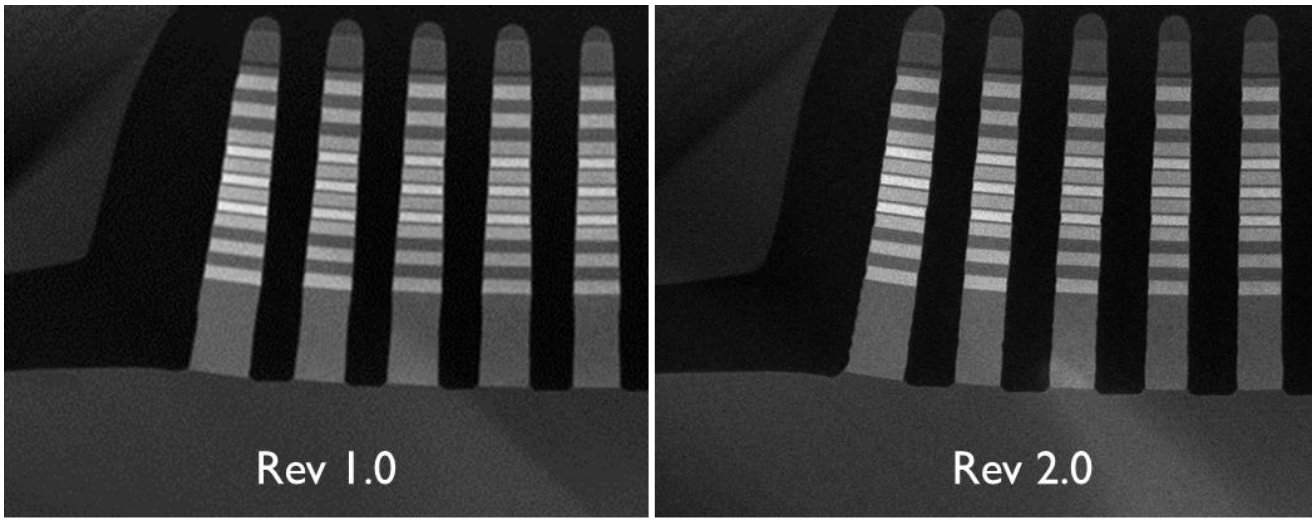

Figure 4 – TEM- Left: process Rev. 1.0 – Right: Process Rev2.0

5. CONCLUSION

In this document, the development and optimization of the NSH patterning were discussed. We demonstrated the capacity to pattern a complex stack with accurate control of key parameters. The profile was kept vertical, the SiGe layers integrity was preserved.

The processes developed are shown to be adaptable, allowing to handle variations from the stack (variations of the layers thicknesses, Ge concentration) but also with depth variations of the STI floor.

The separate processing blocks approach allowed us to define a versatile process able to cope with the active area etch supporting for the future the challenges of CFET.

6. ACKNOWLEDGMENTS

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