# Source mask optimization (SMO) study for high-NA EUV lithography to achieve single patterning on random logic metal

Soobin Hwang<sup>a,b</sup>, Werner Gillijins<sup>b</sup>, Stefan de Gendt<sup>a,b</sup>, Ryoung-han Kim<sup>b</sup>

<sup>a</sup>KU Leuven, Celestijnenlaan 200, 3001, Heverlee, Belgium; <sup>b</sup>imec, Kapeldreef 75, B-3001 Leuven, Belgium

## ABSTRACT

High numerical aperture (NA) extreme ultraviolet (EUV) lithography single patterning is evaluated through source mask optimization (SMO). The patterning performance is assessed on random logic metal design with minimum pitches of 24, 22, and 20nm in the horizontal direction to confirm the feasibility of logic metal scaling. We set a 1 square micron as a cell window and choose 200 gauges to include various types of features such as dense, isolated, and tip-to-tip. SMO is performed assuming eight permutations of a) dark-field versus bright-field, b) Ta-based versus low-n attenuated phase-shift masks, and c) with sub-resolution assist feature (SRAF) versus without SRAF. For each design, the process window is estimated.

Keywords: EUV lithography, high-NA EUV, Source mask optimization

# 1. INTRODUCTION

As the scaling towards increased transistor density continues in the semiconductor industry, photolithography has been considered the key technology enabler to meet the dimensional requirement for circuit design. Photolithography technology has evolved based on Abbe's resolution formula. To enhance resolution, the industry has strived to reduce the wavelength of the light source and increase the numerical aperture for printing smaller features with higher contrast. With the introduction of high-volume manufacturing in EUV lithography, successful single patterning has been achieved down to a pitch of 28nm.<sup>1</sup> The pitch scaling is anticipated to continue, with the expectation that the utilization of high-NA EUV lithography at 0.55 NA will facilitate the production of smaller features.<sup>2</sup> Thus, it is essential to forecast possible pitch scaling scenarios through the study of SMO.

In our previous research, high-NA SMO studies assuming negative tone resist usage were reported on N3 imec random logic metal. The studies addressed the feasibility of single patterning while evaluating the impact of design orientations and mask tonality. To achieve this, combinations of dark-field masks for the direct metal etch process and bright-field masks with the negative tone resist for the damascene process were employed.<sup>3</sup> However, there are still aspects that have not been addressed, and investigating these aspects would be crucial. From a design perspective, evaluating P22 design, which could serve as a pivotal point, is necessary. Additionally, trench patterning with dark-field masks is also required for the preparation of a damascene-based metallization. Furthermore, evaluating the consideration of SRAF insertion on bright-field masks remains necessary.

In this paper, we assess SMO results for various mask solutions including mask tonality, mask absorber, and SRAF which is one of the important resolution enhancement techniques, to check the feasibility of single patterning and anticipate mask choice in high NA EUV lithography. All simulations are conducted assuming trench patterning for the damascene process. Evaluation is conducted on imec random logic metal designs, targeting the node of A14 and below. Furthermore, the required minimum width rule of SRAF and its impact on wafers is assessed with respect to optical proximity correction and mask-writing technology. Finally, we estimate tip-to-tip (T2T) printability of mask solutions by checking image log slope (ILS).

DTCO and Computational Patterning III, edited by Neal V. Lafferty, Proc. of SPIE Vol. 12954, 129540X · © 2024 SPIE · 0277-786X · doi: 10.1117/12.3010869

# 2. METHODS

### 2.1 Design preparation

Figure 1 shows the random logic metal design for the experiment. We select two hundred gauges in a one-square-micron design area, encompassing various features, including dense lines, isolated, two-bar, and tip-to-tip (T2T) patterns as well. The target pitches of the design are 24, 22, and 20nm. The target tip-to-tip sizes are 17.5, 16.0, and 14.5nm, respectively.



Figure 1. Random logic metal design

### 2.2 Various Mask Options and SRAF Insertion

Figure 2 illustrates the various mask options for the assessment. In evaluating single patterning, it is crucial to consider various combinations of mask tonality and absorber. Regarding mask tonality, both dark-field and bright-field masks are employed, while for absorbers, considerations encompass Ta-based masks and low-n attenuated phase-shift masks. Lastly, the evaluation is conducted, considering the insertion of SRAF.



Figure 2. Schematic diagram of various mask options considering mask tonality, absorber and SRAF insertion

### 2.3 Simulation Settings

### 2.3.1 Lithography Process Assumptions

Figure 3 explains lithography assumptions for trench patterning. To print trenches, two combinations are primarily necessary: the dark-field masks in conjunction with positive tone resist, specifically chemically amplified resist (CAR) and the bright-field masks paired with negative tone resist, particularly metal oxide resist (MOR). In the process of optical modeling, this is achieved by modifying aerial image-blur parameters to mimic the resist behavior of CAR and MOR<sup>4,5</sup>.

### 2.3.2 Minimum Mask Rule

In consideration of mask regulations, we have established the minimum mask rule at 24nm, as determined by the current capabilities of mask writing. Owing to anamorphic imaging, the high-NA mask undergoes stretching by a factor of 4 in the x-direction and 8 in the y-direction relative to the design. Consequently, the minimum width of vertical patterns is 6nm, while horizontal patterns have a width of 3nm at the design level.



Figure 3. Lithography process assumptions for trench patterning and its aerial image blur terms to mimic the resist behavior.

### 2.4 Mask Optimization (MO) Flow

In this paper, simulations are executed under the operating parameters of the EXE:5000 high-NA EUV scanner<sup>6</sup>. All simulations are conducted using the recent version of ASML Tachyon<sup>7</sup>, and the default template of MO is used except for the rule of minimum mask width. The experimental procedure is outlined as follows: Mask optimization is performed using sources that were previously optimized for each combination of mask absorber and tonality<sup>3</sup>. Throughout this procedure, the insertion of SRAF is considered to evaluate its potential impact, including the mitigation of the best focus shift. Subsequently, employing the optimized mask, the process window is calculated for each gauge, and the performance of each combination is assessed using exposure latitude versus depth of focus analysis (ED plot).

# 3. MASK OPTIMIZATION RESULTS

### 3.1 MO results of 24nm random logic metal

Figure 4 illustrates ED plots for a 24nm pitch of random logic metal design. The upper ED plot represents the results without the insertion of SRAF into each mask, while the lower graph illustrates the outcomes with the insertion of SRAF. In the figure, the right plot depicts the DOF at EL of 8% of all the mask configurations. Among all the mask options, the best cases are represented with green color. As shown in the figure, the MO with SRAF provides a larger DOF than the MO without SRAF. Compared to bright-field masks, SRAF insertion in dark-field masks is more effective. Especially, DOF in the low-n dark-field masks is increased by 80% with the insertion of SRAF. Smaller DOF in low-n dark-field masks between dense and isolated features. In the comparative analysis between binary dark-field and bright-field masks, it is observed that binary dark-field masks open larger DOF than bright-field masks.



Figure 4. Comparison among the mask configurations for P24 design. Left-top: ED plot of masks without SRAF; Left-bottom: ED plot of masks with SRAF; Right: DOF plot of all mask options.

### 3.1.1 Impact of SRAF in low-n dark-field mask

Figure 5 illustrates the impact of the SRAF insertion in the low-n dark-field masks. The left and right column are the results of MO with and without SRAF, respectively. In the OPW without SRAF, the semi-iso features limit the OPW. The SRAF insertion can mitigate the best focus shift as well as increase individual process windows.

### 3.1.2 DOF comparison between Ta-based dark-field and bright-field masks

Figure 6 presents DOF distribution of all measured gauges through box plot. The left plot is for Ta-based bright-field, and the right plot is for the Ta-based dark-field masks. The median in dark-field is ~12nm higher than in bright-field masks. Also, the values in dark-field exhibit higher DOF distribution compared to bright-field.



Figure 5. The variation of OPW due to SRAF insertion. Left: Process limiters on the mask without SRAF and OPW of mask without SRAF; Right: OPW of the mask with SRAF.



Figure 6. DOF boxplot of all gauges on Ta-based bright-field and dark-field masks.

### 3.2 MO results of 22nm random logic metal

Figure 7 shows ED plot of each mask option (Left) and DOF values from OPW at 8% EL(Right). As discussed in P24 results, SRAF insertion on low-n dark-field masks mitigates the best focus shifts. For this reason, In the case of the low-n dark-field mask, a comparison is conducted considering the insertion of SRAF.

The results exhibit a similar trend to the results of P24. First, dark-filed masks have larger DOF than bright-field masks. Second, among all the options, low-n dark-field masks with SRAF show the largest DOF.



Figure 7. Comparison among the mask configurations for P22 design.

### 3.3 MO results of 20nm random logic metal

Figure 8 illustrates ED plots of mask options without (Left-top) and with SRAF(Left-bottom), and the DOF at EL of 8% (Right). Different from previous results, all the dark-field masks have a rapid decrease in DOF. Compared to dark-field masks, bright-field masks are expected to provide approximately a DOF of 35nm at an EL of 8%. In bright-field masks, SRAF insertion helps to increase 10% of DOF.



Figure 8. Comparison among the mask configurations for P20 design.

# 4. SRAF CONDITIONS AND MANUFACTURABILITY

SRAF is one of the Resolution Enhancement Techniques (RETs), and it is positioned near the main feature to enhance the image contrast of the main feature through constructive interference<sup>8</sup>.

Typically, in logic design, a smaller minimum width rule for SRAF allows for more intricate SRAF insertion on the mask, while larger sizes, within the bounds of non-printability, improve image contrast. This aids in improving DOF and mitigating best focus shift by reducing mask 3D effects<sup>9</sup>.

While a smaller minimum SRAF width is advantageous from the standpoint of OPW, considerations regarding the feasibility of mask writing are necessary. As described in Figure 9, the minimum width of the absorber and mirror achievable with current multi-beam mask writers is approximately 3nm at the design level, which informs the determination of the minimum width rule.



Figure 9. Mask CD-SEM images according to different CD on Ta-based masks.

Figure 10 depicts the minimum SRAF conditions required to avoid SRAF printing on Ta-based bright-field masks. The left graph illustrates the aerial image distribution when both main features and SRAF are present, while the right figure



Figure 10. SRAF size to avoid printing. Left: Aerial image distribution; Right: Corresponding mask design.

represents the corresponding mask design. On P20 design, we anticipate that SRAF width to avoid printing would be around 3nm, which can be supported by current mask technology.

# Low-n / DF Low-n / BF Ta-based / DF Ta-based / BF

# 5. TIP-TO-TIP PRINTABILITY ON P20 RANDOM LOGIC METAL

Figure 11. ILS boxplot of gauges at T2T on mask options without SRAF

Figure 11 represents image log slope (ILS) distribution of all T2T patterning using box plots, categorized by mask options. For T2T printability, we expect that the ILS should be around 100 1/um.<sup>3</sup> The figure shows bright-field masks exhibit higher ILS distribution compared to dark-field masks. Moreover, low-n bright-field masks demonstrate higher ILS than Ta-based bright-field masks.

# 6. CONCLUSIONS

Mask optimization studies with different mask tonality, absorber, and SRAF are conducted on random logic metal design. To assume trench patterning, dark-field with PTD (CAR) and bright-field in conjunction with NTD (MOR) combinations are considered in the modeling by adjusting different aerial image blur. By P22 design, dark-field with PTD (CAR) shows overlap process window which exceeds a DOF of 35nm at an EL of 8%. Low-n dark-field with SRAF option is expected to enable a DOF of 50 nm at 8% EL. Ta-based dark-field masks are anticipated to allow a DOF of 45nm. From P20 design, dark-field masks with PTD (CAR) show small overlap process window. Bright-field masks with NTD (MOR) are foreseen to enable a DOF of 35nm and The SRAF insertion improves DOF by 10%. The required minimum SRAF to avoid printing is ~3nm at 1x scale, on the horizontal design. Regarding T2T printability, bright-field masks have better ILS.

# REFERENCES

[1] Dongbo Xu, Werner Gillijns, Ling Ee Tan, Vicky Philipsen, Ryoung-Han Kim, "Exploration of alternative mask for 0.33NA extreme ultraviolet single patterning at pitch 28-nm metal design," J. Micro/Nanopattern. Mats. Metro. 21(2) 024401 (7 April 2022) https://doi.org/10.1117/1.JMM.21.2.024401

[2] Eelco van Setten, Gerardo Bottiglieri, John McNamara, Jan van Schoot, Kars Troost, Joseph Zekry, Timon Fliervoet, Stephen Hsu, Joerg Zimmermann, Matthias Roesch, Bartosz Bilski, Paul Graeupner, "High NA EUV lithography: Next step in EUV imaging ," Proc. SPIE 10957, Extreme Ultraviolet (EUV) Lithography X, 1095709 (26 March 2019); https://doi.org/10.1117/12.2514952

[3] Dongbo Xu, Ling Ee Tan, Vicky Philipsen, Joerg Zimmermann, Werner Gillijns, "Feasibility of logic metal scaling with 0.55NA EUV single patterning," Proc. SPIE 12494, Optical and EUV Nanolithography XXXVI, 124940M (28 April 2023); https://doi.org/10.1117/12.2657983

[4] Shih-En Tseng, Chun-Kuang Chen, Dong-Seok Nam, Will Lin, Anthony Yen, "A study of patterning 36nm-pitch logic contact holes in a metal oxide resist using a high-reflectance phase-shifting mask that results in image reversal," Proc. SPIE 12293, Photomask Technology 2022, 122930C (1 December 2022); https://doi.org/10.1117/12.2642302

[5] Timothy A. Brunner, Vincent Truffert, Christopher Ausschnitt, Nicola N. Kissoon, Edouard Duriau, Tom Jonckers, Lieve van Look, Joern-Holger Franke, "Image contrast metrology for EUV lithography," Proc. SPIE 12292, International Conference on Extreme Ultraviolet Lithography 2022, 122920A (1 December 2022); https://doi.org/10.1117/12.2640647
[6] Jan van Schoot, Eelco van Setten, Gijsbert Rispens, Kars Z. Troost, Bernhard Kneer, Sascha Migura, Jens Timo Neumann, Winfried Kaiser, "High-numerical aperture extreme ultraviolet scanner for 8-nm lithography and beyond," J. Micro/Nanolith. MEMS MOEMS 16(4) 041010 (30 October 2017)

https://doi.org/10.1117/1.JMM.16.4.041010

[7] Stephen Hsu, Rafael Howell, Jianjun Jia, Hua-Yu Liu, Keith Gronlund, Steve Hansen, Jörg Zimmermann, "EUV resolution enhancement techniques (RETs) for k1 0.4 and below," Proc. SPIE 9422, Extreme Ultraviolet (EUV) Lithography VI, 94221I (16 March 2015); https://doi.org/10.1117/12.2086074

[8] Lars W. Liebmann, James A. Bruce, William Chu, Michael Cross, Ioana C. Graur, Joshua J. Krueger, William C. Leipold, Scott M. Mansfield, Anne E. McGuire, Dianne L. Sundling, "Optimizing style options for subresolution assist features," Proc. SPIE 4346, Optical Microlithography XIV, (14 September 2001); <u>https://doi.org/10.1117/12.435690</u>

[9] Iacopo Mochi, Vicky Philipsen, Emily Gallagher, Eric Hendrickx, Kateryna Lyakhova, Friso Wittebrood, Guido Schiffelers, Timon Fliervoet, Shibing Wang, Stephen Hsu, Vince Plachecki, Stan Baron, Bart Laenens, "Assist features: placement, impact, and relevance for EUV imaging," Proc. SPIE 9776, Extreme Ultraviolet (EUV) Lithography VII, 97761S (18 March 2016); https://doi.org/10.1117/12.2220025